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Factory Acceptance

Test Procedure

For ESS RSMS-PS

2

ASSY SERIAL NO. : 1700704

Factory Acceptance Test Procedure
Part number 8100093700
Document TP-8800110290

Preparation/Review	Signature	Date
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Revision History Log:

Date:	Rev.:	Init:	Changes:
2016-12-23	A	CN	Initial version
2017-02-02	B	CN	Minor changes after DDR
2017-08-24	C	CN	Minor changes after Review
2017-11-30	D	CN	Minor changes; 8500-->8700, first test findings

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1. Scope

This Test Report covers the calibration procedure and the pre-shipment factory test of the Power Supply.
The objective of the test is to verify that the build standard complies with the agreed specification.

This Test Report is divided into the following sections:

Introduction:	This chapter
Acceptance Data:	Key requirements and notes on the recorded performance.
Functional Test:	Procedures for the initial verification and adjustments.
Full Power Test:	Procedures for the long term, full power tests and regulation verification.
As-built Notes:	Lists all configuration/calibration parameters, setups, serial numbers etc.
Final inspection:	Instructions for final inspection before shipment.

1.1. Applicable Documents

AD1. "Appendix_1"

AU, Technical Specification for the pulsed raster scanning system, March 2016

AD2. Quotation 502446
Danfysik; Purchase of the raster scanning magnets for the ESS project, 20-04-2016

AD3. 502446 PDR Rev-B

DF, Preliminary Design Report 25-11-2016

AD4. 502446 DDR Rev-A

DF, Detailed Design Report, 22-12-2016

AD5. 8200093700.E

RSMS-MPS Main schematic

1.2. Abbreviation used

- **CPS** Charge Power Supply
- **DF** Danfysik A/S
- **DRM** Digital Regulation Module
- **DUT** Device Under Test
- **DVM** Digital Voltmeter
- **H,W,D** Height, Width, Depth
- **N/A** Not Applicable
- **PSU** Power supply
- **RSMS** Raster Scanning Magnet System
- **S/C** Short Circuit(ed)
- **TBD** To Be Defined
- **TP#** Test Point number

1.3. Test environment

Ambient temperature: 25±5°C
Humidity: <90%

2. Preparation,

2.1. Equipment

Equipment Reference	Equipment Manufacture and Model	ID: Comment	Calibration date	Calibration due
A	Multimeter Fluke 177	Reg.nr. 1382	___ / ___ 20__	___ / ___ 20__
B	PC HP	MHNN	___ / ___ 20__	___ / ___ 20__
C	Hi-Pot – Earth Tester GW Instek GPT-9804	Reg.nr. 1757-1)	9 / 6 2017	9 / 6 2018
D	Oscilloscope Tektronix TPS2014	su. C013517	___ / ___ 20__	___ / ___ 20__
E	Current probe Tektronix TCP-404XL	1916	___ / ___ 20__	___ / ___ 20__
E	DCCT Danisense DS600IDSM		___ / ___ 20__	___ / ___ 20__
	Testo 625	Reg.nr. 1760-1)	2016-02-17	2018-02-17

2.2. Pre-setting of the module

Described in the specific test points

3. Acceptance Data

DF Ref.	Parameter	Requirement	Comments	Measured Passed	Remarks See also	Test Eqp. Ref.
1.	**Input**					
1.1.	Main Input Voltage variation	230V_{AC}	+/-10%, 1PH+N+PE		Rem 2	
1.2.	Input Frequency	50 – 60Hz			Rem 2	
1.3.	Fuse/ Breaker	10 A 10 A	Control Crate rear Control Crate front		Rem 2	
1.4.	Cooling	Air				
2.	**Output**					
2.1.	Output Voltage, max	±700Vpk		635	150	
2.2.	Output Current	±340Apk		340	142	
2.3.	Scanning Burst Duration	3.57 ms.	Useable raster period	passed	4.13	
2.4.	Pre scanning settling time	500 µs	Burst prior to usable raster period	N/A	-	
2.5.	Pulse burst repetition rate	up to 14 Hz.	Ext. trigger	passed	4.14	
2.6.	Output current shape	Triangle (±3dB @ 200kHz)	Load dependent	passed	4.15	
2.7.	Synchronization accuracy	<200ns		164	5.2	
2.8.	Operating Range	6.9% to 100%		passed	81	
2.9.	Operation Frequency	10kHz to 40kHz		passed	4.10	
2.10.	Absolute accuracy	<1%	Amplitude accuracy	3%	4.12	
2.11.	Burst droop	<1%	First to last pulse in a burst (usable period)	0.9%	4.13	
2.12.	Stability	<1%	±10% Mains; ±5% Load ±10° C Air; 8 Hours	1.7%	5.1	
2.13.	OFFSET (Symmetry)	<1%	Of full current	0.9%	4.12	
2.14.	Output Earth Connection	Minus DC- Link voltage	Earth connected to minus of the DC Link voltage	N/A	-	
3.	**Load**					
3.1.	Magnet Load	7.8µH ±10% 9mΩ ±10%	With cable termination filter in parallel	N/A	-	
3.2.	Cable	4 x 16mm2 shielded cables	30m<Length<35m Two cables connected in parallel to reduce cable inductance	35	-	

DF Ref.	Parameter	Requirement	Comments	Measured Passed	Remarks See also	Test Eqp. Ref.
4.	**Protection**					
4.1.	Internal Interlocks Turns PSU OFF	Over-Current Over-Voltage PS Over Temp. Reg. failure	> 130% > 120% > 80° C Missing OK signal from module	passed		
4.2.	External Interlocks Turns PSU OFF	EXT 1 EXT 2 EXT 3	Wired to mag. over-temp.	passed	4.4	
5.	**Interface**					
5.1.	Remote line	Ethernet,	SCPI protocol	passed	4.17.2	
5.2.	Current setting resolution Digital	16 bit		N/A	Rem 2	
5.3.	Pulse freq. setting	12 bit		N/A	Rem 2	
5.4.	Output Current Read Back Digital	8 bit plus sign		N/A	Rem 2	
5.5.	DC Link Voltage Read Back Digital	8 bit incl. sign		N/A	Rem 2	
5.6.	Front Panel Control	Yes		passed	4.17.1	
5.7.	Software Status signals (Locally and Remotely accessible)	ON / OFF REM / LOC PSU ready Polarity req.missing Pre-trig failure		passed	4.17.2	
5.8.	Hardware Timing input signals	Pre-Trig Polarity	Trig burst on rising edge High->Pos., 10KHz->Neg.	passed	4.7 4.17.5	
5.9.	Hardware Timing and status output signals	Beam Run Perm. Trig Permit Status I-Ready /Pol.req.missing /Pre-trig failure		passed	4.17.5	
5.10.	B-DOT	±10 V (±1V)	dB/dt pick-up coil on magnet return yoke leg	~±6V ~±9.5Vpk	4.17.4	
6.	**Cooling**					
6.1.	Cooling	Air, ΔT<10°C	Input Converter Output Converter Control Crate	9.2	5.1	
6.2.	Power dissipation	Load: 6% Cable: 66% PSU: 28%	Approximate figures.	N/A		
7.	**Mechanical**					
7.1.	Size	19" rack mounted 8U high 650mm. deep		13U *		
7.2.	Connection Mains	Rear		passed		

* External control panel

DF Ref.	Parameter	Requirement	Comments	Measured Passed	Remarks See also	Test Eqp. Ref.
7.3.	Connection Output	Rear		passed		
7.4.	Cabinet colour	RAL 7035		passed		
7.5.	Weight	<20kg <45kg <10kg	Input Converter (CPS) Output Converter Control Crate	not meas.		
8.	**Mechanical**					
8.1.	Relative Humidity	<90%	Non-condensing	not meas.		
8.2.	Norms	CE EN-61010-1 IEC 61508	European Safety Safety	passed	Rem. 3 4.2	

Remarks.

1) Not tested due to power limitation in the test stand. Ensured through design and previous tests at lower power.
2) Ensured through design.
3) Verified under module test.

4. Functional Test

4.1. Pre Inspection

Following test are performed without the power supply connected.

Test Step	Description	Accept Criteria	Result
1.	Check Main cables are tightened.	No visual damage	OK / Not OK
2.	Check protective bonding cables are tightened.	M4: 1.2Nm M5: 2.0Nm M6: 3.0Nm M8: 6.0Nm	OK / Not OK
3.	Check Fuses and ratings: F3 (Control Crate): 3.15 AT F4 (Control Crate): 1 AT X8 (Control Crate): 10 AT X9 (Output Converter): 315 mAT	Correct fuses	OK / Not OK
4.	Visual inspection of crates: • Output Converter. • Control Crate • Connection box (at magnet girder leg)	Cabinets are clean, free from swarf, loose cable cores and other foreign objects.	OK / Not OK

4.2. Grounding Continuity Test

Test Step	Description	Accept Criteria	Result
5.	Connect a 10A power supply minus terminal to the control crate grounding point.	-	OK / Not OK
6.	Connect plus terminal to the following externally accessible parts and measure the voltage at the applied 10A:		
	• Capacitor Charge PS cabinet	< 1V	0.708 V
	• Capacitor Charge PS top plate	< 1V	0.630 V
	• Capacitor Charge PS front plate	< 1V	0.465 V
	• Output Converter cabinet	< 1V	0.568 V
	• Output Converter top plate	< 1V	0.584 V
	• Output Converter front plate	< 1V	0.501 V
	• Output Converter mains inlet, PE pin	< 1V	0.482 V
	• Control Crate cabinet	< 1V	0.136 V
	• Control Crate top plate	< 1V	0.265 V
	• Control Crate front plate	< 1V	0.256 V
	• Control Crate mains inlet, PE pin	< 1V	0.242 V
7.	Connect plus terminal to the following internal parts and measure the voltage at the applied 10A:		
	• Star ground point in Control Crate	< 1V	0.187 V
	• Main heat sink in Output Converter	< 1V	0.591 V

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4.3. Initial Testing and Setup

Test Step	Description	Accept Criteria	Result
 8.	For Safety: Place extra grounding bracket at Capacitor/MOSFET module, X57/X58.	-	OK / Not OK
9.	Turn OFF power for CPS	-	OK / Not OK
10.	Apply MAIN voltage 230V to Control Crate. Measure supply voltage, phase to phase	-	232.4 V
11.	Check that fan in Control Crate is running.	-	OK / Not OK
12.	Adjust Over Current threshold on DRM to 50% (measure on TP5.5, GND on TP5.8, adjust POT6)	853mV±20mV	OK / Not OK
13.	Adjust Capacitor Charge Over Current threshold on DRM to 120% (measure on TP8.1, GND on TP8.12, adjust POT4)	6V±60mV	OK / Not OK
14.	Adjust Capacitor Bank Over Voltage threshold on DRM to 750V (measure on TP8.2, GND on TP8.12, adjust POT2)	-4.433V±40mV	OK / Not OK

4.4. Interlock Test

Test Step	Description	Accept Criteria	Result
 15.	For Safety: Place extra grounding bracket at Capacitor/MOSFET module, X57/X58.	-	OK / Not OK
16.	"Un-dock" the grounding bracket on Capacitor/MOSFET module, X32. Verify "MPS Over-temp/Grounding Bracket" Interlock in Control panel.	-	OK / Not OK
17.	"Re-dock" grounding bracket and reset interlock.	-	OK / Not OK
18.	Disconnecting one wire at thermal switch TSW1. Verify "MPS Over-temp/Grounding Bracket" Interlock in Control panel.	-	OK / Not OK
19.	Activate External Interlock #1 by opening input X1.7-8. Verify External Interlock in Control panel.	-	OK / Not OK
20.	Activate External Interlock #2 by opening input X1.9-10. Verify External Interlock in Control panel.	-	OK / Not OK
21.	Activate External Interlock #3 by opening input X1.11-12. Verify External Interlock in Control panel.	-	OK / Not OK

4.5. Functional, Internal HV Isolation Test

Test Step	Description	Accept Criteria	Result
22.	Turn off main power Remove all power to the system. Connect external manual control panel to the CPS, allowing manual control of output voltage and current. (Connect test jig 0171 "CPS" cable to control crate X3 (CPS interface) to satisfy the regulation module.) Remove grounding bracket at V_{HV} Set the unpowered CPS voltage knob to minimum level. Set CPS to local mode. Turn on power switch of the CPS. WARNING: From this point onwards the output can be energized up to 1kV!	-	OK / Not OK
23.	Connect one DVM across capacitor bank (X57/X58), and one across R3 in the output converter. Note: 1000V	-	OK / Not OK
24.	Set Control System to local mode. Turn on main power. Push the ON button. The CPS should now be ON and enabled. Verify that fans in Output Converter are running	-	OK / Not OK
25.	Set current limiter of the CPS to approx. 100mA. Slowly increase the voltage to 1000V, and verify that the stabilized current doesn't exceed 80mA Note! If the bleeder circuit erroneously activates more than 150mA will be drawn.	< 80mA	51 mA
26.	At 1000V on the capacitor bank, ensure that the midpoint (measured across R3) is:	500V±15V	510 V
27.	Push the OFF button. The CPS should now be OFF and disabled.	-	OK / Not OK
28.	When turned OFF, V_HV must drop from 1000V to below 50V in less than 60s by the bleeder circuit.	< 60s	40 s
29.	Set CPS back to remote mode.		ok

4.6. Charge/Discharge test

Test Step	Description	Accept Criteria	Result
30.	Push the ON button. The CPS should now be ON and enabled.	-	OK / Not OK
31.	Increase ISET and verify that V_HV tracks the setting as follows: ISET = 0A → V_HV: ISET = 34A → V_HV: ISET = 68A → V_HV: ISET = 102A → V_HV: ISET = 136A → V_HV: ISET = 170A → V_HV: ISET = 204A → V_HV: ISET = 238A → V_HV: ISET = 272A → V_HV: ISET = 306A → V_HV: ISET = 340A → V_HV: Note: these are temporary values, changed during test.	 0V ±10V 60V ±10V 120V ±10V 180V ±10V 240V ±12V 300V ±15V 360V ±18V 420V ±21V 480V ±24V 540V ±27V 600V ±30V	 4 V 57 V 116 V 175 V 234 V 293 V 353 V 412 V 470 V 527 V 582 V
32.	Set ISET to 0A and verify that V_HV drops from 600V to below 50V in less than 40s	< 40s	31 s
33.	Adjust TP8.7 close to zero at 34A/340A iteratively POT3/POT5 (offset/gain)	-	OK / Not OK
34.	Turn power supply OFF.	-	OK / Not OK

4.7. Low Current Test

Test Step	Description	Accept Criteria	Result
35.	Connect Raster Scanner Magnet with cable and termination filter to MPS output. Interconnecting cable: 4 x 16mm2 screened cables, two in parallel, each 30-35m long. Note! Cables are connected in "star quad" configuration, and must have the same length within ±0.5m.	30-35m	35 m
36.	For dynamic measurements, insert current transducer on the return lead (in the output converter).	-	OK / Not OK
37.	Connect external trigger generator to fiber optic trigger input, ISO2 "PRE-TRIG".	-	OK / Not OK
38.	Connect oscilloscope with three voltage probes, all referring to negative DC-link in output converter (TP6/TP9/TP10); * Channel 1 on Q1 output (TP5) * Channel 2 on Q2 output (TP8) * Channel 3 on positive DC-link (TP4)	-	OK / Not OK
39.	Connect the magnet current transducer feedback to oscilloscope Channel 4.	-	OK / Not OK
40.	Establish connection to the parameter setup on the DRM, and set the following parameters: * II = 0 (muting the output current loop) * IP = 0 (--||--) * OI = 0 (muting the output offset loop) * OP = 0 (--||--)	-	OK / Not OK
41.	Connect DVM to measure V_HV (X57/X58 or TP7/TP9)	-	OK / Not OK
42.	Turn power supply on at ISET = 68A (20%), and verify that V_HV settles at:	120V ±10V	116 V
43.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
44.	Verify that voltages on Q1 output, Q2 output and DC-link do not exceed the V_HV DVM measurement by +15V or -15V during switching – at any point during the burst (including peaks).	V (pt. 42)+15V -15V	+15 V -15 V

Test Step	Description	Accept Criteria	Result
45.	Inspect the magnet current wave shape and verify the following: Positive Amplitude: Negative Amplitude: Offset (Pos. I_{pk} – Neg. I_{pk})/2: Pulse frequency: Burst duration: Note: Over-shoot of 50% is allowed during the first 500µs of the burst.	 +68A_{pk} ±20A -68A_{pk} ±20A 0A ±2A 40kHz±0.1kHz 4.2ms ±0.1ms	 59 A_{pk} 58 A_{pk} 0.8 A 40.06 kHz 4.24 ms
46.	Based on the amplitude measured above, adjust DRM parameter VFFFA (feed forward factor for output voltage) to achieve ±68Apk±2A magnet current (modify VFFFA as needed and repeat burst).	800-1200	1024
47.	Verify analogue current measurement on regulation module, measure TP5.1/TP5.8; Note: Due to the output cable, power supply output current is distorted after the peaks.	±662mV_{pk} ±20mV	V
48.	Set output current trip-level to 10%, trig a burst and verify over-current interlock.	"DC Overload" interlock	OK / Not OK
49.	Adjust Over Current threshold on DRM to 130% (measure on TP5.5, GND on TP5.8, adjust POT6)	2.218mV±20mV	OK / Not OK
50.	Verify analog voltage measurement on regulation module, measure TP8.9/TP8.12; -1.08V at 120V.	-1.08V ±90mV	-1.06 V
51.	Set output voltage trip-level to minimum level and verify over-voltage interlock (measure on TP8.2, GND on TP8.12, adjust POT2)	-500mV±50mV "PS Fail" interlock	OK / Not OK
52.	Set Over Voltage threshold on DRM back to 750V (measure on TP8.2, GND on TP8.12, adjust POT2)	-4.433V±40mV	OK / Not OK

4.8. High Current Test

Test Step	Description	Accept Criteria	Result
53.	Turn power supply on at ISET = 170A (50%), and verify that V_HV settles at:	0.3*VFFFA±10% (ref: pt. 46)	330 V
54.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
55.	Verify that voltages on Q1 output, Q2 output and DC-link do not exceed the DVM measurement +60V or -60V during switching – at any point during the burst (including peaks).	V (pt. 53) +60V -60V	 +50 V -50 V
56.	Set ISET = 340A (100%), and verify that V_HV settles at:	0.6*VFFFA ±10% (ref: pt. 46)	657 V
57.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
58.	Verify that voltages on Q1 output, Q2 output and DC-link do not exceed the previous DVM measurement at X57/X58 with +100V or -100V during switching – at any point during the burst (including peaks).	V (pt. 56) +100V -100V	 +75 V -75 V
59.	Inspect the magnet current wave shape and verify the following: Positive Amplitude: Negative Amplitude: Offset (Pos. I_{pk} – Neg. I_{pk})/2: Pulse frequency: Burst duration: Note: Over-shoot of 20% is allowed during the first 500µs of the burst.	 +340A_{pk} ±20A -340A_{pk} ±20A 0A ±2A 40kHz±0.1kHz 4.2ms ±0.1ms	 +336 A_{pk} -336 A_{pk} 0 A 40.03 kHz 4.26 ms
60.	Based on the amplitude measured above, fine adjust DRM parameter VFFFA (feed forward factor for output voltage) to achieve ±340Apk±2A magnet current (modify VFFFA as needed and repeat burst).	800-1200	991
61.	SAVE the VFFFA parameter in FPGA.	-	OK / Not OK
62.	Verify analogue current measurement on regulation module, measure TP5.1/TP5.8; Note: Due to the output cable, power supply output current is distorted after the peaks.	~~±3.310V$_{pk}$~~ 3.412 V ±50mV	±3.44 V
63.	During a ±340Apk burst, verify that V_VH does not drop more that 1%.	<1%	3.2 V 0.5 %

4.9. Earth Leak Test

Test Step	Description	Accept Criteria	Result
64.	Turn power supply OFF and connect a 4.7kΩ±10%/≥10W/≥600V low inductance resistor between a positive output terminal and output converter chassis (to simulate a "controlled leak").	-	OK / Not OK
65.	Starting from ISET = 0 and increasing the output current, an earth leakage must be detected (generating an interlock) in the range:	30-50A	37 A
66.	Remove the added resistor.	-	OK / Not OK
67.	Turn power supply OFF and connect a short circuit (≥4mm², ≤30cm) between a positive output terminal and output converter chassis (to simulate a "hard short to ground").	-	OK / Not OK
68.	Set ISET = 34A (10%) and turn power supply ON.	-	OK / Not OK
69.	Apply a single, manual trig, and verify that an earth leakage is detected (generating an interlock).	-	OK / Not OK
70.	Set ISET = 340A (100%) and turn power supply ON.	-	OK / Not OK ✱
71.	Apply a single, manual trig, and verify that an earth leakage is detected (generating an interlock).	-	OK / Not OK ✱
72.	**Remove short circuit between a positive output terminal and output converter chassis after test!**	-	OK / Not OK

✱ PS trips at 60A due to internal balancing resistance

4.10. Frequency Test

Test Step	Description	Accept Criteria	Result
73.	In local control panel, set operating frequency to 20kHz (20000Hz) and verify that V_HV settles at:	0.3*VFFFA ±10% (ref: pt. 60)	350 V
74.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
75.	Inspect the magnet current wave shape and verify the following:		
	Positive Amplitude:	+340A_{pk} ±20A	+342 A_{pk}
	Negative Amplitude:	-340A_{pk} ±20A	-342 A_{pk}
	Offset (Pos. I_{pk} – Neg. I_{pk})/2:	0A ±2A	0 A
	Pulse frequency:	20kHz±0.05kHz	20.08 kHz
	Burst duration:	4.2ms ±0.1ms	4.26 ms
	Note: Over-shoot of 20% is allowed during the first 500µs of the burst.		
76.	In local control panel, set operating frequency to 10kHz (10000Hz) and verify that V_HV settles at:	0.15*VFFFA±10% (ref: pt. 60)	V
77.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
78.	Inspect the magnet current wave shape and verify the following:		
	Positive Amplitude:	+340A_{pk} ±20A	+338 A_{pk}
	Negative Amplitude:	-340A_{pk} ±20A	-338 A_{pk}
	Offset (Pos. I_{pk} – Neg. I_{pk})/2:	0A ±2A	0 A
	Pulse frequency:	10kHz±0.025kHz	10.06 kHz
	Burst duration:	4.2ms ±0.2ms	4.3 ms
	Note: Over-shoot of 20% is allowed during the first 500µs of the burst.		

4.11. Loop Setup and Test

Test Step	Description	Accept Criteria	Result
79.	Establish connection to the parameter setup on the DRM, and set the following parameters: * II = 0.05 (enabling the output current loop) * IP = 0 (--||--) * OI = 300 (enabling the output offset loop) * OP = 0 (--||--) * SAVE the parameters in FPGA.	-	OK / Not OK
80.	Fine adjust DRM parameter INORM (current measurement ADC calibration factor) to achieve ±340Apk±1A magnet current. Calibration is done at 29kHz output current frequency, and current is measured on first peak after 2ms into the burst.	1.100-1.300	1.2019
81.	Changing output current and frequency as follows, verify the loop operation (magnet current settles to within ±2A of the setting in less than 70 bursts): * ISET = 23.5A (6.9%), FSET = 40000kHz * ISET = 340A (100%), FSET = 40000kHz * ISET = 340A (100%), FSET = 10000kHz * ISET = 23.5A (6.9%), FSET = 10000kHz * ISET = 23.5A (6.9%), FSET = 29000kHz * ISET = 340A (100%), FSET = 29000kHz	<±2A in 70 bursts	OK / Not OK OK / Not OK OK / Not OK OK / Not OK OK / Not OK OK / Not OK

4.12. Absolute Accuracy Test

Test Step	Description		Accept Criteria	Result
82.	Measure positive and negative peak-current, and calculate the resulting offset at the below frequencies. Current is measured on first peak after 2ms into the burst.		-	-
83.	10kHz	Positive peak current: Negative peak current: Offset:	-	+343 Apk -341 Apk 1 A
84.	29kHz	Positive peak current: Negative peak current: Offset:	+340A±1% -340A±1% ±3.4A	340 Apk 340 Apk 0 A
85.	40kHz	Positive peak current: Negative peak current: Offset:	+340A±1% -340A±1% ±3.4A	+350 Apk -344 Apk 3 A

Note: Due to cable stored charge, 40kHz peak current is slightly higher than 29kHz peak current.

4.13. Flattop Droop Test

Test Step	Description		Accept Criteria	Result
86.	Measure positive peak-current, and calculate the resulting droop. Current is measured on first positive peak after the specified time into the burst.		-	-
87.	10kHz	500us: 2000us: 4070us: Droop = (first minus last)/first:	- - - -	345 Apk 340 Apk 336 Apk 2.6 %
88.	20kHz	500us: 2000us: 4070us: Droop = (first minus last)/first:	- - - -	339.5 Apk 338 Apk 336.5 Apk 0.9 %
89.	29kHz	500us: 2000us: 4070us: Droop = (first minus last)/first:	- - - 1%	342 Apk 340.5 Apk 339 Apk 0.9 %
90.	40kHz	500us: 2000us: 4070us: Droop = (first minus last)/first:	- - - 1%	347.5 Apk 347.5 Apk 346 Apk 0.4 %

4.14. Full Repetition Rate Test

Test Step	Description	Accept Criteria	Result
91.	Set ISET = 340A (100%), FSET = 40000kHz and turn power supply ON.	-	OK / Not OK
92.	Apply external trigger of 14Hz -0/+0.1Hz	-	OK / Not OK
93.	Verify that the power supply produces bursts at 14Hz (does not skip bursts).	No burst skipping, 5 min.	OK / Not OK
94.	Verify that the power supply maintains regulation.	<±2A, 5 min.	± 2 A
95.	Verify that the CPS is able to maintain V_HV with charging time to within 0.1% of final V_HV in <50ms after a burst.	<0.1% <50ms.	1V from DC in 68 ms
96.	Measure the CPS mains input current: * I(L1)	≤3A_{RMS}	2.69 A_{RMS}
97.	Reduce FSET to 29000kHz	-	OK / Not OK
98.	Verify that the power supply produces bursts at 14Hz (does not skip bursts).	No burst skipping, 5 min.	OK / Not OK
99.	Verify that the power supply maintains regulation.	<±2A, 5 min.	± 2 A
100.	Verify that the CPS is able to maintain V_HV with charging time to within 0.1% of final V_HV in <50ms after a burst.	<0.1% <50ms.	2V from DC in 68 ms
101.	Measure the CPS mains input current: * I(L1)	≤3A_{RMS}	2 A_{RMS}
102.	Reduce FSET to 10000kHz	-	OK / Not OK
103.	Verify that the power supply produces bursts at 14Hz (does not skip bursts).	No burst skipping, 5 min.	OK / Not OK
104.	Verify that the power supply maintains regulation.	<±2A, 5 min.	± 1.5 A
105.	Verify that the CPS is able to maintain V_HV with charging time to within 0.1% of final V_HV in <50ms after a burst.	<0.1% <50ms.	2V from DC in 68 ms
106.	Measure the CPS mains input current: * I(L1)	≤3A_{RMS}	1.6 A_{RMS}

4.15. Waveform/Bandwidth Test

Test Step	Description	Accept Criteria	Result
107.	Set ISET = 340A (100%), FSET = 40000kHz and turn power supply ON.	-	OK / Not OK
108.	Apply external trigger of 14Hz -0/+0.1Hz.	-	OK / Not OK
109.	Verify that the power supply produces bursts at 14Hz.	-	OK / Not OK
110.	Perform an FFT analysis of the **Magnet** current and verify the following frequency content (measured in dB compared to the 1st harmonic (40kHz)). Note that input to the analysis should be limited to "usable pulses"; the first 500us should be omitted, and time after burst end should be omitted.	-	-
111.	120kHz (3rd harmonic)	-19.1 ±1.3dB	-18.5 dB
112.	200kHz (5th harmonic)	-28.0 ±3.0dB	-27.1 dB
113.	280kHz (7th harmonic)	-33.8 ±4.7dB	-32 dB
114.	Attach the recorded FFT plot to this report.	-	OK / Not OK

4.16. Over-Frequency Protection Test

Test Step	Description	Accept Criteria	Result
115.	At ISET = 34A (10%), verify "over-freq. protection": • At 14.1Hz trig: PS must operate as above.	Normal opr.	OK / Not OK
	• At 15Hz trig: PS must skip every 2nd burst, give warning: "Pre-Trig Failure" (ISO16) and activate the STATUS signal (ISO13).	Burst skip + ISO16 off + ISO13 off	OK / Not OK
	• At 14.1Hz trig: PS must operate as above. Trigger pulses (rising edge) must be separated by minimum 70ms. Trigger pulses arriving earlier than 70ms after a previous trigger will be ignored and the "Pre-Trig Fault" (warning) will be issued. The "Pre-Trig Fault" (warning) is latched on the DRM until issuing a reset command (remote/local).	Normal opr., warning latched until reset	OK / Not OK

4.17. Interface Test

4.17.1. Local Control

Test Step	Description	Accept Criteria	Result
116.	Verify the functionality of the Local Control Panel	-	OK / Not OK
117.	Verify that current can be set in Amps from	0 to 340.0A	OK / Not OK
118.	Verify that current is read out in Amps from	0 to 340.0A	OK / Not OK
119.	Verify that voltage is read out in Volts	-	OK / Not OK

4.17.2. Remote Control

Test Step	Description	Accept Criteria	Result
120.	Verify the functionality of the Remote line: • Read status of MPS, generate interlock and read it: STAT? STAT:OPER? STAT:OPER:REG1? STAT:OPER:REG2? STAT:OPER:REG3? • Reset interlock and verify: *RST STAT? • Turn power supply ON/OFF: OUTP:REL? OUTP:REL STB OUTP:REL ON • Set and measure an output current/voltage: CURR? CURR 170 MEAS:CURR? MEAS:VOLT? • Read and write an output frequency setpoint: FREQ? FREQ 29000	-	OK / Not OK
121.	Verify the calibration of the read-back signals: Iout V_HV	 ±1A ±2V	OK / Not OK

4.17.3. Control/Status I/O (potential free hardware I/O)

Test Step	Description	Accept Criteria	Result
122.	ENABLE input (X1.1-2):		
	With main power ON, enable input **closed**:	Bursting	OK / Not OK
	With main power ON, enable input **open**:	Not bursting	OK / Not OK
	With main power ON, enable input **closed**:	Bursting	OK / Not OK
	Note: Power supply will only produce bursts if enable input is shorted. The enable input does not affect the ON/OFF state of the power supply or the CPS, it only enables/disables the trigger.		
123.	MAIN PWR IS ON output (X1.3-4):		
	With main power ON:	Closed(<10Ω)	OK / Not OK
	With main power OFF:	Open (>1MΩ)	OK / Not OK
124.	/INTERLOCK output (X1.5-6):		
	With no interlock (PS interlock free):	Closed(<10Ω)	OK / Not OK
	With any interlock:	Open (>1MΩ)	OK / Not OK

4.17.4. B-dot test

Test Step	Description	Accept Criteria	Result
125.	Measure the B-dot output on control crate front panel with oscilloscope. Note: signal must be 50 Ohm terminated.	±6V (±1V) square waves, <±10Vpk	± ~6V V ± ~9.5 Vpk
126.	Attach a scope plot (first full period) to this report.	-	OK / Not OK

4.17.5. Timing/Control/Status I/O (fiber optic I/O)

Test Step	Description	Accept Criteria	Result
127.	Apply POLARITY control signal (ISO3) via test jig.	-	OK / Not OK
128.	Issue a reset and verify via test jig, that STATUS output is high (ISO13 active) Note: STATUS (low) output is a sum of: * PRE-TRIG fault (latched) * POLARITY signal missing (**non**-latched) Read individual signals via fiber optic output and issue a reset command to reset latch.	STATUS is high	OK / Not OK
129.	Apply 15Hz Pre-trig and verify that:	STATUS is low	OK / Not OK
130.	Apply 14Hz Pre-trig and verify that:	STATUS is low	OK / Not OK
131.	Issue reset command and verify that:	STATUS is high	OK / Not OK
132.	Remove POLARITY control signal and verify that:	STATUS is low	OK / Not OK
133.	Reapply POLARITY control signal and verify that:	STATUS is high	OK / Not OK
134.	With POLARITY signal constant **high**, verify that output bursts start with **positive** voltage/current	Bursts starting **Positive**	OK / Not OK
135.	With POLARITY signal **pulsing** (approx.. 10kHz square wave), verify that output bursts start with **negative** voltage/current	Bursts starting **Negative**	OK / Not OK
136.	**Remove** POLARITY signal, verify that output bursts start with **negative** voltage/current	Bursts starting **Negative**	OK / Not OK
137.	When changing current set point from 34A to 340A (at 40KHz output frequency), verify that TRIG PERMIT (ISO12) goes low and comes back high within 10 sec.	Low->high in <10s	8 s
138.	When changing current set point from 340A to 34A (at 40KHz output frequency), verify that TRIG PERMIT goes low and comes back high within 40 sec.	Low->high in <40s	33 s
139.	Open the ENABLE input (X1.1-2) and verify that TRIG PERMIT is:	Low	OK / Not OK
140.	Close the ENABLE input (X1.1-2) and verify that TRIG PERMIT is:	High	OK / Not OK
141.	Verify that I-READY (ISO14) is high when output current is within ±2% of ISET (burst-by-burst)	-	OK / Not OK

5. LONG TERM STABILITY

5.1. Amplitude Stability

Test Step	Description	Accept Criteria	Result
142.	Record the ~~8h~~ 4h stability at 340A (100%), 40kHz, 14Hz trigger on an oscilloscope (zoom in on the last positive current peak in the burst, set display to infinite persistence). Current is measured with DCCT on the **magnet** end of the cable. 8h stability must be better than:	±0.5%	1.7 % pkpk 100% 1.2% pkpk 99% 0.5% pkpk 90%
143.	Attach the recorded stability trace to this report.	-	OK / Not OK
144.	While still running full current, measure ambient temperature (cooling air intake):	22°C ±5°C	23.3 °C
145.	Measure Output Converter air exhaust 1 (main heatsink):	ΔT≤10K	32.5 °C
146.	Measure Output Converter air exhaust 2 (general cabinet):	ΔT≤10K	28.2 °C
147.	Measure Control Crate air exhaust (general cabinet):	ΔT≤10K	26.2 °C
148.	Measure CPS air exhaust (general cabinet):	ΔT≤10K	26.8 °C
149.	Using a thermal camera; inspect the inside of the Output Converter	All temps. <60°C	60 (68)* °C
150.	Measure V_HV at capacitor bank	-	639 V
151.	Measure output voltage on Output Converter output terminals during burst	-	~600V/~900 V_{pk}
152.	Measure output voltage on magnet terminals during burst	-	~400V/~800 V_{pk}

* R19-26 measures 68°C

5.2. Jitter/timing Stability

Test Step	Description	Accept Criteria	Result
153.	Record the 8h jitter at 340A (100%), 40kHz, 14Hz trigger on an oscilloscope (zoom in on the 2nd last current zero-crossing in the burst, set display to infinite persistence). 8h jitter must be less than:	200ns	164 ns
154.	Attach the recorded stability trace to this report.	-	OK / Not OK

6. AS-BUILT NOTES

6.1. HW Configuration

Module	DF p/n	Ver.	Manuf., Manuf. p/n	Serial Number
Digital Regulation Module	8100093679	B	DF	1700504
Interface Module	8100093707	A	DF	1700426
MOSFET/Bleeder Module	8100093702	C	DF	1700494
Capacitor Module	8100093701	A	DF	1700551
MOSFET Gate driver, Q1	2100070002		CREE/Wolfspeed	
MOSFET Gate driver, Q1	2100070002		CREE/Wolfspeed	
Transducer, DCCT1	8100089165		LEM	1163540049
Charge Power Supply, CPS	1300075001		HiVolt	900299
IPC	1400151808		Beckhoff	2352925-001

6.2. SW Configuration

Module	SW version
IPC, Control SW	
IPC, GUI	
Digital Regulation Module	2017-11-28

6.3. Calibration/setup parameters

Test Step	Description	Accept Criteria	Result
155.	Attach the regulation module DISI config. parameters	-	OK / Not OK
156.	Attach the IPC factory settings recipe	-	OK / Not OK
157.	Attach the IPC calibration recipe	-	OK / Not OK

7. Final Inspection

Test Step	Description	Accept Criteria	Result
158.	Ensure that all the main cables are correctly connected and all screws and bolts are fastened. Add a speed marker point on all checked items.	-	OK / Not OK
159.	Check clamp springs on all relays	-	OK / Not OK
160.	Place Lightning symbols according to drawing	-	OK / Not OK
161.	Place Data label	-	OK / Not OK

7.

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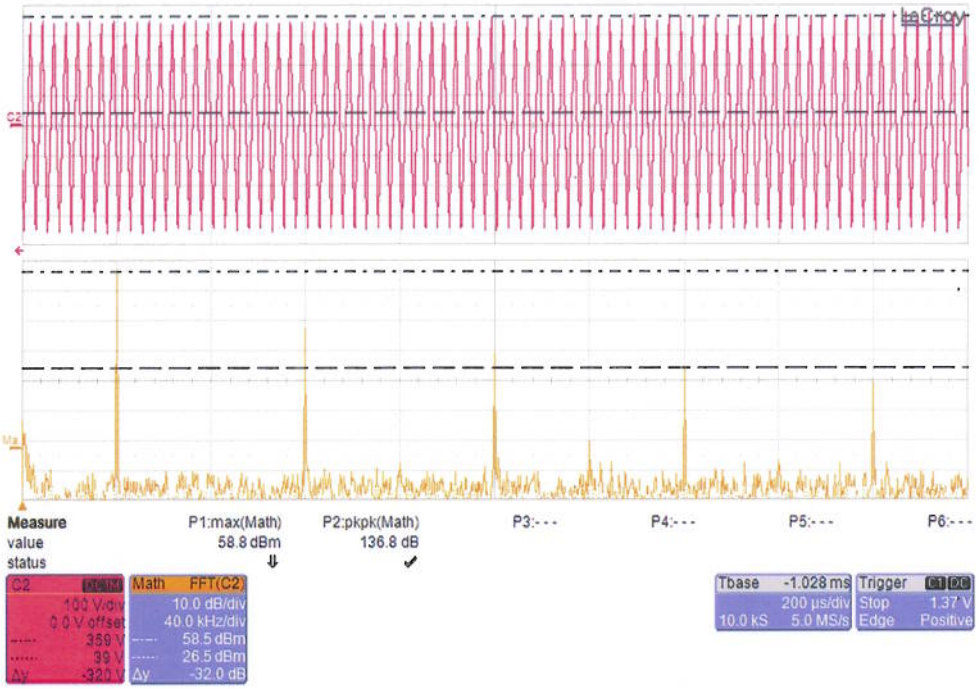
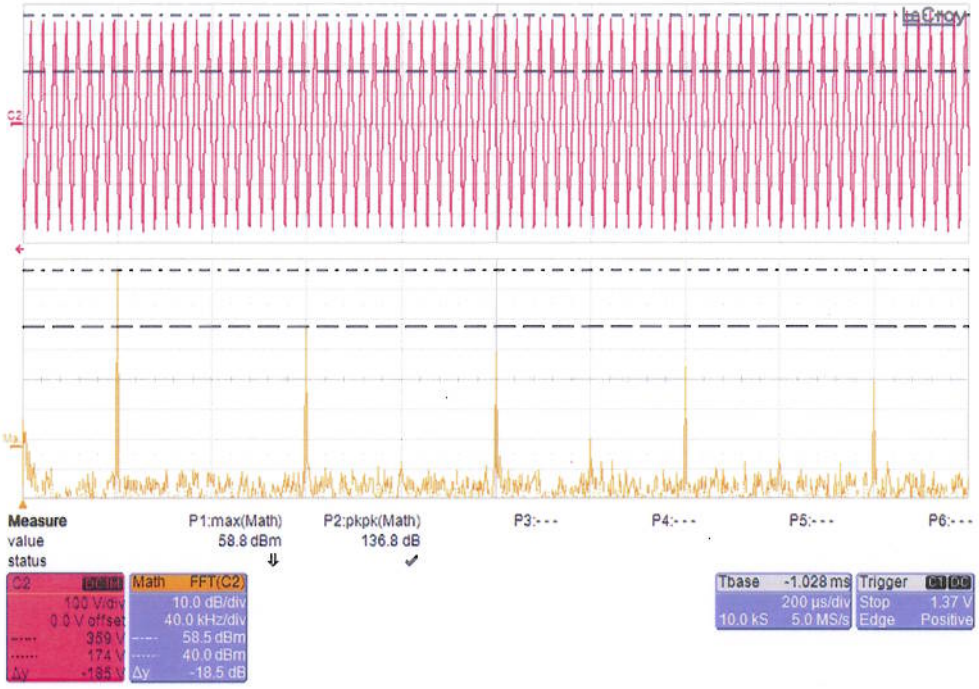
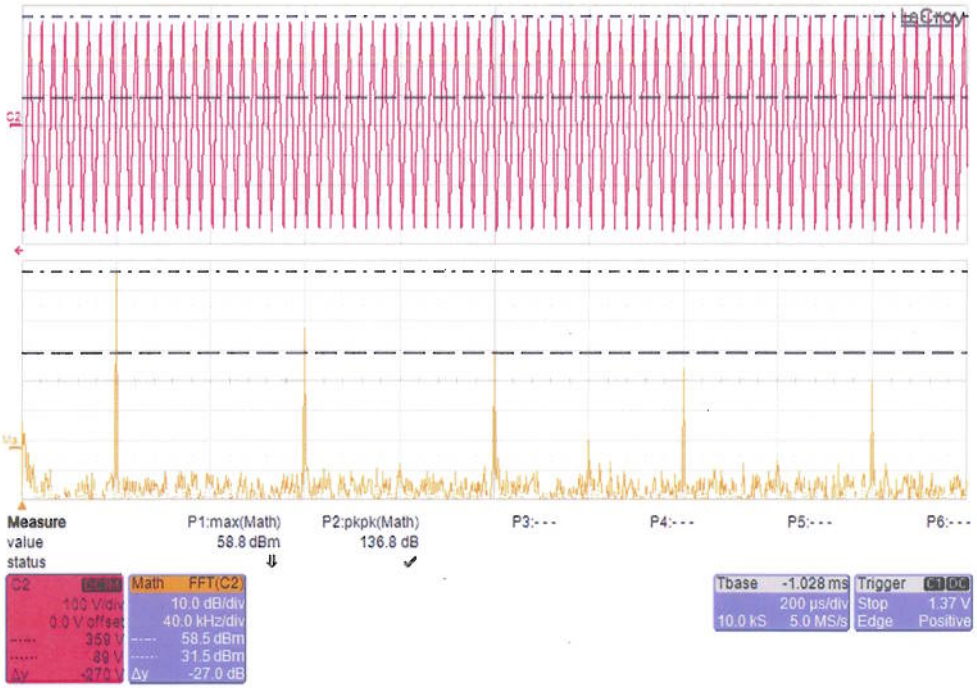
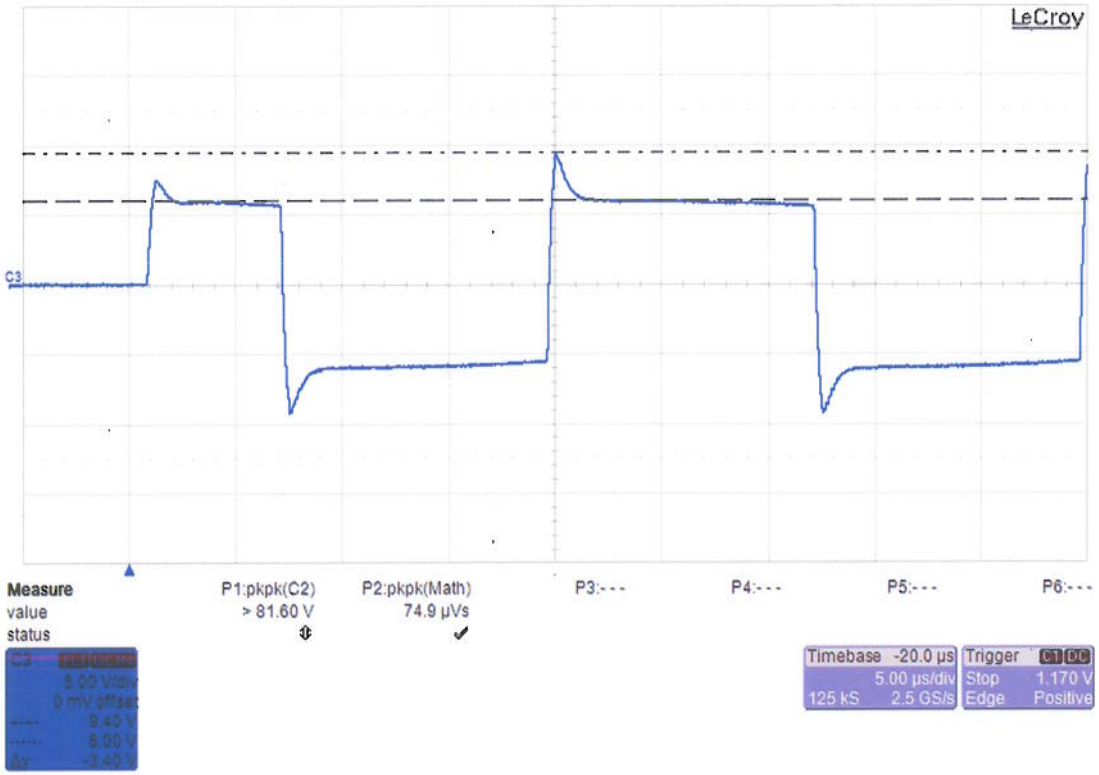
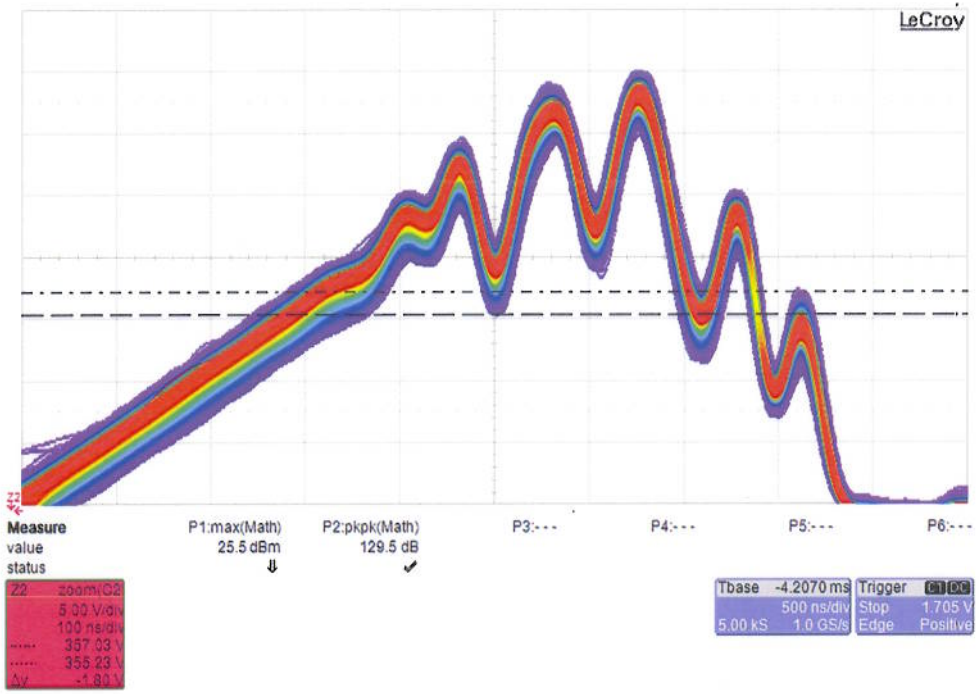
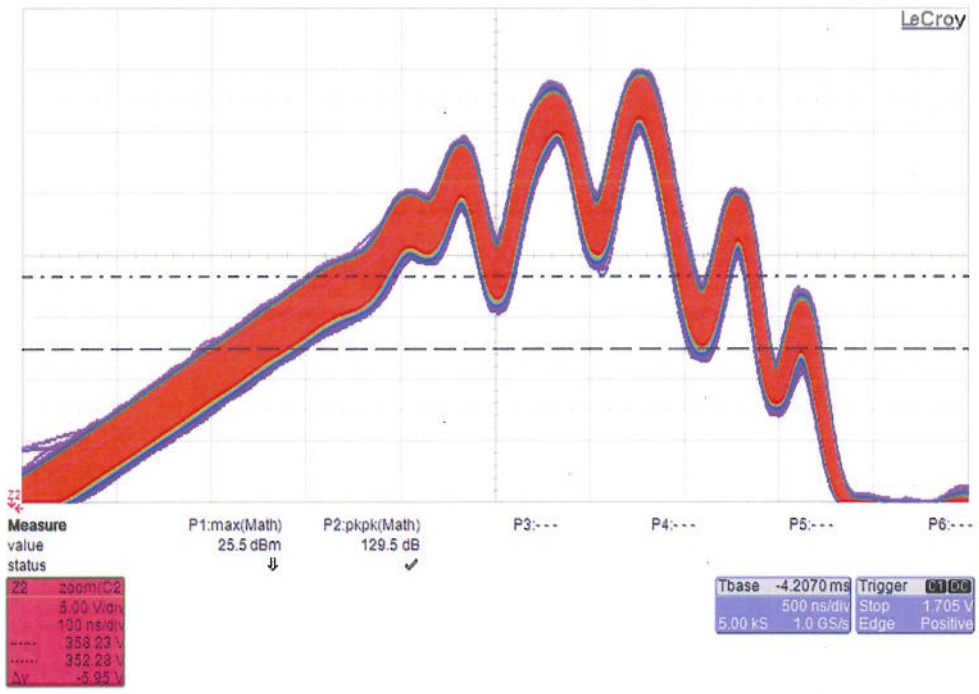

LeCroy
C2
M10
Measure
value
status
P1:max(Math)
58.8 dBm
P2:pkpk(Math)
136.8 dB
P3:---
P4:---
P5:---
P6:---
C2
100 V/div
0.0 V offset
359 V
39 V
Δy -320 V
Math FFT(C2)
10.0 dB/div
40.0 kHz/div
58.5 dBm
26.5 dBm
Δy -32.0 dB
Tbase -1.028 ms
200 µs/div
10.0 kS 5.0 MS/s
Trigger C1 DC
Stop 1.37 V
Edge Positive

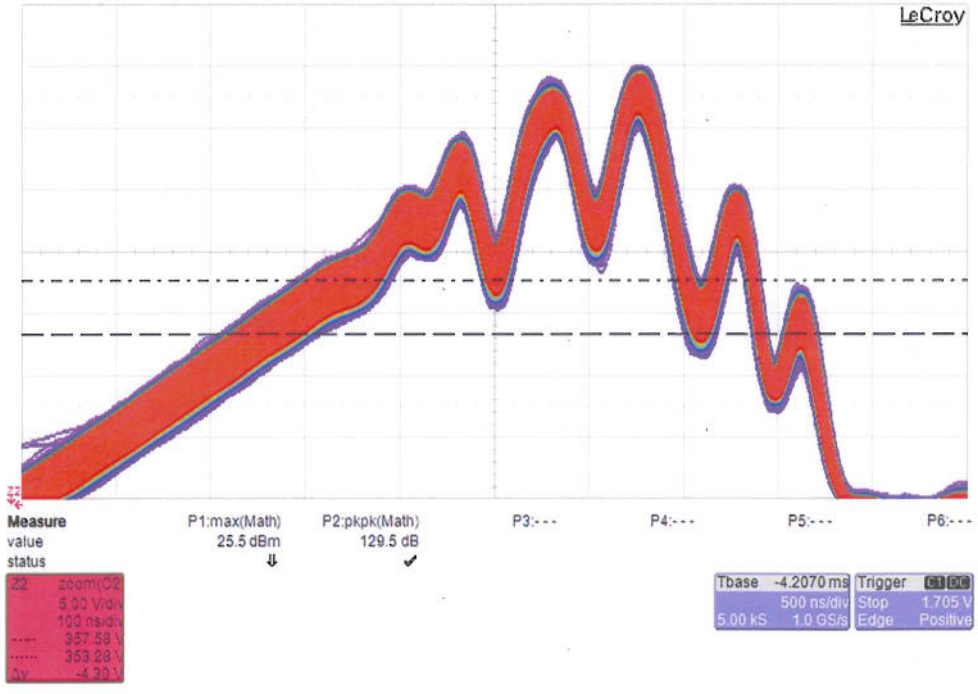

LeCroy
C2
M10
Measure
value
status
P1:max(Math)
58.8 dBm
P2:pkpk(Math)
136.8 dB
P3:---
P4:---
P5:---
P6:---
C2
100 V/div
0.0 V offset
359 V
174 V
Δy -185 V
Math FFT(C2)
10.0 dB/div
40.0 kHz/div
58.5 dBm
40.0 dBm
Δy -18.5 dB
Tbase -1.028 ms
200 µs/div
10.0 kS 5.0 MS/s
Trigger C1 DC
Stop 1.37 V
Edge Positive


LeCroy
C2
M10
Measure
value
status
P1:max(Math)
58.8 dBm
P2:pkpk(Math)
136.8 dB
P3:---
P4:---
P5:---
P6:---
C2
100 V/div
0.0 V offset
359 V
89 V
Δy -270 V
Math FFT(C2)
10.0 dB/div
40.0 kHz/div
58.5 dBm
31.5 dBm
Δy -27.0 dB
Tbase -1.028 ms
200 µs/div
10.0 kS 5.0 MS/s
Trigger C1 DC
Stop 1.37 V
Edge Positive


LeCroy
C3
Measure
value
status
P1:pkpk(C2)
> 81.60 V
P2:pkpk(Math)
74.9 µVs
P3:- - -
P4:- - -
P5:- - -
P6:- - -
Timebase -20.0 µs
5.00 µs/div
125 kS 2.5 GS/s
Trigger C1 DC
Stop 1.170 V
Edge Positive


LeCroy
Measure
value
status
P1:max(Math)
25.5 dBm
P2:pkpk(Math)
129.5 dB
P3:---
P4:---
P5:---
P6:---
Z2 zoom(C2
5.00 V/div
100 ns/div
357.03 V
355.23 V
Δy -1.80 V
Tbase -4.2070 ms
500 ns/div
5.00 kS 1.0 GS/s
Trigger C1 DC
Stop 1.705 V
Edge Positive


LeCroy
Measure
value
status
P1:max(Math)
25.5 dBm
P2:pkpk(Math)
129.5 dB
P3:---
P4:---
P5:---
P6:---
Z2 zoom(C2
5.00 V/div
100 ns/div
358.23 V
352.28 V
Δy -5.95 V
Tbase -4.2070 ms
500 ns/div
5.00 kS 1.0 GS/s
Trigger C1 DC
Stop 1.705 V
Edge Positive


LeCroy
Measure
value
status
P1:max(Math)
25.5 dBm
P2:pkpk(Math)
129.5 dB
P3:---
P4:---
P5:---
P6:---
Z2 zoom(C2
5.00 V/div
100 ns/div
357.58 V
353.28 V
Δy -4.30 V
Tbase -4.2070 ms
500 ns/div
5.00 kS 1.0 GS/s
Trigger C1 DC
Stop 1.705 V
Edge Positive


Tek
Stop
M Pos: 4.213ms
CURSOR
Type
Time
Source
CH2
Δt 164.0ns
1/Δt 6.098MHz
ΔV 15.2mV
Cursor 1
4.21ms
-5.20mV
Cursor 2
4.21ms
10.0mV
CH2 5.00mV
M 100ns
CH1 2.00V
28-Nov-17 13:35
14.0000Hz

No.:	Name:	Read only?	Register content:		
x00	CTRL	- N -	x00000000	Bits	x00000000
x04	STAT	- Y -	x00003130	Bits	x00003130
x08	LLIVE	- Y -	x00000D00	Bits	x00000D00
x09	LFIRST	- Y -	x00000100	Bits	x00000100
x0A	LLATCH	- Y -	x00000D00	Bits	x00000D00
x0C	FREQ	- N -	4000	Uint(12)	x00000FA0
x0D	ISET	- N -	0,1470	Ufix(4.12)	x0000025A
x10	FINIT	- N -	1000	Uint(12)	x000003E8
x12	FMIN	- N -	1000	Uint(12)	x000003E8
x13	FMAX	- N -	4000	Uint(12)	x00000FA0
x14	FSET	- Y -	4000	Uint(12)	x00000FA0
x20	VCMP	- Y -	x0000000C	Bits	x0000000C
x24	VFFA	- N -	991,0000E+0	FloatH	x000063BE
x25	VFFB	- N -	1,6499E-3	FloatH	x000016C2
x26	VFFC	- N -	88,1875E+0	FloatH	x00005583
x28	VDCLM	- Y -	41,8240E+3	FloatH	x0000791B
x29	VPRE	- Y -	6,1480E+3	FloatH	x00006E01
x2C	VREQ	- Y -	6396	Uint(16)	x000018FC
x2D	VMIN	- N -	0	Uint(16)	x00000000
x2E	VMAX	- N -	65535	Uint(16)	x0000FFFF
x2F	VSET	- Y -	6396	Uint(16)	x000018FC
x30	VMONV	- Y -	0,0027	Ufix(4.12)	x0000000B
x34	VMONI	- Y -	0,0027	Ufix(4.12)	x0000000B
x40	IPEAKP	- Y -	0,1477	Ufix(4.12)	x0000025D
x41	IPEAKN	- Y -	0,1475	Ufix(4.12)	x0000025C
x42	IBAVG	- Y -	0,1475	Ufix(4.12)	x0000025C
x43	OMEAS	- Y -	0,0002	Sfix(4.12)	x00000001
x44	INORM	- N -	1,2019	Ufix(1.12)	x0000133B
x50	IERROR	- Y -	-0,0005	Sfix(4.12)	x0000FFFE
x51	IP	- N -	0,0000E+0	FloatH	x00000000
x52	IPUSE	- Y -	0,0000E+0	FloatH	x00000000
x53	II	- N -	49,9878E-3	FloatH	x00002A66
x54	IIUSE	- Y -	2,0900E+3	FloatH	x00006815
x55	IIC	- Y -	0,1187	Sfix(4.12)	x000001E6
x56	IICMAX	- N -	2,0000	Ufix(4.12)	x00002000
x60	OERROR	- Y -	-0,0002	Sfix(4.12)	x0000FFFF
x61	OP	- N -	0,0000E+0	FloatH	x00000000
x62	OPUSE	- Y -	0,0000E+0	FloatH	x00000000
x63	OI	- N -	300,0000E+0	FloatH	x00005CB0
x64	OIUSE	- Y -	75,0122E-3	FloatH	x00002CCD
x65	OIC	- Y -	0,4404	Sfix(4.12)	x0000070C
x66	OICMAX	- N -	1,0000	Ufix(4.12)	x00001000
x67	OSCALE	- N -	30,0000E+0	FloatH	x00004F80
x70	TBR	- N -	68	Uint(12)	x00000044
x71	TBW	- N -	4200	Uint(16)	x00001068
x72	TBRPD	- N -	10	Uint(4)	x0000000A
x73	TDEADBGN	- N -	0	Uint(8)	x00000000
x74	TDEADOTH	- N -	200	Uint(8)	x000000C8
x75	TOVMAX	- N -	150	Uint(8)	x00000096
x76	TOFFADJ	- Y -	0	Sint(12)	x00000000
x78	RDYLIMI	- N -	0,0303	Ufix(0.12)	x0000007C
x79	RDYLIMO	- N -	0,0200	Ufix(0.12)	x00000052

xE0	VFPGA	- Y -	30992	Uint(16)	x00007910
xE1	VPARAM	- N -	1	Uint(16)	x00000001
xEF	NOTEPAD	- N -	0	Uint(16)	x00000000
xF0	DEVC	- N -	x00000000	Bits	x00000000
xF4	DEVV0	- N -	0	Uint(16)	x00000000
xF5	DEVV1	- N -	0	Uint(16)	x00000000
xF8	DEVIBAVG	- N -	0,0000	Ufix(4.12)	x00000000
xF9	DEVOMEAS	- N -	0,0000	Sfix(4.12)	x00000000
xFA	DEVPEAKP	- N -	0,0000	Ufix(4.12)	x00000000
xFB	DEVPEAKN	- N -	0,0000	Ufix(4.12)	x00000000
xFC	DEVDBG0	- Y -	x00000079	Bits	x00000079
xFD	DEVDBG1	- Y -	x00000079	Bits	x00000079
xFE	DEVDBG2	- Y -	x00000079	Bits	x00000079
xFF	DEVDBG3	- Y -	x00000079	Bits	x00000079

```
PersistentData.rConfig_NominalCurrentMax:=340
PersistentData.rConfig_NominalCurrentMin:=-340
PersistentData.rConfig_NominalSlewRate:=433
PersistentData.rConfig_NominalVSlewRate:=100
PersistentData.rTemperatureLimit:=30
PersistentData.rConfig_NominalVoltageMax:=1000
PersistentData.rConfig_NominalVoltageMin:=0
PersistentData.rFlowLimit:=8
PersistentData.bShowCurrentInAmps:=TRUE
PersistentData.bControlMode:=FALSE
PersistentData.eProject:=1
```

```
PersistentData.rVoltageGain:=0.07347
PersistentData.rVoltageOffset:=-2
```