DANFYSIK

Danfysik 2016

Factory Acceptance

Test Procedure

For ESS RSMS-PS

ASSY SERIAL NO. : _____

Factory Acceptance Test Procedure
Part number 8100093---
ESS RSMS-PS

DANFYSIK

Preparation/Review	Signature	Date
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1. Scope

This Test Report covers the calibration procedure and the pre-shipment factory test of the Power Supply.
The objective of the test is to verify that the build standard complies with the agreed specification.

This Test Report is divided into the following sections:

Introduction:	This chapter
Acceptance Data:	Key requirements and notes on the recorded performance.
Functional Test:	Procedures for the initial verification and adjustments.
Full Power Test:	Procedures for the long term, full power tests and regulation verification.
As-built Notes:	Lists all configuration/calibration parameters, setups, serial numbers etc.
Final inspection:	Instructions for final inspection before shipment.

1.1. Applicable Documents

AD1. "Appendix_1"

AU, Technical Specification for the pulsed raster scanning system, March 2016

AD2. Quotation 502446
Danfysik; Purchase of the raster scanning magnets for the ESS project, 20-04-2016

AD3. 502446 PDR Rev-B

DF, Preliminary Design Report 25-11-2016

AD4. 502446 DDR Rev-A

DF, Detailed Design Report, 22-12-2016

AD5. 8200093700.A

RSMS-MPS Main schematic

1.2. Abbreviation used

- **CPS** Charge Power Supply
- **DRM** Digital Regulation Module
- **DF** Danfysik A/S
- **H,W,D** Height, Width, Depth
- **N/A** Not Applicable
- **S/C** Short Circuit(ed)
- **TBD** To Be Defined
- **DUT** Device Under Test
- **RSMS** Raster Scanning Magnet System
- **PSU** Power supply
- **DVM** Digital Voltmeter
- **PT#** Test Point number

1.3. Test environment

Ambient temperature: 25±5°C
Humidity: <90%

2. Preparation,

2.1. Equipment

Equipment Reference	Equipment Manufacture and Model	ID: Comment	Calibration date	Calibration due
A	Multimeter		___ / ___ 20__	___ / ___ 20__
B	PC		___ / ___ 20__	___ / ___ 20__
C	Hi-Pot – Earth Tester		___ / ___ 20__	___ / ___ 20__
D	Oscilloscope		___ / ___ 20__	___ / ___ 20__
E	DCCT IT 400		___ / ___ 20__	___ / ___ 20__

2.2. Pre-setting of the module

Described in the specific test points

3. Acceptance Data

DF Ref.	Parameter	Requirement	Comments	Measured Passed	Remarks See also	Test Eqp. Ref.
1.	**Input**					
1.1.	Main Input Voltage variation	230V_{AC}	+/-10%, 1PH+N+PE		Rem 2	B
1.2.	Input Frequency	50 – 60Hz			Rem 2	
1.3.	Fuse/breaker	TBD A TBD A	Input Converter Control Crate		Rem 2	
1.4.	Cooling	Air				
2.	**Output**					
2.1.	Output Voltage, max	±700Vpk				
2.2.	Output Current	±340Apk				
2.3.	Scanning Burst Duration	3.57 ms.	Useable raster period			
2.4.	Pre scanning settling time	500 µs	Burst prior to usable raster period			
2.5.	Pulse burst repetition rate	up to 14 Hz.	Ext. trigger			
2.6.	Output current shape	Triangle	Load dependent			
2.7.	Synchronization accuracy	<200ns				
2.8.	Operating Range	6.9% to 100%				
2.9.	Operation Frequency	10kHz to 40kHz				
2.10.	Absolute accuracy	1%	Amplitude accuracy			
2.11.	Absolute accuracy Repeatability	1%	First to last pulse in a burst (usable period)			
2.12.	Absolute accuracy Repeatability	1%	Burst to burst			
2.13.	Stability	0.5%	±10% Mains; ±5% Load ±10° C Air; 8 Hours			
2.14.	OFFSET (Symmetry)	<1%	Of full current			
2.15.	Output Earth Connection	Minus DC- Link voltage	Earth connected to minus of the DC Link voltage			
2.16.	Output Voltage, max	±700Vpk				
3.	**Load**					
3.1.	Magnet Load	7.8µH ±10% 9mΩ ±10%	With cable termination filter in parallel			
3.2.	Cable	4 x 16mm2 shielded cables	30m<Length<35m Two cables connected in parallel to reduce cable inductance			

DF Ref.	Parameter	Requirement	Comments	Measured Passed	Remarks See also	Test Eqp. Ref.
4.	**Protection**					
4.1.	Internal Interlocks Turns PSU OFF	Over-Current Over-Voltage Mains failure PS Over Temp. Reg. failure	> 130% > 120% -20% V line > 80° C Missing OK signal from module			
4.2.	External Interlocks Turns PSU OFF	EXT 1 EXT 2 EXT 3				
5.	**Interface**					
5.1.	RS422	Remote				
5.2.	Current setting resolution Digital	16 bit				
5.3.	Pulse freq. setting	12 bit				
5.4.	Output Current Read Back Digital	8 bit plus sign				
5.5.	DC Link Voltage Read Back Digital	8 bit incl. sign				
5.6.	Front Panel Control	Yes				
5.7.	Software Status signals (Locally and Remotely accessible)	PSU ready ON / OFF REM / LOC Aux supply +15V Aux supply +5V Aux supply -15V				
5.8.	Hardware Timing input signals	Sync. Freq. Pre-Trig Polarity				
5.9.	Hardware Timing and status output signals	Trig Permit Beam Run Perm. Status I-Ready				
5.10.	B-DOT	±10 V (±1V)				
5.11.	Remote control protocol	DF Standard.				
6.	**Cooling**					
6.1.	Cooling	Air, ΔT<10°C	Input Converter Output Converter Control Crate			
6.2.	Power dissipation	Load: 6% Cable: 66% PSU: 28%	Approximate figures.			

DF Ref.	Parameter	Requirement	Comments	Measured Passed	Remarks See also	Test Eqp. Ref.
7.	**Mechanical**					
7.1.	Size	19" rack mounted 8U high 650mm. deep				
7.2.	Connection Mains	Rear				
7.3.	Connection Output	Rear				
7.4.	Cabinet colour	RAL 7035				
7.5.	Weight	<20kg <45kg <10kg				
8.	**Mechanical**					
8.1.	Relative Humidity	<90%	Non-condensing			
8.2.	Norms	CE EN-61010-1 IEC 61508	European Safety Safety			

Remarks.

1) Not tested due to power limitation in the test stand. Ensured through design and previous tests at lower power.
2) Ensured through design.
3) Verified under module test.

4. Functional Test

4.1. Pre Inspection

Following test are performed without the power supply connected.

Test Step	Description	Accept Criteria	Result
1.	Check Main cables are tightened.	No visual damage	OK / Not OK
2.	Check protective bonding cables are tightened.	M4: 1.2Nm M5: 2.0Nm M6: 3.0Nm M8: 6.0Nm	OK / Not OK
3.	Check Fuses and ratings: F1 (Control Crate): TBD AT F2 (Control Crate): TBD AT X8 (Control Crate): TBD AT X9 (Output Converter): TBD AT	Correct fuses	OK / Not OK
4.	Visual inspection of crates: • Output Converter. • Control Crate • Connection box (at magnet girder leg)	Cabinets are clean, free from swarf, loose cable cores and other foreign objects.	OK / Not OK

4.2. Insulation Test

Following tests are performed with the power supply disconnected from the mains.

Test Step	Description	Accept Criteria	Result
5.	Short circuit the main power input (phase and neutral line together). Close circuit breaker (Q1) and bypass the main contacts on contactor K2. Short circuit all inputs and outputs on capacitor banks, MOSFET Q1 and Q2 in the output converter to PE. Short circuit power supply output terminals to PE. Short circuit all pins of X1 on the control crate to PE.	-	OK / Not OK
6.	Apply 1400V_{AC} between main power input and PE. Measure current:	No short or spark may occur.	mA_{RMS}
7.	Short circuit the main power input (phase and neutral line together) to PE.		
8.	Apply 350V_{AC} between all pins of X1 on the control crate and PE. Measure current:	No short or spark may occur.	mA_{RMS}
9.	Remove short circuits and re-establish circuits modified under [5].	-	OK / Not OK

4.3. Grounding Continuity Test

Test Step	Description	Accept Criteria	Result
10.	Connect a 10A power supply minus terminal to the output converter grounding point.	-	OK / Not OK
11.	Connect plus terminal to the following externally accessible parts and measure the voltage at the applied 10A: • Capacitor Charge PS cabinet • Capacitor Charge PS top plate • Capacitor Charge PS front plate • Output Converter cabinet • Output Converter top plate • Output Converter front plate • Output Converter mains inlet, PE pin • Control Crate cabinet • Control Crate top plate • Control Crate front plate • Control Crate mains inlet, PE pin • Connection box at magnet girder	< 1V < 1V < 1V < 1V < 1V < 1V < 1V < 1V < 1V < 1V < 1V < 1V < 1V < 1V	V V V V V V V V V V V V V V
12.	Connect plus terminal to the following internal parts and measure the voltage at the applied 10A: • Yoke of T1 in Control Crate • Main heat sink in Output Converter	< 1V < 1V	V V

4.4. Initial Testing and Setup

Test Step	Description	Accept Criteria	Result
 13.	For Safety: Place extra grounding bracket at Capacitor/MOSFET module, X31.	-	OK / Not OK
14.	Turn OFF power for CPS	-	OK / Not OK
15.	Apply MAIN voltage 230V to Control Crate. Measure supply voltage, phase to phase	-	V
16.	Check that fan in Control Crate is running.	-	OK / Not OK
17.	Adjust Over Current threshold on DRM to 120% (measure on TPxxx, GND on TPxxx, adjust POTxxx)	xxxV±xxxmV	OK / Not OK
18.	Adjust Capacitor Bank Over Voltage threshold on DRM to 120% (measure on TPxxx, GND on TPxxx, adjust POTxxx)	xxxV±xxxmV	OK / Not OK
19.	Adjust MOSFET Over Temperature threshold on DRM to 90°C (measure on TPxxx, GND on TPxxx, adjust POTxxx)	xxxV±xxxmV	OK / Not OK

4.5. Interlock Test

Test Step	Description	Accept Criteria	Result
 20.	For Safety: Place extra grounding bracket at Capacitor/MOSFET module, X31.	-	OK / Not OK
21.	"Un-dock" the grounding bracket on Capacitor/MOSFET module, X32. Verify "MPS Over-temp/Grounding Bracket" Interlock in Control panel.	-	OK / Not OK
22.	"Re-dock" grounding bracket and reset interlock.	-	OK / Not OK
23.	Disconnecting one wire at thermal switch TSW1. Verify "MPS Over-temp/Grounding Bracket" Interlock in Control panel.	-	OK / Not OK
24.	Activate External Interlock #1 by opening input X1.7-8. Verify External Interlock in Control panel.	-	OK / Not OK
25.	Activate External Interlock #2 by opening input X1.9-10. Verify External Interlock in Control panel.	-	OK / Not OK
26.	Activate External Interlock #3 by opening input X1.11-12. Verify External Interlock in Control panel.	-	OK / Not OK

4.6. Functional, Internal HV Isolation Test

Test Step	Description	Accept Criteria	Result
 27.	Turn off main power Remove grounding bracket at V_{HV} Set the unpowered CPS voltage knob to minimum level. Set CPS to local mode. Turn on power switch of the CPS. WARNING: From this point onwards the output can be energized up to 1kV!	-	OK / Not OK
28.	Set Control System to local mode. Turn on main power. Push the ON button. The CPS should now be ON and enabled. Verify that fans in Output Converter are running	-	OK / Not OK
29.	Set current limiter of the CPS to approx. 10mA. Disable the over voltage interlock in DRM Slowly increase the voltage to 1000V, and check that the stabilized current doesn't exceed 5mA Note! If the bleeder circuit erroneously activates more than 5mA will be drawn.	< 5mA < 1V	mA V
30.	Push the OFF button. The CPS should now be OFF and disabled.	-	OK / Not OK
31.	When turned OFF, V_HV must drop from 1000V to below 50V in less than 60s by the bleeder circuit.	< 60s	s
32.	Set CPS back to remote mode.		
33.	Adjust Over Voltage threshold on DRM to 750V (measure on TPxxx, GND on TPxxx, adjust POTxxx)	xxxV±xxxmV	OK / Not OK

4.7. Charge/Discharge test

Test Step	Description	Accept Criteria	Result
34.	Push the ON button. The CPS should now be ON and enabled.	-	OK / Not OK
35.	Increase ISET and verify that V_HV tracks the setting as follows: ISET = 0A → V_HV: ISET = 34A → V_HV: ISET = 68A → V_HV: ISET = 102A → V_HV: ISET = 136A → V_HV: ISET = 170A → V_HV: ISET = 204A → V_HV: ISET = 238A → V_HV: ISET = 272A → V_HV: ISET = 306A → V_HV: ISET = 340A → V_HV: Note: these are temporary values, changed during test.	 0V ±10V 60V ±10V 120V ±10V 180V ±10V 240V ±12V 300V ±15V 360V ±18V 420V ±21V 480V ±24V 540V ±27V 600V ±30V	 V V V V V V V V V V V
36.	Set ISET to 0A and verify that V_HV drops from 600V to below 50V in less than 40s	< 40s	s
37.	Turn power supply OFF.	-	OK / Not OK

4.8. Low Current Test

Test Step	Description	Accept Criteria	Result
38.	Connect Raster Scanner Magnet with cable and termination filter to MPS output. Interconnecting cable: 4 x 16mm2 screened cables, two in parallel, each 30-35m long. Note! Cables are connected in "star quad" configuration, and must have the same length within ±0.5m.	30-35m	m
39.	For dynamic measurements, insert an IT-400 transducer on the magnet return lead terminated with a 2R000 burden resistor (high precision). Transfer function is 0.4V@400A (=340mV@340A, 1:1000).	-	OK / Not OK
40.	Setup the regulation module for "Test Mode" with "Manual trig" and "Force to 40kHz".	-	OK / Not OK
41.	Connect oscilloscope with three voltage probes, all referring to negative DC-link in output converter (TP5/TP8); * Channel 1 on Q1 output (TP4) * Channel 2 on Q2 output (TP7) * Channel 3 on positive DC-link (TP3)	-	OK / Not OK
42.	Connect the magnet current transducer feedback to oscilloscope Channel 4.	-	OK / Not OK
43.	Establish connection to the parameter setup on the DRM, and set the following parameters: * II = 0000 (muting the output current loop) * IP = 0000 (--||--)	-	OK / Not OK
44.	Connect DVM to measure V_HV (X31)	-	OK / Not OK
45.	Turn power supply on at ISET = 68A (20%), and verify that V_HV settles at:	120V ±10V	V
46.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
47.	Verify that voltages on Q1 output, Q2 output and DC-link do not exceed the previous DVM measurement at X31 by +5V or -5V during switching – at any point during the burst (including peaks).	V (pt. 45)+ 5V -5V	V V

Test Step	Description	Accept Criteria	Result
48.	Inspect the magnet current wave shape and verify the following: Positive Amplitude: Negative Amplitude: Offset (Pos. I_{pk} – Neg. I_{pk})/2: Pulse frequency: Burst duration: Note: Over-shoot of 50% is allowed during the first 500µs of the burst.	 +68A_{pk} ±20A -68A_{pk} ±20A 0A ±2A 40kHz ±1kHz 4.2ms ±0.1ms	 A_{pk} A_{pk} A kHz ms
49.	Based on the amplitude measured above, adjust DRM parameter VFFF (feed forward factor for output voltage) to achieve ±68Apk±2A magnet current (modify VFFF as needed and repeat burst).	5000-7000	_____
50.	Verify analogue current measurement on regulation module, measure TPxxx/TPxxx (TBD); ±2V_{pk} at ±68A_{pk}. Note: DCCT on magnet end of cable measures magnet current. Due to the cable length, magnet peak current is ~3% higher than power supply output current, and power supply output current is distorted after the peaks.	±2V_{pk} ±20mV	V
51.	Set output current trip-level to 10%, trig a burst and verify over-current interlock.	"DC Overload" interlock	OK / Not OK
52.	Set output current trip-level back to 130%.	-	OK / Not OK
53.	Verify analog voltage measurement on regulation module, measure TPxxx/TPxxx (TBD); 1.2V at 120V.	1.2V ±12mV	V
54.	Set output voltage trip-level to 10% and verify over-voltage interlock.	"DC Overload" interlock	OK / Not OK
55.	Set output voltage trip-level back to 120%.	-	OK / Not OK

4.9. High Current Test

Test Step	Description	Accept Criteria	Result
56.	Turn power supply on at ISET = 170A (50%), and verify that V_HV settles at:	.05*VFFF±5% (ref: pt. 49)	V
57.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
58.	Verify that voltages on Q1 output, Q2 output and DC-link do not exceed the DVM measurement +10V or -10V during switching – at any point during the burst (including peaks).	V (pt. 56) +10V -10V	 V V
59.	Set ISET = 340A (100%), and verify that V_HV settles at:	0.1*VFFF ±5% (ref: pt. 49)	V
60.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
61.	Verify that voltages on Q1 output, Q2 output and DC-link do not exceed the previous DVM measurement at X31 with +25V or -25V during switching – at any point during the burst (including peaks).	V (pt. 59) +25V -25V	 V V
62.	Inspect the magnet current wave shape and verify the following: Positive Amplitude: Negative Amplitude: Offset (Pos. I_{pk} – Neg. I_{pk})/2: Pulse frequency: Burst duration: Note: Over-shoot of 20% is allowed during the first 500µs of the burst.	 +340A_{pk} ±20A -340A_{pk} ±20A 0A ±2A 40kHz ±1kHz 4.2ms ±0.1ms	 A_{pk} A_{pk} A kHz ms
63.	Based on the amplitude measured above, fine adjust DRM parameter VFFF (feed forward factor for output voltage) to achieve ±340Apk±2A magnet current (modify VFFF as needed and repeat burst).	5000-7000	_____
64.	SAVE the VFFF parameter in FPGA.	-	OK / Not OK
65.	Verify analogue current measurement on regulation module, measure TPxxx/TPxxx (TBD); ±10V_{pk} at ±340A_{pk}. Note: DCCT on magnet end of cable measures magnet current. Due to the cable length, magnet peak current is ~3% higher than power supply output current.	±10V_{pk} ±20mV	V
66.	During a ±340Apk burst, verify that V_VH does not drop more that 1%.	<1%	V %

4.10. Earth Leak Test

Test Step	Description	Accept Criteria	Result
67.	Turn power supply OFF and connect a 10kΩ±10%/≥10W/≥600V low inductance resistor between a positive output terminal and output converter chassis (to simulate a "controlled leak").	-	OK / Not OK
68.	Stating from ISET = 0 and increasing the output current, an earth leakage must be detected (generating an interlock) in the range:	160A->340A	A
69.	Remove the added resistor.	-	OK / Not OK
70.	Turn power supply OFF and connect a short circuit (≥4mm^2, ≤30cm) between a positive output terminal and output converter chassis (to simulate a "hard short to ground").	-	OK / Not OK
71.	Set ISET = 34A (10%) and turn power supply ON.	-	OK / Not OK
72.	Apply a single, manual trig, and verify that an earth leakage is detected (generating an interlock).	-	OK / Not OK
73.	Set ISET = 340A (100%) and turn power supply ON.	-	OK / Not OK
74.	Apply a single, manual trig, and verify that an earth leakage is detected (generating an interlock).	-	OK / Not OK

4.11. Frequency Test

Test Step	Description	Accept Criteria	Result
75.	Remove 40kHz. jumper on DRM to allow adjustable frequency setting.	-	OK / Not OK
76.	In local control panel, set operating frequency to 20kHz (20000Hz) and verify that V_HV settles at:	.05*VFFF ±5% (ref: pt. 63)	V
77.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
78.	Inspect the magnet current wave shape and verify the following: Positive Amplitude: Negative Amplitude: Offset (Pos. I_{pk} – Neg. I_{pk})/2: Pulse frequency: Burst duration: Note: Over-shoot of 20% is allowed during the first 500µs of the burst.	 +340A_{pk} ±20A -340A_{pk} ±20A 0A ±2A 20kHz ±0.5kHz 4.2ms ±0.1ms	 A_{pk} A_{pk} A kHz ms
79.	In local control panel, set operating frequency to 10kHz (10000Hz) and verify that V_HV settles at:	.025*VFFF ±5% (ref: pt. 63)	V
80.	Apply a single, manual trig, and verify that the power supply produces a raster burst.	-	OK / Not OK
81.	Inspect the magnet current wave shape and verify the following: Positive Amplitude: Negative Amplitude: Offset (Pos. I_{pk} – Neg. I_{pk})/2: Pulse frequency: Burst duration: Note: Over-shoot of 20% is allowed during the first 500µs of the burst.	 +340A_{pk} ±20A -340A_{pk} ±20A 0A ±2A 10kHz±0.25kHz 4.2ms ±0.2ms	 A_{pk} A_{pk} A kHz ms

4.12. Loop Setup and Test

Test Step	Description	Accept Criteria	Result
82.	Establish connection to the parameter setup on the DRM, and set the following parameters: * II = TBD (enabling the output current loop) * IP = TBD (--||--) * SAVE the parameters in FPGA.	-	OK / Not OK
83.	Changing output current and frequency as follows, verify the loop operation (magnet current settles to within ±2A of the setting in less than TBD bursts): * ISET = 23.5A (6.9%), FSET = 40000kHz * ISET = 340A (100%), FSET = 40000kHz * ISET = 340A (100%), FSET = 10000kHz * ISET = 23.5A (6.9%), FSET = 10000kHz * ISET = 23.5A (6.9%), FSET = 29000kHz * ISET = 340A (100%), FSET = 29000kHz	<±2A in TBD bursts	OK / Not OK OK / Not OK OK / Not OK OK / Not OK OK / Not OK OK / Not OK

4.13. Full Repetition Rate Test

Test Step	Description	Accept Criteria	Result
84.	Set ISET = 340A (100%), FSET = 40000kHz and turn power supply ON.	-	OK / Not OK
85.	Apply external trigger of 14Hz -0/+0.1Hz	-	OK / Not OK
86.	Verify that the power supply produces bursts at 14Hz (does not skip bursts).	No burst skipping, 5 min.	OK / Not OK
87.	Verify that the power supply maintains regulation.	<±2A, 5 min.	A
88.	Verify that the CPS is able to maintain V_HV with charging time to within 0.1% of final V_HV in <50ms after a burst.	<0.1% <50ms.	ms
89.	Measure the CPS mains input current: * I(L1)	≤3A_{RMS}	A_{RMS}
90.	Reduce FSET to 29000kHz	-	OK / Not OK
91.	Verify that the power supply produces bursts at 14Hz (does not skip bursts).	No burst skipping, 5 min.	OK / Not OK
92.	Verify that the power supply maintains regulation.	<±2A, 5 min.	A
93.	Verify that the CPS is able to maintain V_HV with charging time to within 0.1% of final V_HV in <50ms after a burst.	<0.1%<50ms.	ms
94.	Measure the CPS mains input current: * I(L1)	≤3A_{RMS}	A_{RMS}
95.	Reduce FSET to 29000kHz	-	OK / Not OK
96.	Verify that the power supply produces bursts at 14Hz (does not skip bursts).	No burst skipping, 5 min.	OK / Not OK
97.	Verify that the power supply maintains regulation.	<±2A, 5 min.	A
98.	Verify that the CPS is able to maintain V_HV with charging time to within 0.1% of final V_HV in <50ms after a burst.	<0.1%<50ms.	ms
99.	Measure the CPS mains input current: * I(L1)	≤3A_{RMS}	A_{RMS}

4.14. Over-Frequency Protection Test

Test Step	Description	Accept Criteria	Result
100.	At ISET = 34A (10%), verify "over-frequency protection": • At 14.1Hz trig: PS must operate as above. • At 15Hz trig: PS must skip every 2nd burst and give warning: "Pre-Trig Fault" (local control panel) and S3 bit 5. • At 14.1Hz trig: PS must operate as above. Trigger pulses (rising edge) must be separated by minimum 70ms. Trigger pulses arriving earlier than 70ms after a previous trigger will be ignored and the "Pre-Trig Fault" (warning) will be issued. The "Pre-Trig Fault" (warning) is latched on the DRM until issuing an N1 command (remote line).	Normal opr. Burst skipping + warning Normal opr., warning latched until reset (N1)	OK / Not OK OK / Not OK OK / Not OK

4.15. Interface Test

4.15.1. Local Control

Test Step	Description	Accept Criteria	Result
101.	Verify the functionality of the Local Control Panel	-	OK / Not OK
102.	Verify that current can be set in Amps from	0 to 340.0A	OK / Not OK
103.	Verify that current is read out in Amps from	0 to 340.0A	OK / Not OK
104.	Verify that voltage is read out in Volts from	0 to 999V	OK / Not OK

4.15.2. Remote Control (Serial Line)

Test Step	Description	Accept Criteria	Result
105.	Verify the functionality of the Remote line: * Turn main power ON/OFF, read S1…	-	OK / Not OK
106.	Verify and calibrate the read-back signals: Iout (AD0) V_HV (AD2)	-	OK / Not OK

4.15.3. Control/Status I/O (potential free hardware I/O)

Test Step	Description	Accept Criteria	Result
107.	ENABLE input (X1.1-2): With main power ON, enable input **closed**: With main power ON, enable input **open**: With main power ON, enable input **closed**: Note: Power supply will only produce bursts if enable input is shorted. The enable input does not affect the ON/OFF state of the power supply or the CPS, it only enables/disables the trigger.	 Bursting Not bursting Bursting	 OK / Not OK OK / Not OK OK / Not OK
108.	MAIN PWR IS ON output (X1.3-4): With main power ON: With main power OFF:	 Closed(<10Ω) Open (>1MΩ)	 OK / Not OK OK / Not OK
109.	/INTERLOCK output (X1.5-6): With no interlock (PS interlock free): With any interlock:	 Closed(<10Ω) Open (>1MΩ)	 OK / Not OK OK / Not OK

4.15.4. Timing/Control/Status I/O (fiber optic I/O)

Test Step	Description	Accept Criteria	Result
110.	Apply external 88MHz SYNC CLK (ISO1) and POLARITY control signal (ISO3) via test jig.	-	OK / Not OK
111.	Issue N1 command and verify via test jig, that STATUS output is high (ISO13 active) Note: STATUS (low) output is a latched sum of: * PRE-TRIG fault (S3 bit 5) * SYNC CLK missing (S3 bit 6) * POLARITY signal missing (S3 bit 7) Read individual signals via S3 command and issue command N1 to reset latch.	STATUS is high	OK / Not OK
112.	Apply 15Hz Pre-trig and verify that:	STATUS is low S3 bit 5 is high	OK / Not OK
113.	Apply 14Hz Pre-trig and verify that:	STATUS is low S3 bit 5 is high	OK / Not OK
114.	Issue N1 command and verify that:	STATUS is high S3 bit 5 is low	OK / Not OK
115.	Remove external SYNC CLK and verify that:	STATUS is low S3 bit 6 is high	OK / Not OK
116.	Reapply external SYNC CLK and verify that:	STATUS is low S3 bit 6 is high	OK / Not OK
117.	Issue N1 command and verify that:	STATUS is high S3 bit 6 is low	OK / Not OK
118.	Remove POLARITY control signal and verify that:	STATUS is low S3 bit 7 is high	OK / Not OK
119.	Reapply POLARITY control signal and verify that:	STATUS is low S3 bit 7 is high	OK / Not OK
120.	Issue N1 command and verify that:	STATUS is high S3 bit 7 is low	OK / Not OK
121.	With POLARITY signal constant **high**, verify that output bursts start with **positive** voltage/current	Bursts starting **Positive**	OK / Not OK
122.	With POLARITY signal **pulsing** (approx.. 10kHz square wave), verify that output bursts start with **negative** voltage/current	Bursts starting **Negative**	OK / Not OK
123.	**Remove** POLARITY signal, verify that output bursts start with **positive** voltage/current	Bursts starting **Positive**	OK / Not OK

Test Step	Description	Accept Criteria	Result
124.	When changing current set point from 34A to 340A, verify that TRIG PERMIT (ISO12) goes low and comes back high within 10 sec.	Low->high in <10s	s
125.	When changing current set point from 340A to 34A, verify that TRIG PERMIT goes low and comes back high within 40 sec.	Low->high in <40s	s
126.	Open the ENABLE input (X1.1-2) and verify that TRIG PERMIT is:	Low	OK / Not OK
127.	Close the ENABLE input (X1.1-2) and verify that TRIG PERMIT is:	High	OK / Not OK
128.	Verify that I-READY (ISO14) is high when output current is within ±2% of ISET (burst-by-burst)	-	OK / Not OK

5. LONG TERM STABILITY

5.1. Amplitude Stability

Test Step	Description	Accept Criteria	Result
129.	Record the 8h stability at 340A (100%), 40kHz, 14Hz trigger on an oscilloscope (zoom in on the last positive current peak in the burst, set display to infinite persistence). 8h stability must be better than:	±0.5%	%
130.	Attach the recorded stability trace to this report.	-	OK / Not OK
131.	While still running full current, measure ambient temperature (cooling air intake):	22°C ±5°C	°C
132.	Measure Output Converter air exhaust 1 (main heatsink):	ΔT≤10K	K
133.	Measure Output Converter air exhaust 2 (general cabinet):	ΔT≤10K	K
134.	Measure Control Crate air exhaust (general cabinet):	ΔT≤10K	K
135.	Measure CPS air exhaust (general cabinet):	ΔT≤10K	K
136.	Using a thermal camera; inspect the inside of the Output Converter	All temps. <60°C	°C
137.	Measure V_HV at capacitor bank	-	V
138.	Measure output voltage on Output Converter output terminals during burst	-	V_{pk}
139.	Measure output voltage on magnet terminals during burst	-	V_{pk}

5.2. Jitter/timing Stability

Test Step	Description	Accept Criteria	Result
140.	Record the 8h jitter at 340A (100%), 40kHz, 14Hz trigger on an oscilloscope (zoom in on the 2nd last current zero-crossing in the burst, set display to infinite persistence). 8h jitter must be less than:	200ns	ns
141.	Attach the recorded stability trace to this report.	-	OK / Not OK

6. AS-BUILT NOTES

6.1. HW Configuration

Module	DF p/n, Ver.	Manuf., Manuf. p/n, Ver.	Serial Number
8500 Control Module	8100083852	DF	
Digital Regulation Module	8100093xxx	DF	
M-panel	8100092459	DF	
Interface Module	8100093xxx	DF	
AUX Power Supply	8100081760	DF	
MOSFET PCB Module	8100093702	DF	
Capacitor Module	8100093701	DF	
MOSFET Gate driver, Q1	2100070002	CREE/Wolfspeed	
MOSFET Gate driver, Q1	2100070002	CREE/Wolfspeed	
Transducer, DCCT1	8100089165	LEM	
Charge Power Supply, CPS	1300075001	HiVolt	

6.2. SW Configuration

Module	SW version
8500 Control Module	
Digital Regulation Module	

6.3. Setup and Calibration, 8500 Control Module

Category	Parameter	Calibration / Value	N/A
Serial number			
Software number			
AD scaling/calibration	AD0		
	AD2		
UART	Remote		
	Local		
Address	Remote		
	Local		
Serial line			
Cold boot			
Auxiliary			
ON pulse			
Interlock			
DA			
AUX2			

6.4. Setup and Calibration, 8500 Control Module

Category	Parameter	Calibration / Value	N/A
TBD			

7. Final Inspection

Test Step	Description	Accept Criteria	Result
142.	Ensure that all the main cables are correctly connected and all screws and bolts are fastened. Add a speed marker point on all checked items.	-	OK / Not OK
143.	Check clamp springs on all relays	-	OK / Not OK
144.	Place Lightning symbols according to drawing	-	OK / Not OK
145.	Place Data label	-	OK / Not OK