DANFYSIK

Danfysik 2016

Regulation Module

ESS raster system

DDR Regulation Module
Rev A
DF project no: 502446

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Revision History Log:

Date:	Rev.:	Init:	Changes:
2016-08-20	A	PAE	Initial version

Reference Documents

Abstract

This document contains the description of the regulation module to be used for the RSMS-PS

Content

1. Introduction

This document contains the description for the detailed design of the regulation module to be used for the RSMS-PS.

2. Functional Description

To control the output converter and ensure that the output current stays within the specification the regulation module performs tasks:

- Receive a current set-point from the control-system
- Receive an operating frequency setting from the control system
- Preset and regulate the DC-Link voltage to achieve the right triangle current amplitude (burst-to-burst "slow" regulation)
- Capacitor bank Bleeder control (for discharging the capacitor bank)
- Offset current control (pulse-to-pulse "fast" regulation)
- Timing control including start polarity control
- H-Bridge control (MOSFET ON/OFF)
- Current Read back
- Voltage read back (= DC Link Voltage)
- Interlock supervision including minimum-time-hold for transient overload conditions
- Test mode timing control

The timing and regulation functions are attained using an FPGA (managing the digital loop and digital controls) with various supporting sub circuits (AD/DA converters, peak detectors and S/H circuits).

See also the block schematic in Figure 1

The heart of the regulation module is an FPGA, that in short works as follows:

When the MPS is turned ON, a DC-Link voltage set-point is calculated based on the output current set-point and the operating frequency setting (higher current or higher frequency -> higher voltage).
When the calculated DC-Link value (voltage across the capacitor bank) is obtained, pulsing is enabled (but not started) by setting the "Trig Permit" signal. When receiving a "Pre-Trig", the regulation module starts pulsing by issuing gate signals to the H-Bridge for a duration of 4.2ms (settable burst duration). After a given number of pulses, a "Beam Run Permit" signal is issued.

Two regulation loops are to be implemented in the FPGA for controlling the triangular output current wave shape. These are:

- A "fast loop" controlling the offset (symmetry), and
- a "slow loop" controlling the current peak value (amplitude)

Both loops make use of feedback from output current measurements, which are peak-detected and sampled by AD converters on the regulation module (positive and negative peak measurements).

Fast loop:
The positive and negative peak values are measured and compared once every pulse cycle by the FPGA to detect and eliminate any offset occurring in the output current. Based on the measured current offset, a timing skew is applied to the H-Bridge control signals thereby manipulating the overall volt-seconds to become zero. This correction is performed every cycle of the triangular output current pulse.

Slow loop:
For each burst, the FPGA measures the average peak to peak current (amplitude) by averaging the measured positive and negative peak measurements throughout the burst. After the burst, this averaged output current peak to peak value (divided by two) is compared with the output current set value and passed to the "I" Controller loop. This "slow" loop is executed only once pr. burst (immediately after the burst) and modifies the predicted DC-Link voltage so that the next burst will be closer to the I-set value.

Note!

- The sampled measured p-p current signals are filtered with a running average filter.

A block schematic of the regulation module is shown in Figure 1 on the next page

Note: The purple boxes are functions intended to be managed by the FPGA.

2.1. Block Schematic

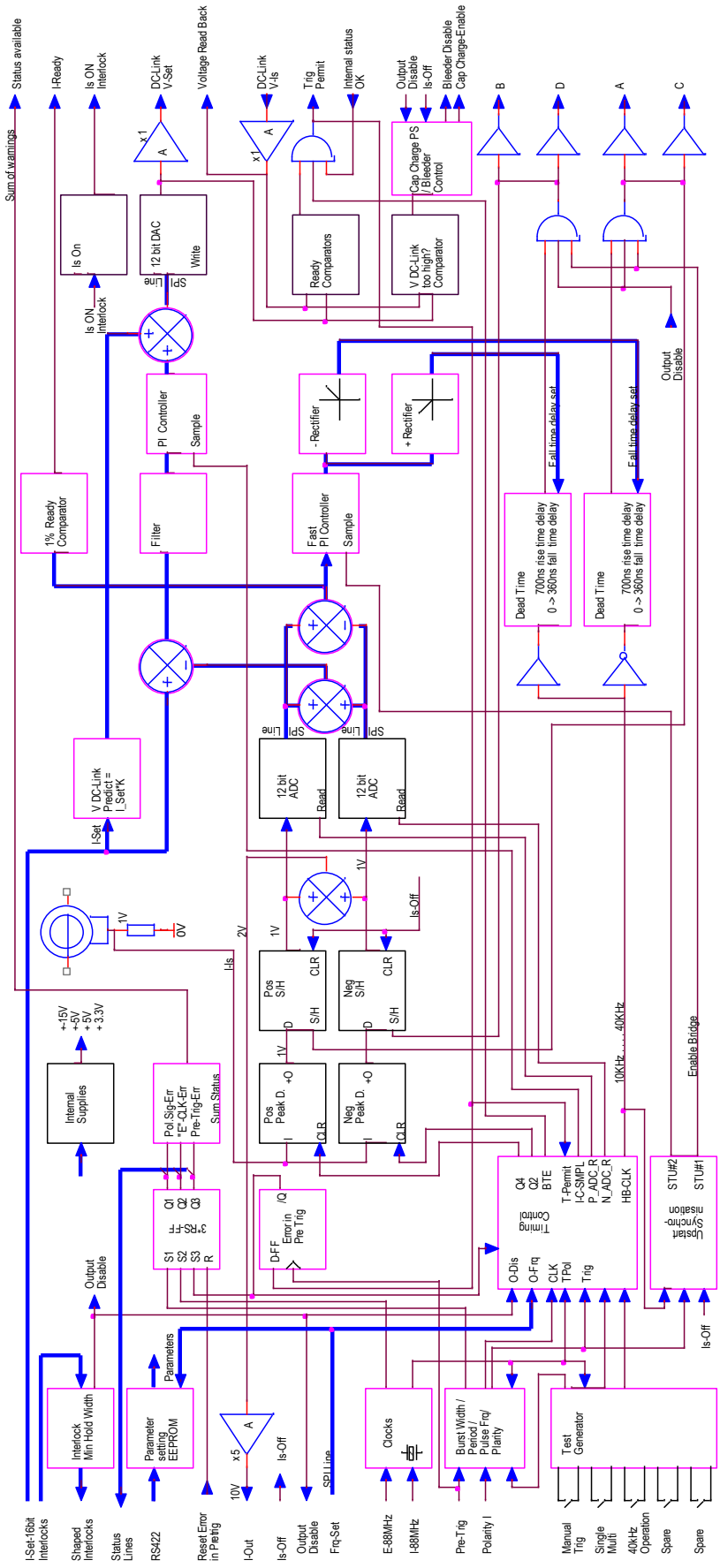


Figure 1

STU#1 = Active signal from synchronized Pre-Trig signal delayed a quarter of a pulse width until last pulse issued at zero output current. This to ensure proper start and ending at zero output current thereby having no start or ending offsets

STU#2 = Active signal after two positive and two negative current peaks and ends at the same time as the burst. When active it enables the offset regulation. The delay is equal to 2*1/f

2.2. Functional Flow Chart

The tasks the FPGA has to perform, and thereby also the main functionality of the regulation module, are given by the flow chart below:

Note: The flow chart is not to be seen as full definition of tasks but more as an illustration of the task constrains together with the block schematic in Figure 1

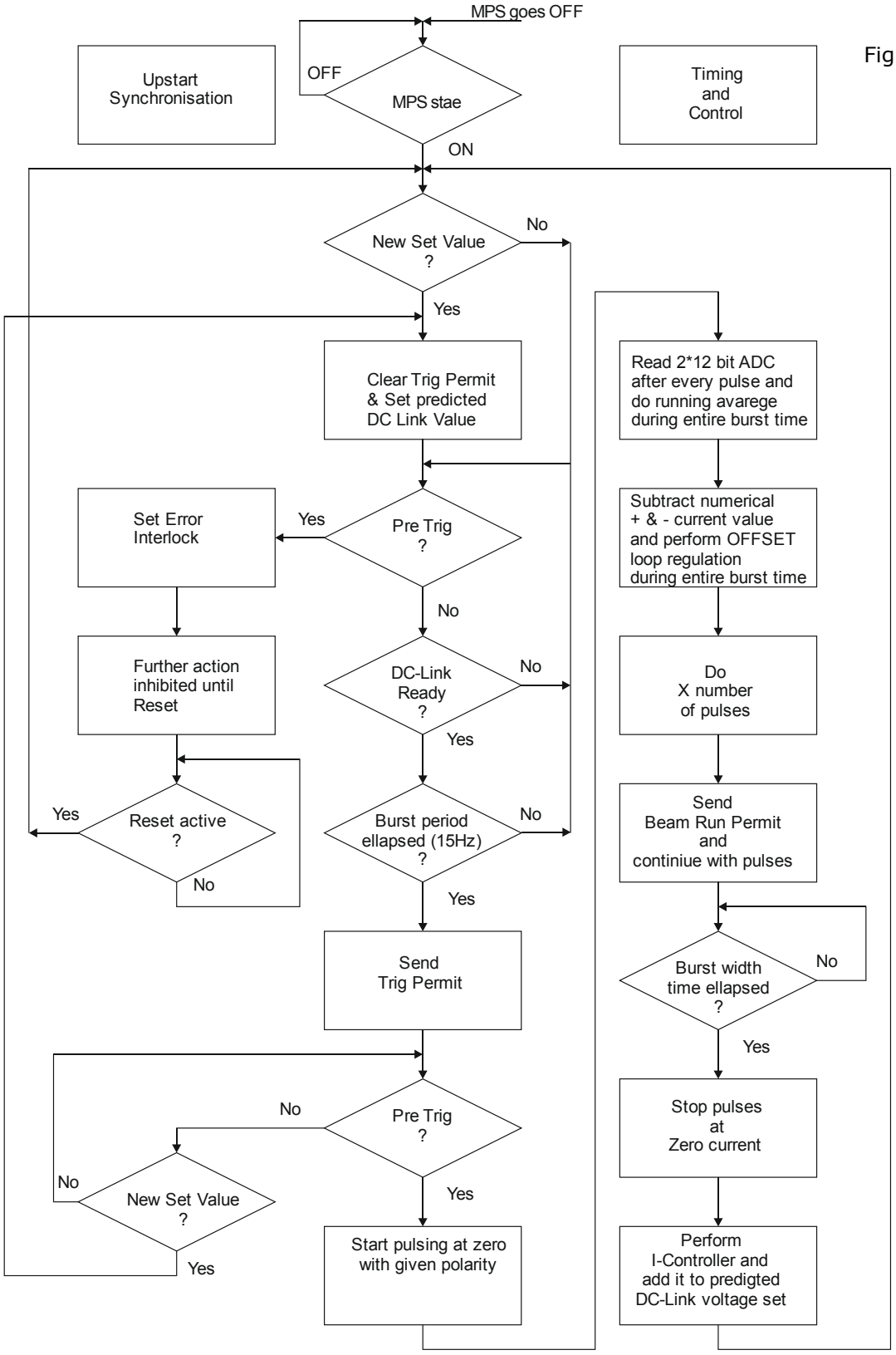


Figure 2

2.3. Simulation

A Simulation circuit of the total power supply is shown in Figure 10 indicating the working principle of the total RSMS.

Below sub chapters shows some interesting simulation results displaying the well working of the RSMS.

2.3.1. One burst

The simulation traces below show one burst.

Top trace: Output current
Middle trace: DC link voltage (Capacitor storage voltage)
Lower trace: Input converter output current. (set to 1A so end of charging can be seen within the 50ms trace time)

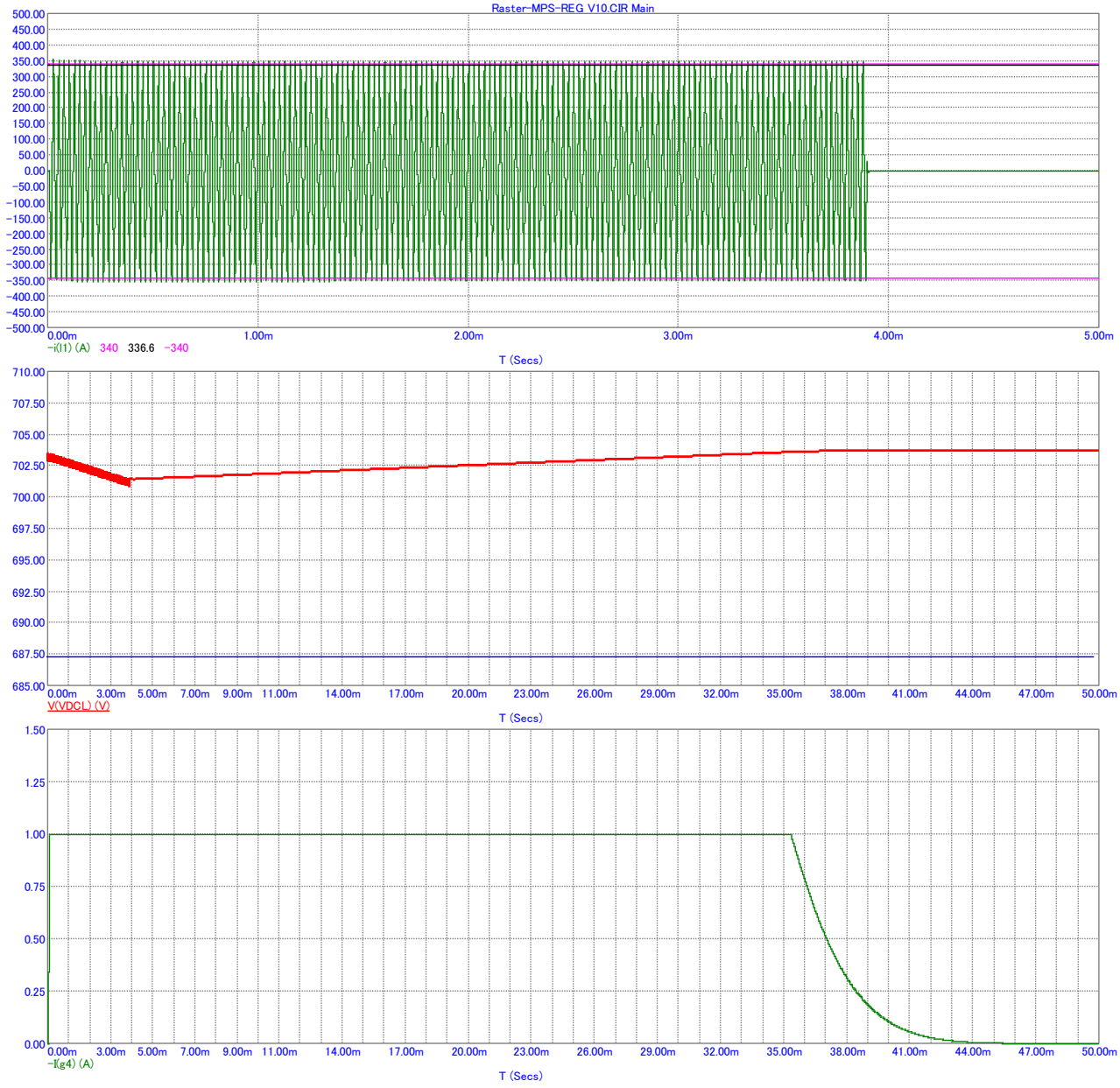


Figure 3

From the trace in Figure 3 it is to be seen that:

- The output current is stable within the specification
- The DC-Link voltage drops 2.5V which is less than 1% of the initial value 702V. (Well-designed capacitor bank size)
- The capacitor bank has to be recharged within 1/14 s = 71.4ms. With 1A the recharging is well issued.

Figure 4 and 5 is a zoom of Figure 3.

Figure 4: Output current.
Blue trace: measured output current
Purple trace: Set current
Green trace: Magnet current.

Figure 5: DC Link voltage.

It is to be seen that due to the cable and output filters is the magnet current (350A) somewhat higher than the actual measured current (340A) at the PS output leads. This difference must be compensated in the set value.

The shown DC-Link voltage at the bottom trace displays influence of the 40kHz triangle current demand.

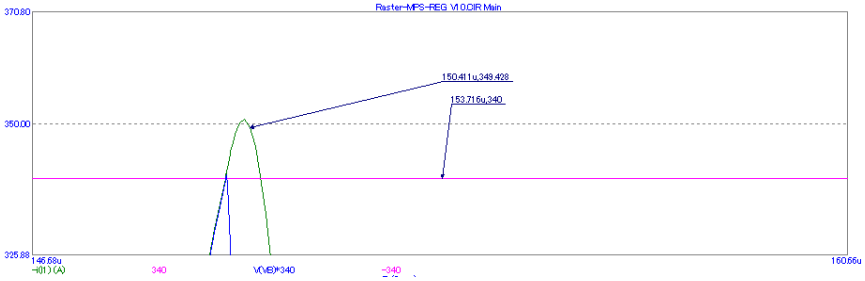


Figure 4

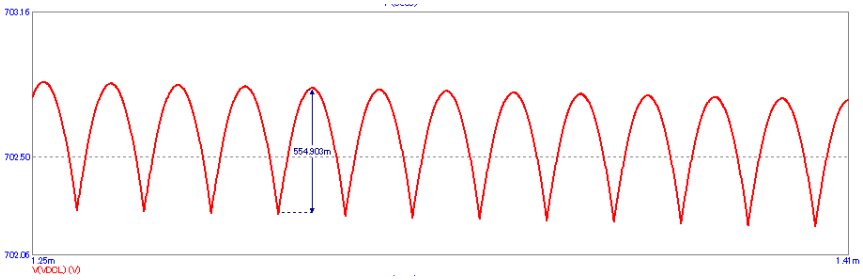


Figure 5

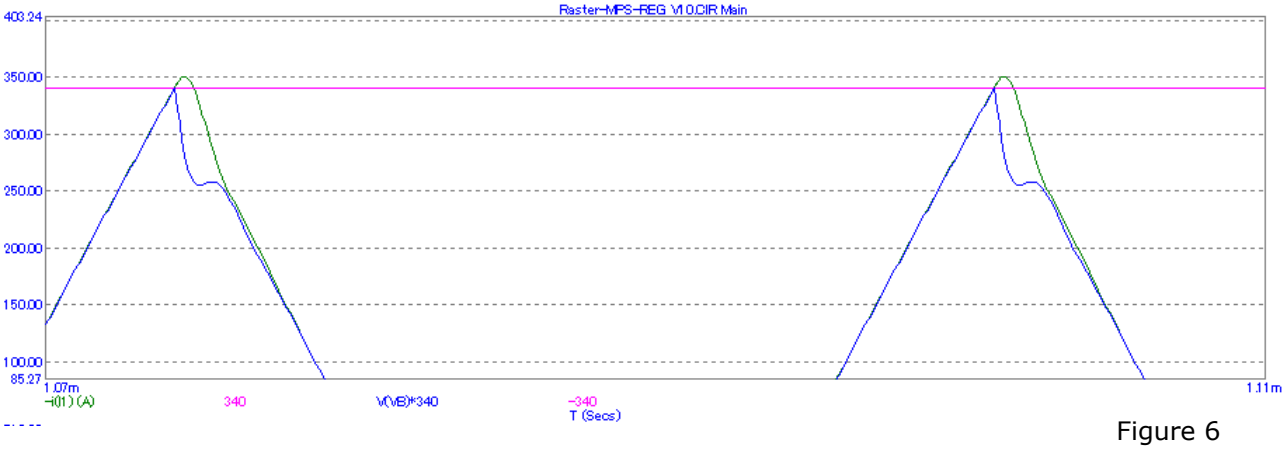


Figure 6

Figure 6 which is a zoom of Figure 3 shows the current distortion due to the cable.

Green trace: Magnet current
Blue trace: Output current of the power supply.

2.3.2. OFFSET Regulation

Figure 7 to Figure 9 below illustrate the working of the OFFSET adjustment circuit.

Figure 7: A 300ns clock asymmetry is imposed and OFFSET regulation circuit is disabled.
Figure 8: First burst with 300ns clock asymmetry and OFFSET regulation circuit enabled.
Figure 9: Second burst with 300ns clock asymmetry and OFFSET regulation circuit enabled.

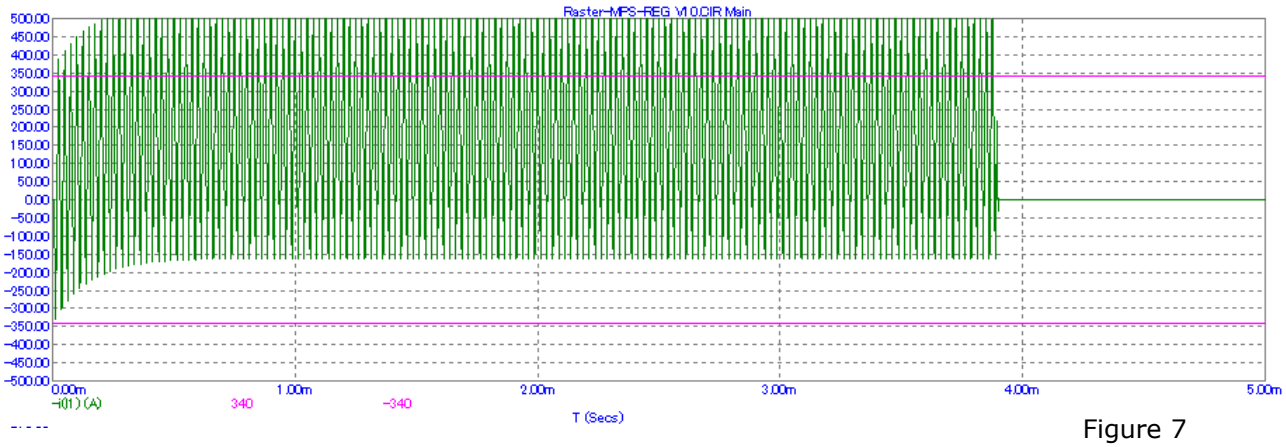


Figure 7

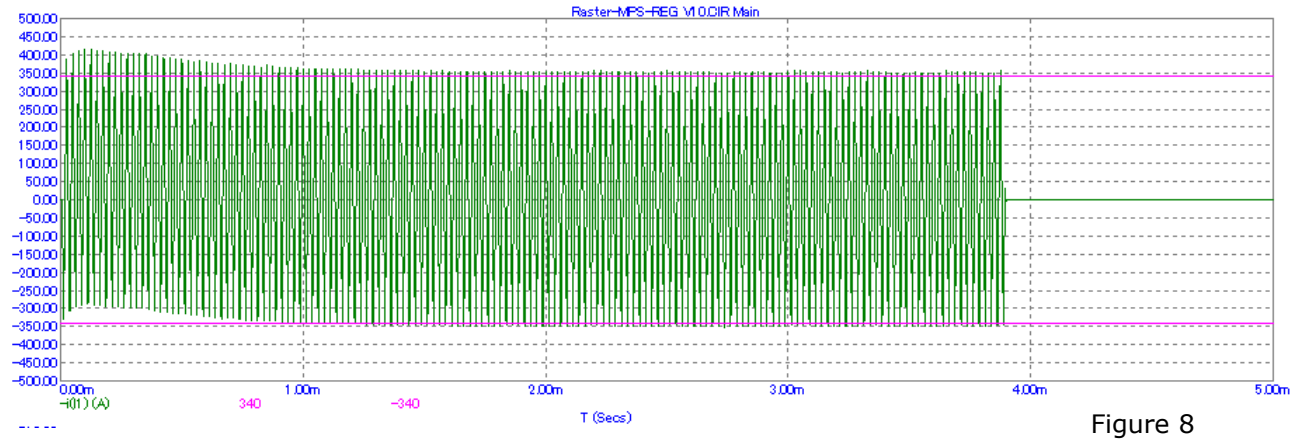


Figure 8

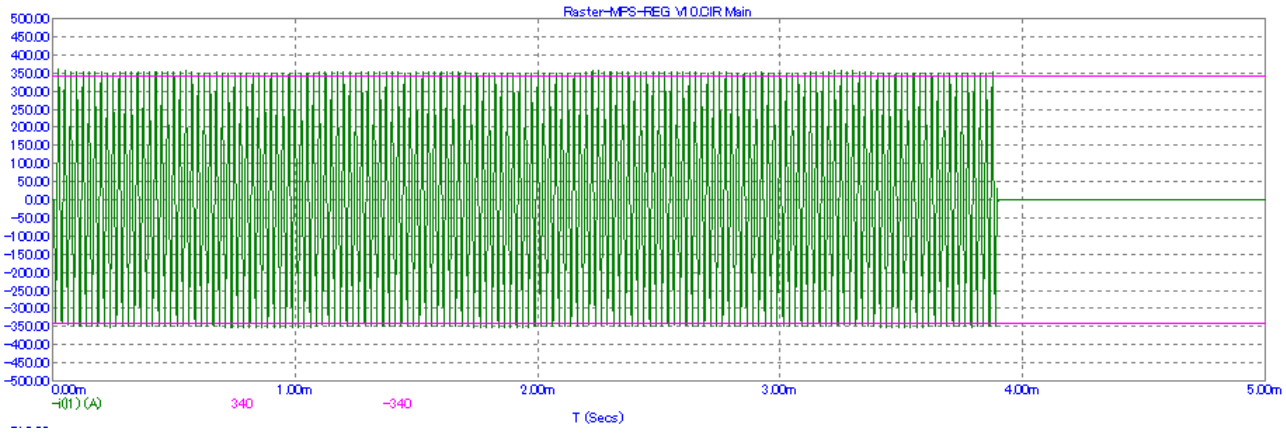
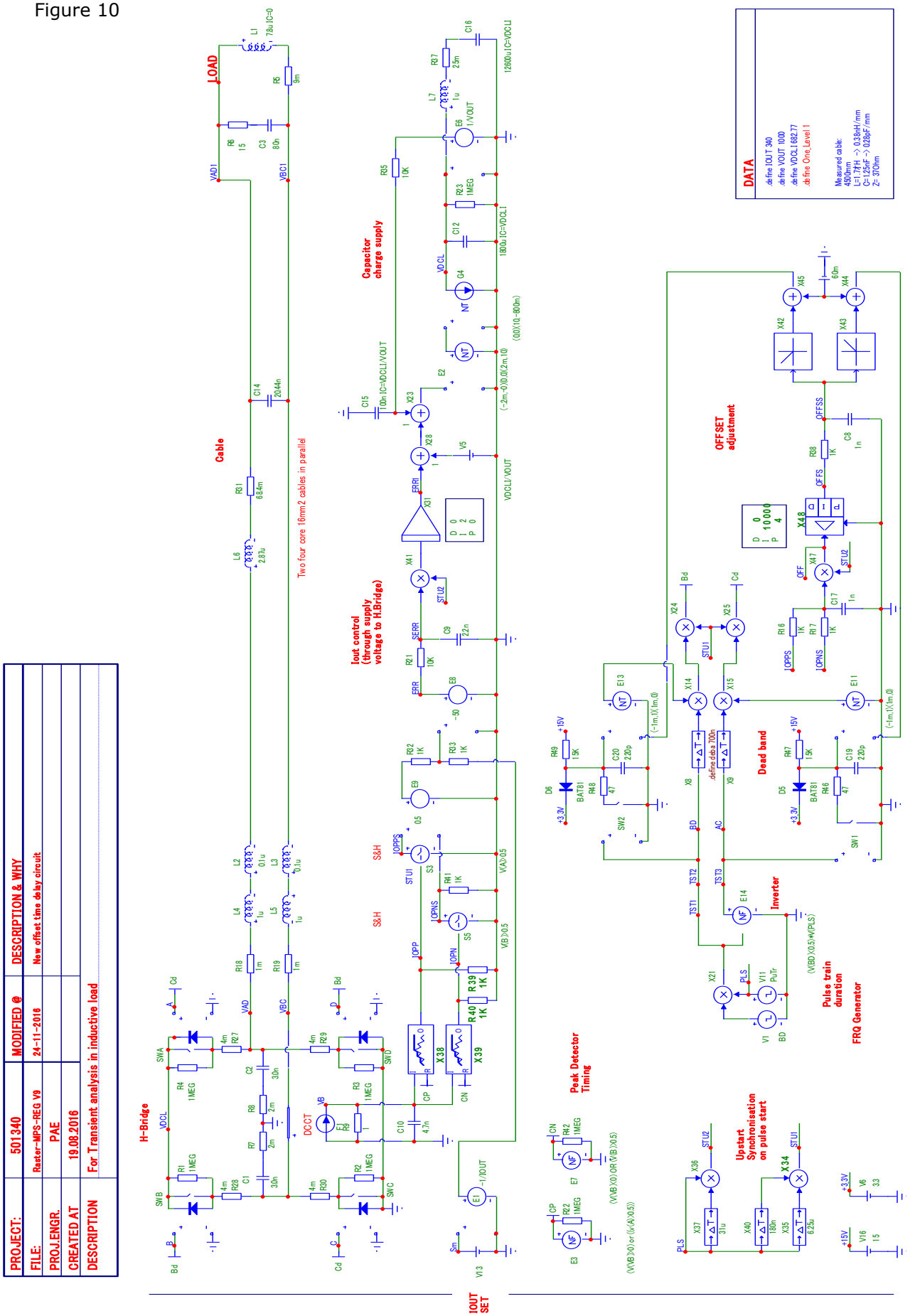


Figure 9

Figure 10


PROJECT: 501340
MODIFIED @
DESCRIPTION & WHY
FILE: Raster-MPS-REG V9
24-11-2016
New offset time delay circuit
PROJ.ENGR. PAE
CREATED AT 19.08.2016
DESCRIPTION For Transient analysis in inductive load
LOAD
Cable
Two four core 16mm2 cables in parallel
Capacitor charge supply
Iout control (through supply voltage to H.Bridge)
H-Bridge
S&H
OFFSET adjustment
Dead band
Inverter
Pulse train duration
FRQ Generator
Peak Detector Timing
Upstart Synchronisation on pulse start
DATA
define IOUT 340
define VOUT 1000
define VDCL1 682.77
define One_Level 1
Measured cable:
430mm
L=1.71H -> 0.38nH/mm
C=125nF -> 026pF/mm
Z= 37Ohm
IOUT SET

3. Regulation Module Sub circuits

This chapter describes Figure 3 in further detail. The tasks described are both tasks within the FPGA as well as the supporting circuits around the FPGA.

The main tasks are:

- Timing & Control
  - Divisor and timing
  - Upstart synchronization
  - Pulse frequency clock
  - Control signals for sub circuits
  - Burst Width Limiter
- DC-Link set point
- AD Converters
- DA Converter
- Output Current Loop I controller ("slow" loop controlling the amplitude)
- "Input Converter" interface
- H-Bridge Signal Drive
- Offset Delay circuit (symmetry regulation, "fast" loop controlling the offset)
  - PI controller
  - Rectifier
  - Dead Band & Pulse Width delay
- Bleeder Interface
- Interlock minimum hold time
- Warning handling
- Test Generator

3.1. Timing & Control

Blocks: "Clocks"; "Timing and Control"; "Burst Width …"; "Upstart Synchronization"

The "Timing & Control" function realised inside the FPGA covers the following tasks:

- Internal timing
- Upstart synchronization
- Pulse frequency clock (in quarters) (10 to 40kHz)
- Burst width timer
- Maximum burst repetition frequency limiter
- Signal for H-Bridge (10 to 40kHz)
- Control signals for peak detectors, S/H

3.1.1. Error! Reference source not found.

Block "Clocks"

Realised inside the FPGA

The clock for the timing is taken from the incoming external 88MHz clock. If this clock is missing, an automatic switch redirects the timing circuit to a regulation module internal crystal driven crystal oscillator having the same frequency within an accuracy of 25ppm.

Notes: If a timing skew of 100ns is allowed after 4.2ms, the asynchronous internal clock must have an accuracy of 100n/4.2ms = 24 ppm.

3.1.2. Upstart synchronisation

Block "Upstart Synchronization"

For right upstart timing following synchronisation signals are generated inside the FPGA.

#1. Active signal delayed a quarter of a pulse width after receiving the synchronized Pre-Trig signal lasting until the last pulse given at zero output current. This to ensure proper start and ending at zero output current thereby having no start or ending offsets.

#2. Active signal after two positive and two negative current peaks and ends at the same time as the burst. When active it enables the offset regulation and AD sampling. The delay is equal to 2*1/f

Figure 11

below shows a positive and a negative burst start.

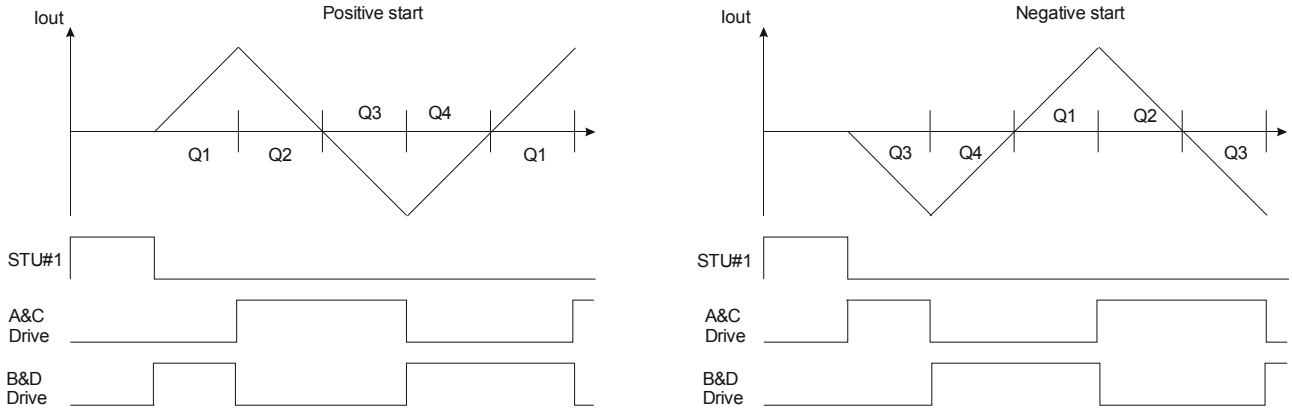


Figure 11

3.1.3. Error! Reference source not found.

Block "Timing Control"

Function inside the FPGA.

When a Pre-Trig signal is received, a burst is generated with a fixed length. This length is per default set to 4.2ms, but adjustable through a parameter setting (local RS422 line used for factory settings).

Note: The burst length can only be changed by service personnel.
Note: The burst width ends at zero output current.

At the same time as the Pre Trig signal arrives, a burst repetition timer is started, which inhibits a restart before this time has elapsed (to limit the burst repetition frequency). This timer can also be set through a parameter, but per default it is set to 70ms.

Note: If a Pre-Trig signal is received within the 70ms, a HW warning signal must be generated and no further bursts can be generated before a reset signal is issued.
Note: The burst repetition timer can only be changed by service personnel.

Figure 12 below shows the output current timing definition.

Note! Synchronisation to master clock is not shown.

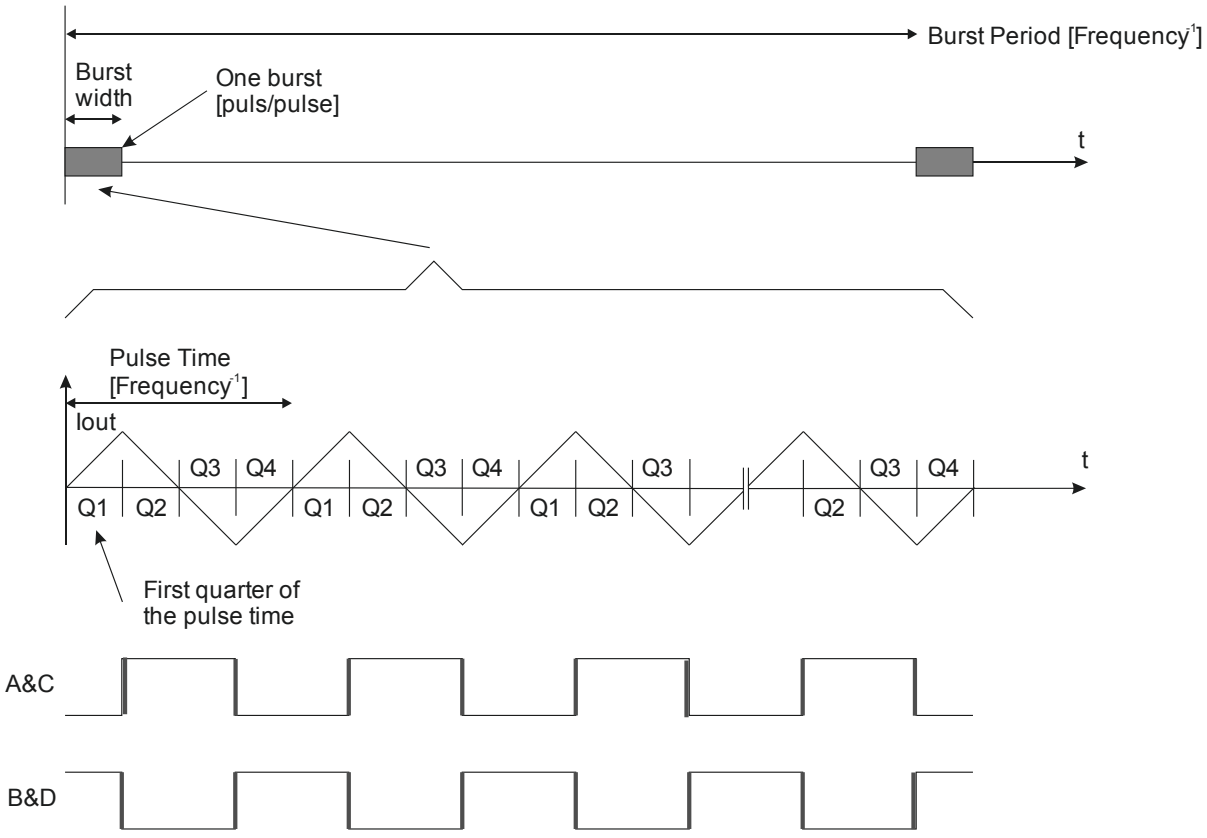


Figure 12

3.1.4. Control Signals for Sub Circuits

Block "Timing Control"

Circuits that need timing signals, such as S/H and Peak detectors, get their signals from the timing and control circuit. The signals are generated by the FPGA.

Figure 13 below shows the generated signals:

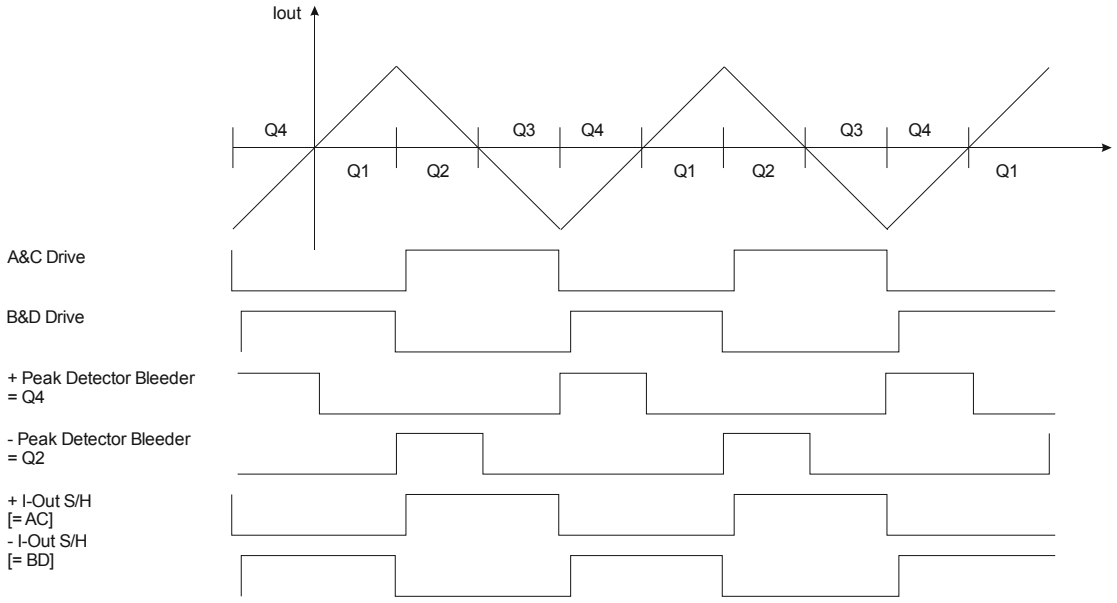


Figure 13

Note: In power OFF is the peak detector bleeder signal active.

3.1.5. Error! Reference source not found.

Function inside the FPGA.

Not to overload the power supply with too many bursts per second a burst limiter is to be implemented. This time is set with the parameter TBR.
If the power supply is triggered before the minimum time has elapsed, then further bursts are skipped and the error flag raised.

3.2. Error! Reference source not found.

Block "V_DC-Link Predict"

Function inside the FPGA.

Based on the set output current and frequency, a DC-Link voltage is predicted (feed forward): $V_{DC\text{-}Link\text{-}Set} = I_{Set} * F_{Set} *$ VFFF where VFFF is parameter adjustable.

The predicted DC-Link voltage is summed with the output of the "slow" current-loop to form the set-point for the capacitor charge PS after each burst.

Note: This calculation is only inhibited during a burst period. I.e. if the set current is changed between two bursts, the set-point for the capacitor charge PS must be updated accordingly.
Note: Time between new I-set values is larger than 1ms. (In this case the DC-Link voltage will of course not be able to follow)

3.3. Error! Reference source not found.

Blocks "12-bit ADC"

The positive and negative peak-detected output currents are converted with 12-bit AD converters having an SPI interface to the FPGA. The AD type implemented is DAC7611. This DAC has an internal reference and a maximum output voltage of 4.085V which corresponds to a DC-Link voltage of 819V, or well above desired level. Not amplifying this signal will automatically limit the DC Link voltage to 819V.

3.4. Error! Reference source not found.

Block "12-bit DAC"

The set point to the input converter is an analogue value from 0 to 5V, where 5V equals 1kV. A DAC connected with an SPI line to the FPGA gives the analogue set point value. The DA type is ADS7822

The FPGA starts reading the values after upstart signal STU#2, thereafter every half a pulse duration until the end of the burst period.

Due to the peak detector and S/H circuits the FPGA has ½ a pulse period to read the ADC values which with 40kHz is 12.5 µs. The conversion time of the ADC's is 12µs when using a 1 MHz Clock.

3.5. Output Current PI controller

Block "PI-Controller"

Function inside the FPGA.

The two sampled and running average filtered 12-bit ADC values representing the positive and negative output current are numerically summed and scaled to represent a 16-bit value for full scale for thereafter to be subtracted from the 16 bit I-Set value as the ERROR signal for the PI controller that, with a given but adjustable gain (IP) and integral part (II), modifies the DC-Link voltage set point. This "slow" loop is operated once pr. burst.

Note: The scale factor, gain and integral part values are settable.
Note: Current over shoots of 25% may occur, that is 100% output current of the 12-bit ADC's are only 80% reading or in other words 125% measured current is 100% of the 12-bit ADC range.

3.6. Error! Reference source not found.

Block "12 bit DAC"

The DC-Link set voltage is transferred via an SPI channel to a 12 bit DAC, which could be of the type DAC7611.
There must be an adjustable maximum and minimum (VMAX and VMIN) value, limiting the settable range of the DC-Link set value.

The capacitor charge PS must be enabled when the power supply is ON. However, the capacitor power supply must be disabled if the bleeder is enabled. See also chapter 3.9.

Disabling Capacitor Charge PS when: [Cap Voltage to high] or [Interlock present] or [Is OFF]

3.7. H-Bridge Signal Drive

Block "Delay and dead time"

Function inside the FPGA.

The A&C and B&D drive signals for the H-Bridge are derived from the clock frequency including dead band and corrective delays, ref. section 3.8).

The H-Bridge is driven as follows supposing the first pulse starts positive:

- Leg B & D turns ON simultaneously
- After a fixed time given by the pulse frequency all MOSFET's are turned OFF
- After a fixed dead time leg A & C will be turned ON
- After a fixed time given by the pulse frequency all MOSFET's are turned OFF
- After a fixed dead time, leg B & D will be turned ON
- Etc.

The above scheme is illustrated in Figure 14.

Note: In pauses between bursts, or when power supply is OFF, all MOSFETs are OFF.

Note: In case of any interlock, all MOSFETs must be driven OFF regardless of operating state.

The drive signals are transferred to the Power Cubicle as balanced symmetrical lines suited for the gate driver module.

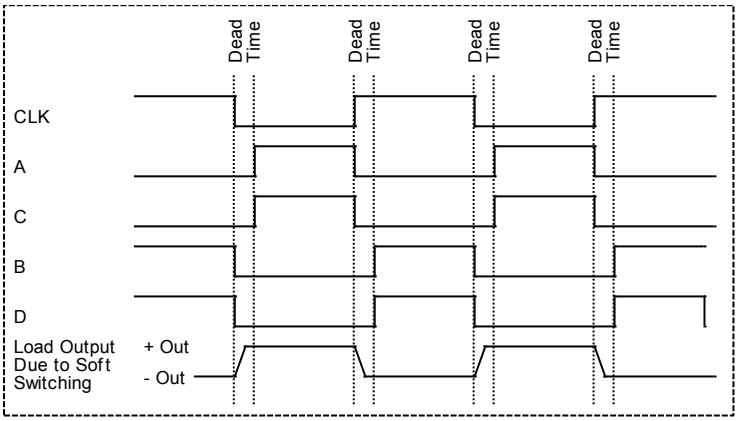


Figure 14

3.8. Error! Reference source not found.

Block "Fast PI controller"; "+ Rectifier" & "- Rectifier"; "Dead time"

Function inside the FPGA.

When reading this chapter please also refer to **Error! Reference source not found.** and Figure 7 to Figure 9.

3.8.1. Theory

Due to slightly timing deviations and component tolerances, the positive and negative voltage integral across the inductive load may be slightly different. This will lead to an offset in the output current wave shape (an uncontrolled timing deviation of just 1ns at 40kHz will sum up to a current offset of 3% over 4.2ms). To overcome this issue, an offset regulation circuit must be implemented.

The offset regulation circuit works as follows:

For every triangle period in a burst, the positive and the negative peak current is compared. The difference between positive and negative current (the offset) is input to a PI controller, whose output presents a correction variable to eliminate the offset. As the loop is a pulse-by-pulse regulation, its operating rate equals the pulse frequency ("fast" loop).

Loop parameters to set are:

- Integral factor
- Proportional factor
- Max correction output value

Note: Important: Between bursts, the PI controller is paused and the output value and integrator content is kept as starting value for the next burst.

Before switching an H-bridge leg ON a fixed dead band of 700ns (where all Mosfet's are OFF) is inserted, which is much wider than the required offset regulation span.

Note: Actually due to the soft switching where the total seen output inductance (output choke, cable and the load) the length of this dead time has no practical meaning, as long as it is lower than a quarter of the pulse duration, and the stored energy of the total inductances are large enough to keep the output voltage switched (continuous current)

Note: As soon as the B-Bridge is turned OFF the load inductances will perform the switching transition.

Before switching an H-bridge leg OFF a variable time delay is inserted proportional to the output of the PI controller. The added delay is implemented as given below:

- Positive PI values results in B&D leg delays
- Negative PI values results in A&C leg delays
- The delay is a multiple of half clock cycles (1/88e6 * ½ = 5.7ns)

Note: The delays can be implemented as a pre-set able count down counter.

Note: It is to be ensured that the added variable switch OFF delay is shorter than the fixed switch ON delay.

Error! Reference source not found. below shows as left top trace a symmetrical H-Bridge drive. Below left the A&C drive is delayed with a time equal to +d ns. It is to be seen, that pulse pause width relationship has been changed with 2*d ns. The right traces show the same but where the B&D drive signal has been delayed +d ns. It is to observe that the pulse pause relationship between the right output trace and left are different concerning the pause and pulse width.

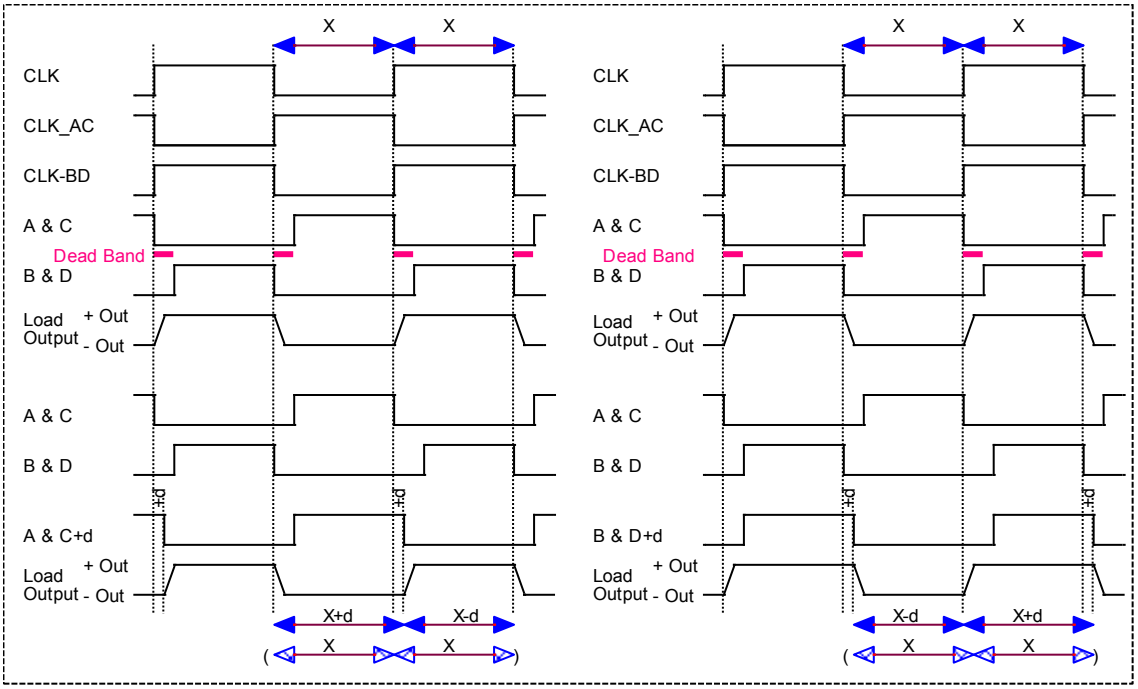


Figure 15

3.9. Bleeder Interface

Partly within the FPGA and partly outside.

Without a Bleeder, the only manner to discharge the capacitor is to:

- Use the energy during a bursts
- Turning the power supply off thereby activating a discharge circuit

Due to the above it will not be possible to set a lower output current needing a lower capacitor voltage without a bleeder circuit.
The bleeder circuit is turned on if the DC-Link voltage is above 2% of the set value.
The bleeder discharge must be equal or at least a bit faster than charging of the DC-Link capacitors with the given capacitor charge PS.

A comparator compares the set capacitor voltage with the measured capacitor voltage. If the measured voltage is too high, the bleeder is enabled.
The bleeder is also enabled when the power supply is OFF or an interlock is present.

Enabling Bleeder when: [Cap Voltage to high] or [Interlock present] or [Is OFF]

3.10. Interlock Minimum Hold Width

The FPGA must handle/generate a number of interlock signals:

Basic logic signals:

- Over-current (from comparator on regulation module)
- Over-voltage (from comparator on regulation module)
- A/D MOSFET driver fault (from A/D MOSFET driver)
- B/C MOSFET driver fault (from B/C MOSFET driver)
- Earth leakage (from earth leakage detector)
- Capacitor charge PS fault (from capacitor charge PS)

Any of these interlock signals must prevent further operation of the power supply by:

- Disabling the capacitor charge PS
- Driving all MOSFETs OFF
- Enabling the bleeder
- Reporting the given interlock signal(s) to the control system

Since many of the interlock signals are transient by nature, a min-time-hold function must be implemented, ensuring that any fault condition is reported to the control system for a minimum of 500ms.

3.11. Warning handling

The FPGA must handle/generate a number of warning signals:

If a Pre-Trig signal is received before the defined minimum burst repetition time since the previous burst has elapsed, a warning must be generated, and the Pre-Trig signal must be ignored.

The following conditions must also generate a warning:

- If no polarity signal is present, see Figure 1
- If no external clock signal is present, see Figure 1

3.12. First Pulse Polarity

Block "--; Polarity"

The first triangle current must either start with a positive or negative top depending on the "Polarity I" signal.

The interpretation of the "Polarity I" signal is as follows:
High signal = Start positive
Frequency above 10kHz = Start negative
Low/No signal = Start negative, set the warning signal

This functionality can be implemented by starting the pulse clock inverted. That is pulse generator BD on the simulation Figure 10. See also Figure 11.

3.13. Test Generator

Block "Test Generator"

If a test jumper is applied to the regulation module, the timing and control is transferred to internally generated trigger signals. The following controls are implemented:

- Test mode jumper
- Set to always to 40kHz
- Manual Pre Trig input (Single burst)
- Automatic Pre Trig generation (Continuous bursts given by the minimum burst repetition time)

For easy board and system tests, a test generator circuit is implemented.
Following test cases are foreseen:

a) Enable test generator circuit
Must be set to activate the below functions
b) Force to 40kHz pulse operation
Note! If not forced to 40kHz the programmed frequency must be used
d) Manual trig (In parallel with external Pre Trig)
e) Automatic multi bursts after trig (After minimum burst repetition time)

4. Interface

4.1. HW Interfaces

The regulation module will be designed to be attached to the System 8500 control module, connector P2.
See manual for the system 8500 control module for functions and interface

The regulation module will be a PCB module with the approximately outline given in Figure 16.

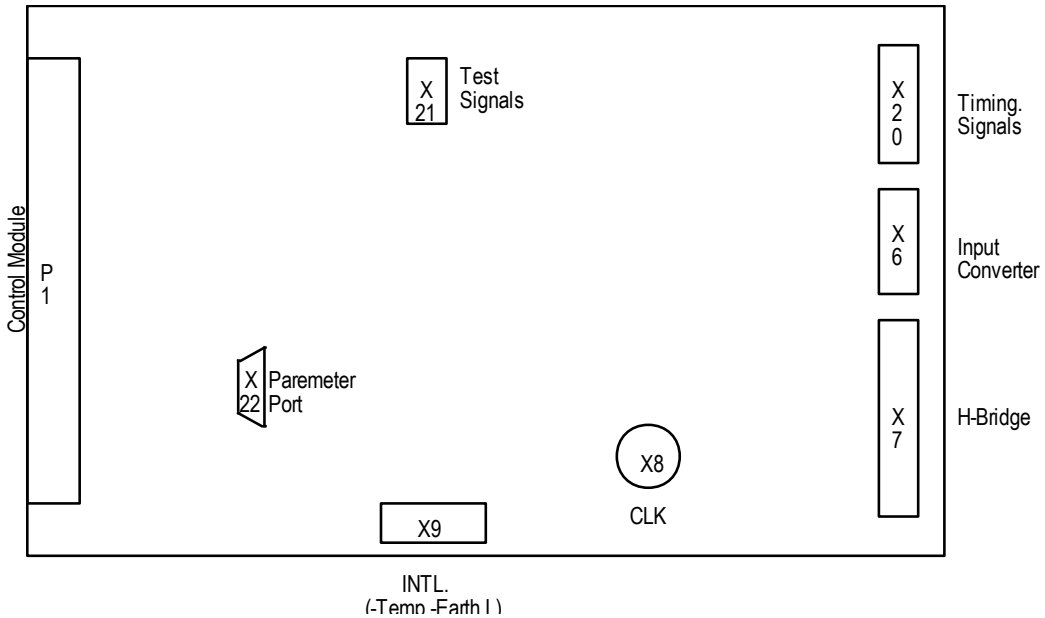


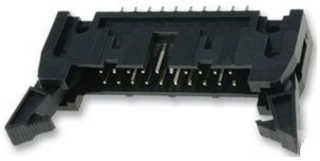
Figure 16

4.1.1. P1 Control Module Interface

Please refer to the "P2" description of the system 8500 control module manual for detailed explanation of all signals and type.

4.1.2. X6 Input Converter Interface

The interface signals to the input converter are given in the table below.



FC 10 pin Male connector

Pin	Name	Value	I/O	Description
1	GND		-	Return of pins 2-9
2	GND		-	Return of pins 2-9
3	V_{mon_I}	(0..5V)	I	Monitor output current
4	V_{mon_v}	(0..5V)	O	Monitor output voltage
5	/INHIBIT		O	Digital input signal 10k pulled up
6	V_{set_v}	(0..5V)	O	Set value output Voltage
7	V_{set_i}	(0..5V)	O	Set value output current
8	V_{ref}	5.1V	I	Reference
9	/ON	5V	O	Digital input signal 10k pulled up
10	NU		-	Not used

The signals are connected with a flat cable to a DB9 male connector on the back of the cubicle. The pin-numbers given above refer to flat-cable indexing, not DB9 pin numbers.

4.1.3. X7 H-Bridge Interface

The signals to the H-Bridge are connected with a flat cable to a DB37 Female connector on the back of the cubicle

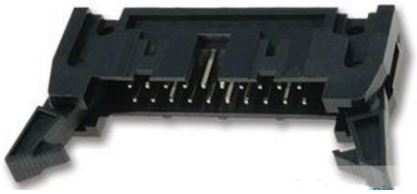


Figure 18

FC 40 pin Male connector

Pin	Name	Value	I/O	Description
1	AD-Power	12V	O	Power Supply Output Pin for gate driver AD
2	AD-Common		-	Common
3	AD-HS-P	5V	O	Positive Line of 5 V Differential High Side PWM Signal Pair. Terminated Into 250 Ω on gate driver.
4	AD-HS-N	5V	O	Negative Line of 5 V Differential High Side PWM Signal Pair. Terminated Into 250 Ω on gate driver.
5	AD-	5V	O	Positive Line of 5 V Differential Low Side PWM Signal Pair.

FC 40 pin Male connector

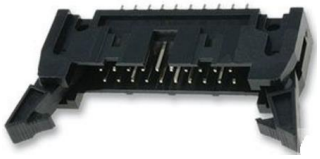
Pin	Name	Value	I/O	Description
	LS-P			Terminated Into 250 Ω on gate driver.
6	AD-LS-N	5V	O	Negative Line of 5 V Differential Low Side PWM Signal Pair. Terminated Into 250 Ω on gate driver.
7	AD-FAULT- P	5V	I	Positive Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
8	AD-FAULT- N	5V	I	Negative Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
9	AD-RTD-P	5V	I	Positive Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20 mA. Temperature Measurement is Encoded Via PWM.
10	AD-RTD-N	5V	I	Negative Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20mA. Temperature Measurement is Encoded Via PWM.
11	AD-PS-Dis	5V	O	Pull Down to Disable Power Supply. Pull Up, or Leave Floating to Enable. Gate-Source will be Connected with 10 kΩ when disabled.
12	AD-Common		-	Common
13	AD-PWM-EN	5V	O	Pull Down to Disable PWM Input Logic. Pull Up/Leave floating to enable. Gate-source will be held low through gate resistor if power supplies are enabled.
14	AD-Common		-	Common
15	AD-OC-EN	5V	O	Over-current Protection Enable. Pull down to disable detection of over-current fault. PWM and UVLO will continue to function. Pull up or leave floating to enable detection of over-current fault.
16	AD-Common		-	Common
17	BC-Power	12V	O	Power Supply Input Pin for gate driver AD
18	BC-Common		-	Common
19	BC-HS-P	5V	O	Positive Line of 5 V Differential High Side PWM Signal Pair. Terminated Into 250 Ω on gate driver.
20	BC-HS-N	5V	O	Negative Line of 5 V Differential High Side PWM Signal Pair. Terminated Into 250 Ω on gate driver.
21	BC-LS-P	5V	O	Positive Line of 5 V Differential Low Side PWM Signal Pair. Terminated Into 250 Ω on gate driver.
22	BC-LS-N	5V	O	Negative Line of 5 V Differential Low Side PWM Signal Pair. Terminated Into 250 Ω on gate driver.
23	BC-FAULT- P	5V	I	Positive Line of 5 V Differential Fault Condition Signal Pair. Drive Strength 20 mA.
24	BC-	5V	I	Negative Line of 5 V Differential Fault Condition Signal Pair.

FC 40 pin Male connector

Pin	Name	Value	I/O	Description
	FAULT- N			Drive Strength 20 mA.
25	BC-RTD-P	5V	I	Positive Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20 mA. Temperature Measurement is Encoded Via PWM.
26	BC-RTD-N	5V	I	Negative Line of 5 V Temperature Dependent Resistor Output Signal Pair. Drive Strength 20mA. Temperature Measurement is Encoded Via PWM.
27	BC-PS-Dis	5V	O	Pull Down to Disable Power Supply. Pull Up, or Leave Floating to Enable. Gate-Source will be Connected with 10 kΩ when disabled.
28	BC-Common		-	Common
29	BC-PWM-EN	5V	O	Pull Down to Disable PWM Input Logic. Pull Up/Leave floating to enable. Gate-source will be held low through gate resistor if power supplies are enabled.
30	BC-Common		-	Common
31	BC-OC-EN	5V	O	Over-current Protection Enable. Pull down to disable detection of over-current fault. PWM and UVLO will continue to function. Pull up or leave floating to enable detection of over-current fault.
32	BC-Common		-	Common
33	Power	12V	O	Power Supply Input Pin
34	CRB-P	5V	O	Bleeder disable
35	CRB-N	0V	-	Return signal for Bleeder disable
36	OTI	NC	I	Over temperature Interlock (0V as return)
37	ELI	NC	I	Earth Leakage Interlock (0V as return)
38	-	-	-	Not connected
39	-	-	-	Not connected
40	-	-	-	Not connected

4.1.4. X20 Timing Signal Interface

The signals are connected with a FC16



FC 16 pin Male connector

Pin	Name	Value	I/O	Description
1	Enable	Logic	I	External Active low signal to enable PS
2	0V		-	
3	INTL	Logic	O	Active high when PS is interlocked
4	0V		-	
5	Pre-Trig	Logic	I	Start pulsing
6	0V		-	
7	Beam Run Permit	Logic	O	Beam may be issued
8	0V		-	
9	Trig Permit	Logic	O	All OK for burst
10	0V		-	
11	Polarity I	Logic	I	Start with given polarity
12	0V		-	
13	I-Ready	Logic	O	Output current within 1% of set value
14	+5V		-	
15	Status A.	Logic	O	Status available. Read status command
16	+5V		-	

4.1.5. X21 Test Signal Interface

The signals are connected with a 14 pin male connector

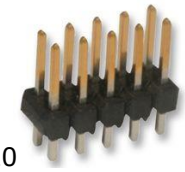


Figure 20

10 pin DIL Molex male connector

Pin	Name	Value	I/O	Description
1	Test	5V	I	Pulled up to 5V. Connect to 0V to enable test mode
2	0V		-	0V
3	Multi		I	Pulled up to 5V. Connect to 0V to enable multi burst test mode Else single burst mode
4	0V		-	0V
5	Trig		I	Pulled up to 5V. Connect to 0V to trig a burst
6	0V		-	0V
7	40kHz		I	Forced to 40kHz operation
8	0V		-	0V
9	5V		O	5V Max 100mA (PTC fused)
10	0V		-	0V

4.1.6. X8 88MHz clock

Figure 21

2 pin female connector SMA

Pin	Name	Value	I/O	Description
Center	CLK	-	I	88 MHz clock input
Screen	GND	-	I	GND

4.1.7. X22 RS 422 Parameter setting Port

Setting parameters for the regulation module is done through an RS422 interface connection.

DB9 pin Female connector

Pin	Name	Value	I/O	Description
1				
2	RxD-	-	I	- Receive
3	TxD-	-	O	- Transmit
4				
5	GND	-	-	Ground
6	RxD+	-	I	+ Receive
7	TxD+	-	O	+ Transmit
8	-	-	-	-
9	-	-	-	-

4.1.8. FPGA Signal interface

The FPGA will have the following HW inputs:

Signal	Pin	Type	Description
Is ON	TBD	Logic	State signal from control system
Output current set value	TBD	Logic	16 bit parallel set value from control system
Frequency Set	TBD	SPI	12 bit serial data from the control system (FPGA is slave) Sets the pulse frequency
External Clock	TBD	Logic	88 MHz
Internal Clock	TBD	Logic	88 MHz
Polarity Input	TBD	Logic	Start at given polarity (High="positive", 10kHz="negative")
Pre-Trig	TBD	Logic	Start pulsing
Positive peak current measurement	TBD	SPI	12 bit serial DAC on regulation module (FPGA is master)
Negative peak current measurement	TBD	SPI	12 bit serial DAC on regulation module (FPGA is master)
Factory setup	TBD	RS422	Parameter setup via terminal (FPGA is slave)
Over-current Positive	TBD	Logic	Comparator on regulation module
Over-current Negative	TBD	Logic	Comparator on regulation module
A/D MOSFET driver fault	TBD	Logic	From A/D MOSFET driver
B/C MOSFET driver fault	TBD	Logic	From B/C MOSFET driver
Earth leakage	TBD	Logic	From earth leakage detector (for future upgrade)
Capacitor charge PS fault	TBD	Logic	From capacitor charge PS (for future upgrade)
A/D MOSFET temperature	TBD	PWM	from A/D MOSFET driver (for future upgrade)
B/C MOSFET temperature	TBD	PWM	from B/D MOSFET driver (for future upgrade)
Manual Trig	TBD	Logic	
Single/Multi	TBD	Logic	
40kHz Operation	TBD	Logic	
Set test mode	TBD	Logic	Enable test mode
Test trig	TBD	Logic	Single or multi burst test
Force to 40kHz	TBD	Logic	Test condition
Spare 1	TBD	Logic	
Spare 2	TBD	Logic	
Charged voltage too high	TBD	Logic	Comparator on regulation module
Charged voltage too low	TBD	Logic	Comparator on regulation module

Note: SPI lines can be input and output
Note: More HW lines may be added

The FPGA will have the following HW outputs:

Signal	Pin	Value	Description
DC-Link set voltage	TBD	SPI	12 bit DAC setting charge voltage (FPGA is master)
Capacitor charge PS ON	TBD	Logic	Turns capacitor charge PS
Capacitor charge PS INH.	TBD	Logic	Inhibits capacitor charge PS
A; B; C; & D	TBD	Logic	H-Bridge driving signals
Switched to Internal Clock	TBD	Logic	Status signal confirming presence of external clock
Clear Pos. peak detector	TBD	Logic	Control signal resetting the positive peak detector
Clear Neg. peak detector	TBD	Logic	Control signal resetting the negative peak detector
Status Available	TBD	Logic	Flag indicating the presence of a status/warning sig.
Trig Permit	TBD	Logic	FPGA will start burst when trigged
Beam run permit	TBD	Logic	TBD
Bleeder disable	TBD	Logic	Disables bleeder (in output converter)
I-Ready	TBD	Logic	Output current for last burst was within 1% of set value
Over-current/-voltage	TBD	Logic	Interlock for control system, 500ms min-time-hold
Summed MOSFET driver fault	TBD	Logic	--||--
Earth leakage	TBD	Logic	--||--
Pre-Trig Error	TBD	Logic	Warning for control system, latched
Missing polarity signal	TBD	Logic	--||--
Missing external clock	TBD	Logic	--||--

Note: SPI lines can be input and output
Note: More HW lines may be added

4.2. SW Setup Local Interface

Various control parameters are changeable and can therefore be down-loadable to the FPGA through a RS422 connection carrying ASCII characters (dedicated DB9 connector on the regulation module)

The parameter syntax is as follows:

[Parameter name] sp [Value] cr {sp=space; cr= carriage return; lf= line feed}
Line feed characters may be transmitted, but should be ignored.

All parameters can be read at any time, but parameters can only be set when power supply is OFF.

The following parameters are foreseen:

Param.	Range	Unit	Useful range	R/W	Description
FMAX	0-4095	10Hz	0-40950Hz	R/W	MAXimum allowable Frequency setting
FMIN	0-4095	10Hz	0-40950Hz	R/W	MINimum allowable Frequency setting
FSET	0-4095	10Hz	0-40950Hz	R	Frequency SET point from control system
GA	0000-9999	0.001x	0-9.999x	R/W	Gain Adjustment of ADC for current measurement.
IBAVG	0000-9999	100ppm	0-99.99%	R	I Burst AVeraGe, average current measured during previous burst
IERROR	0000-±9999	0.01%	0-±99.99%	R	Difference between ISET and IBAVG
II	0000-±9999	0.01%	0-±99.99%	R/W	I-loop Integration constant
IIC	0000-±9999	0.01%	0-±99.99%	R/W	I-loop Integrator Content
IICMAX	0000-9999	0.01%	0-99.99%	R/W	I-loop Integrator Content Max value (positive and negative clamp)
IP	0000-±9999	0.01%	0-±99.99%	R/W	I-loop Proportional constant
ISET	0000-9999	100ppm		R	Current SETpoint from control system (converted from 16-bit parallel)
NBRPD	0000-9999	Pulse cycles	TBD	R/W	Beam Run Permit Delay, fixed time from trig
OERROR	0000-±9999	0.01%	0-±99.99%	R	Difference between OSET and OMEAS
OI	0000-±9999	0.01%	0-±99.99%	R/W	Offset-loop Integration constant
OIC	0000-±9999	0.01%	0-±99.99%	R/W	Offset-loop Integrator Content
OICMAX	0000-9999	0.01%	0-99.99%	R/W	Offset-loop Integrator Content Max value (positive and negative clamp)

Param.	Range	Unit	Useful range	R/W	Description
OMEAS	0000-±9999	0.01%	0-±99.99%	R	Offset Measurement (difference between positive and negative peak current)
OP	0000-±9999	0.01%	0-±99.99%	R/W	Offset-loop Proportional constant
OSET	0000-±9999	0.01%	0-±99.99%	R/W	Offset-loop Set-point, default 0000
RDYLIMI	0000-9999	0.01%	0-±99.99%	R/W	Ready LIMit, current (I) loop.
RDYLIMO	0000-9999	0.01%	0-±99.99%	R/W	Ready LIMit, Offset-loop.
SAVE	-	-	-	W	SAVEs savable parameters to non-volatile memory.
TBR	0000-9999	10000/CLK	0-99990000/CLK	R/W	Burst Repetition Time, the minimum time between successive bursts
TBW	0010-9999	1000/CLK	10000-9999000/CLK	R/W	Burst Width Time, the duration of a burst, from trig
TDEAD	0000-0099	1/CLK	0-99/CLK	R/W	Dead-Time, delay before MOSFET's are turned ON.
TOVMAX	0000-0099	1/CLK	0-99/CLK	R/W	MAXimum allowed Variable Time delay in Offset-loop timing correction. Must be smaller than TDEAD.
TP	0-99999	1/CLK	0-99999/CLK	R	Pulse Time in CLKs = f(CLK)/FSET
VER	-	-	-	R	Returns the VERsion and identification of the firmware built.
VFFF	0000-9999	0.01%	0-99.99%	R/W	Feed Forward Factor for the prediction of charge Voltage based on set current (ISET) and operating frequency (FSET).
VMAX	0000-9999	0.01%	0-99.99%	R/W	MAXimum allowed VSET (clamp).
VMIN	0000-9999	0.01%	0-99.99%	R/W	MINimum allowed VSET (clamp).
VSET	0000-9999	0.01%	0-99.99%	R	Voltage SETpoint

4.3. Parameter Setup, Remote SPI Interface

Block "Parameter Setting"

Param.	Range	Unit	Useful range	R/W	Description
FSET	0-4095	10Hz	0-40950Hz	W	Frequency SET point from control system (12-bit serial line)

Note: The parameter will be transmitted from the 8500 control module to the FPGA as if it is a 12 bit DAC (e.g. of the type DAC7611), with 1xLSB representing 10Hz.
40 kHz will be transmitted as: (MSB) 111110100000 (LSB)
10 kHz will be transmitted as: (MSB) 001111101000 (LSB)

Note: Independent on the received frequency setting, FSET must be limited by FMAX and FMIN (setup parameters).

5. Auxiliaries Power Supplies

5.1. Input Auxiliaries

The Regulation module gets its power from the system 8500 connection. These are:

Voltage	Accuracy	Loading	Comment
+5V	±4%		For TTL logic only
5V RTN	-		
+23V	+15%/-10%		Unregulated
0V	-		
+23V	+15%/-10%		Unregulated
D+23V	+15%/-10%		Unregulated
D0V-RTN	-		
D-23V	+15%/-10%		Unregulated

5.2. Generated Auxiliary Voltage Supplies

Voltage	Accuracy	Loading	Comment
+5V	±4%		For TTL logic and Interface module
5V RTN	-		
+3.3V	±1%		For FPGA and low voltage logic
3.3V RTN			
+A5V	±2%		For low voltage analogue circuits
A0V RTN			
-A5V	±2%		For low voltage analogue circuits
+15V	±5%		For analogue circuits
15V RTN			
-15V	±5%		For analogue circuits
+A15V	±5%		For Sensitive analogue circuits
A15V RTN			
-A15V	±5%		For sensitive analogue circuits
O+15V	±4%		For Interface module
O15V RTN	-		