NATIONAL CENTRE FOR NUCLEAR RESEARCH ŚWIERK

Description:	This document describes the production of the PIN diode device designed for the ESS LLRF control system
Title:	**Critical Design Report for the PIN Diode device**

Authors:	Marcin Gosk, Dominik Rybka
Co Authors:	Jarosław Szewiński

Version:	0.01
Date:	20.04.2018

1. Mechanical design description

Mechanical design is provided by ESS partner.

2. Tests of the prototype

PEG partner has received from ESS assembled PIN diode prototype PCB in version 3.0, dated March 2017. Basic functionality tests were performed. The block diagram of the test system is presented on Figure 1 and the photo of system during the tests is presented on Figure 2.

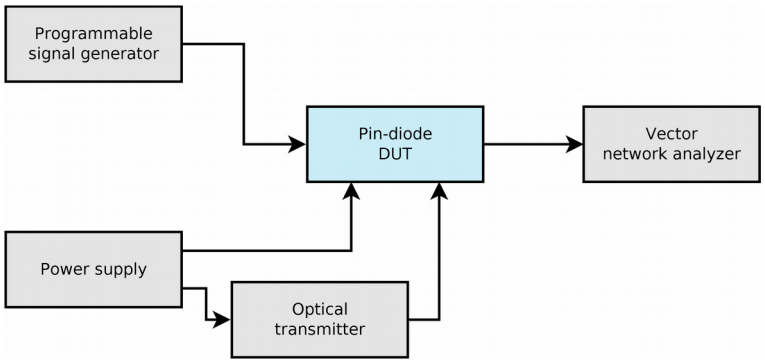

Figure 1. Test system layout

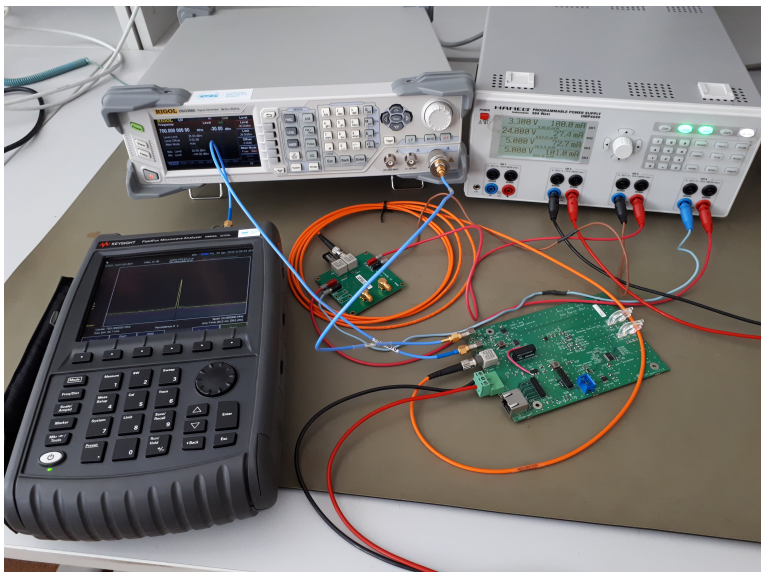

Figure 2. Test system implementation

The testing procedure consisted of analysis of the RF signal transmission through the device. As the input sinus waveform of 700MHz and amplitude level of -20dBm (output from programmable signal generator Rigol DSG3060) was used. The optical interlock signal was delivered from HFBR-0410Z evaluation board. Output level signal was measured utilizing vector network analyzer

Keysight Fieldfox N9950A. In principle, the device is working correctly. The spectra of the output signals are presented below:

- On Figure 3, when device is powered on and interlock is off
- On Figure 4, when device is powered on and interlock is on
- On Figure 5, when device is not powered on

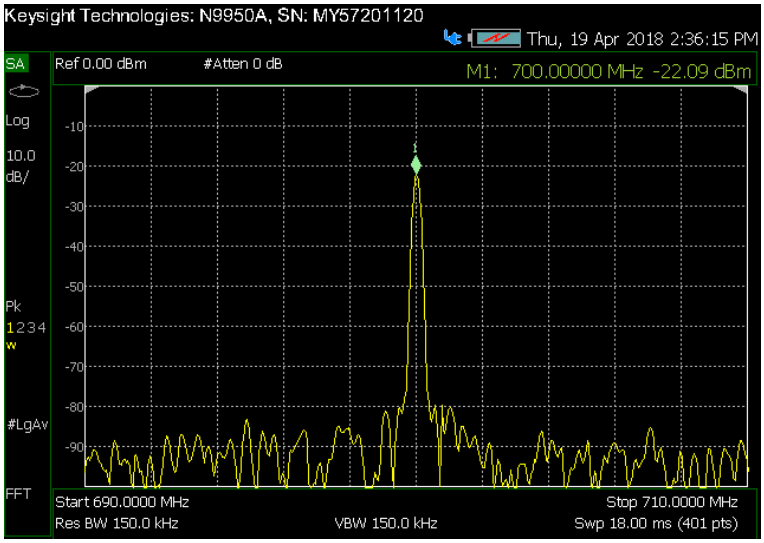

Figure 3. Output when powered is on and interlock is off

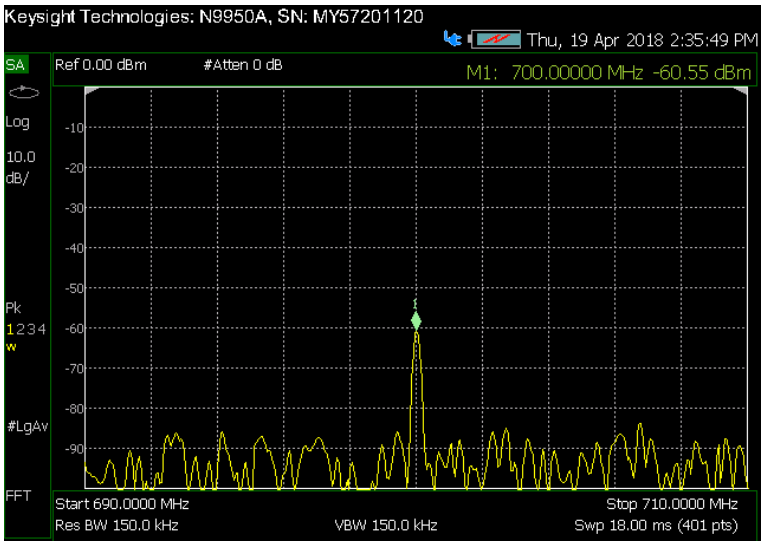

Figure 4. Output when powered is on and interlock is on

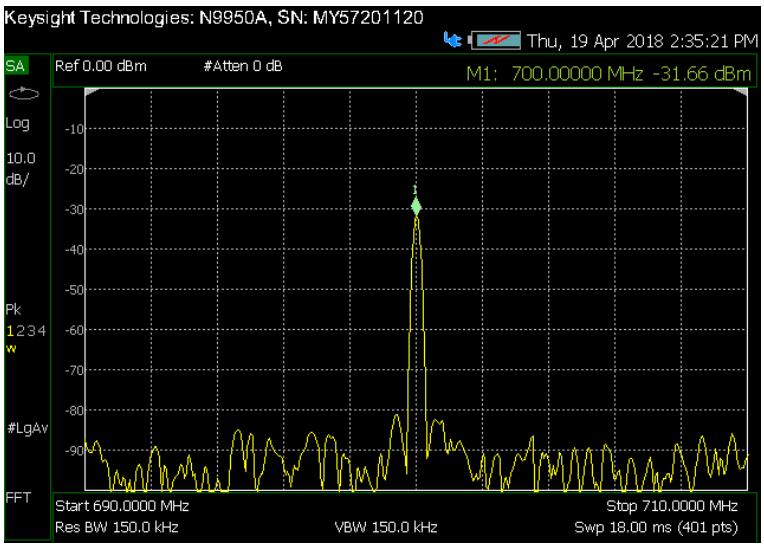

Figure 5. Output after power has been switched off

The device behavior, presented on Figure 5, should be analyzed and revised according to the specification by ESS partner.

During the optical inspection following problems were noticed:

- capacitors C5, C6 - two components soldered instead of each of them;
- connection between Ethernet connector and XT-Pico: additional components soldered, some signal lines cut;
- additional wiring after production added between U6 and C4;
- we strongly suggest to use gold-plating pads, due to used QFN package components (PCB metallization in prototype device was HAL).

This states that next improved PCB design revision should be considered. Otherwise, the quality of the devices mass production cannot be guaranteed.

Besides the functional tests, manufacturability of the device was checked. All components that are utilized in the design were available, without long lead times, in reasonable MOQ (minimum order quantity). The PCB is manufacturable in Euro Circuit company, that is able to produce printed circuit board with provided stackup.

Mechanical enclosure drawings were not provided, that's why its availability was not validated.

3. Procurement, production and delivery planning

As soon as ESS partner provides PEG with final proven designs of the device, inluding schematics of the subsystem, layout of the PCB, GERBER production files of the PCB, pick and place file for automatic components placement, bill of materials and assembly drawings of the PCB and the

mechanical enclosure, PEG partner will start the production procedure. This contains following steps:

- analysis of the changes made to the device schematics and PCB layout (if any) [0.5 month];
- verification of the production files, including GERBER production files of the PCB, pick and place file for automatic components placement, bill of materials and assembly drawings of the PCB [0.5 month];
- call for tender for PCB production and assembly [1 month];
- call for tender for mechanical enclosure manufacturing and delivery [1 month];
- production of elements in external companies [2 months];
- visual inspection of delivered elements of the device [0.25 month];
- DC electrical measurements of delivered PCBs [0.25 month];
- assembly of the devices [2 month];
- functional tests of devices [2 month];
- delivery to ESS partner [1 month].

In order to maximize production yield AOI (Automated optical inspection) will be included in terms of call for tender for PCB manufacturing.

If changes of the device layout will not be done, some additional manual PCB rework has to be applied. This can cause increase of the device assembling time because of higher failure probability and lower production yield.

4. Description of planned tests and measurements including FAT

Following tests and measurements are foreseen to be performed by PEG:

- on components delivered from external manufacturers:
  - visual inspection of delivered elements of the device:
    - PCB manufacturing defects;
    - components placement on PCB;
    - soldering quality check;
    - mechanical enclosure manufacturing defects.
  - DC electrical measurements of delivered PCBs:
    - PCB connection to power supply;
    - measurements of low voltages generated on device, when powered on;
- on assembled devices:

    - visual inspection of assembled devices.
- automated functional tests of devices connected to test setup:
    - ethernet communication with XT-Pico;
    - complete tests of functions embedded in XT-Pico firmware;
    - output spectra analysis:
        - with interlock off;
        - with interlock on.

Results of all completed tests and measurements will be contained in final manufacturing report.