Towards final BCM firmware and interface to MPS

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BCM machine protection functions

The following machine protection functions have already been defined and agreed through discussions with the MPS group:

- Too-high beam currents
- Errant beams
- Inconsistent pulse rate
- Inconsistent pulse length
- Differential current interlock

Extra machine protection functions (optional):

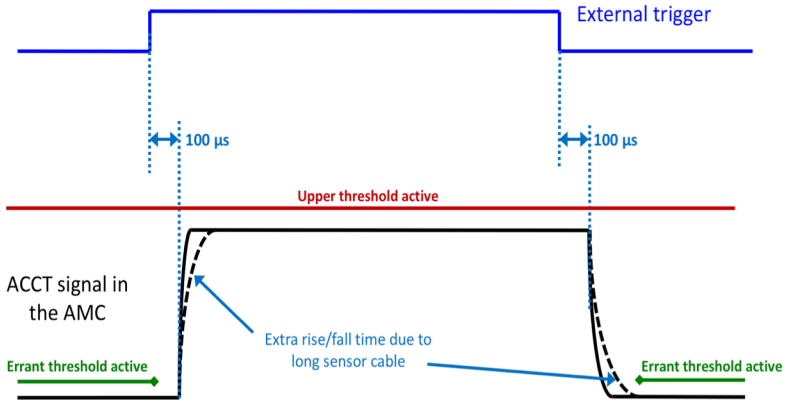
- Too low beam currents
- Trigger width too short

Protection functions on the BCM digitizer board:

- ADC stuck
- ADC clock missing
- Optical link errors

Not fully defined yet:

- Protection of the insertable devices



References for BCM machine protection

- BCM HW/FW/SW specifications document: '**LEBT upgrade ACCT firmware, software and hardware specifications**' (close to final)
- Machine Protection Features of the ESS Beam Current Monitor System: IPAC'18 paper **WEPAF088** (co-authored with the MPS group)
- Concept and Scope for Beam Current Monitor use for Machine Protection: ESS-**0178171** (released)
- MP requirements on ACCTs: **ESS-0105300** (preliminary)
- BCM system and FBIS ICD: **ESS-0105298** (preliminary)

BCM FW versions

- BCM FW from 2013 (FW by U. Legat from Cosylab):
  - Currently being used for the ISrc and LEBT ACCTs
  - Readout from max 2 ACCTs
  - Includes baseline level correction, droop compensation and digital filtering
  - Pulse shape display, measurement of pulse charge and baseline level
  - No machine protection function

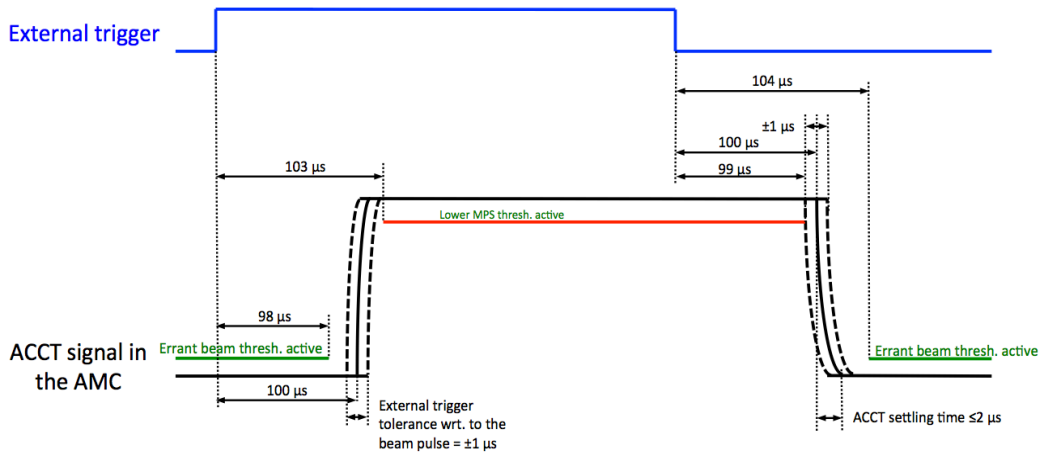
- BCM FW from 2017 (core FW by M. Werner from DESY + integration FW by M. Mohammadnezhad)
  - Intended for the warm linac (i.e. ISrc, LEBT, RFQ, MEBT and DTL)
  - Readout from max 10 ACCTs
  - Includes ACCT calibration
  - Timing and FBIS interfaces (not fully operational yet)
  - Several protection functions including those agreed with the MPS group
  - Differential current measurement using both local and remote (i.e. over optical fiber) ACCTs
  - Pulse shape display (raw and processed), pulse current/width/rate/charge measurements
  - Includes probe signals (very useful for test and verification)

- Full version (not available yet):
  - Intended for all the ACCTs including those in the super-conducting linac as well as the A2T and DmpL sections
  - Specifications are defined to a good extent but machine protection functions (ex. protection of insertable devices) are not fully defined yet.

BCM timing requirements

1. ADC clock (from EVR over backplane): 88.0525 MHz, locked to RF

2. Pulse trigger (from EVR over backplane): same width and frequency as the beam pulse; should be received by the BCM FPGA 100 us before the beam pulse.



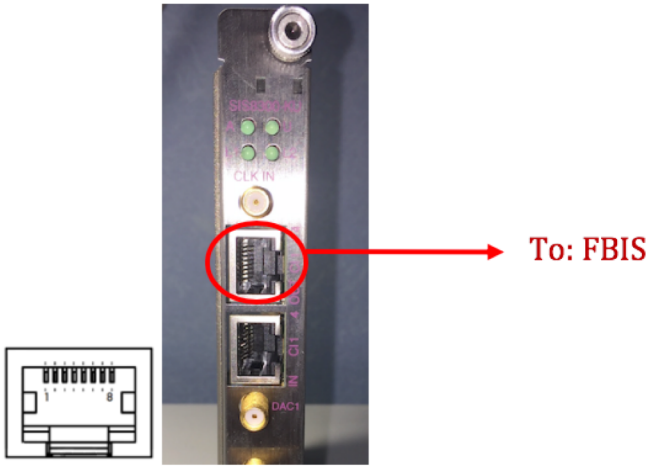
3. Beam mode (~~EVR over backplane~~ -> EPICS): pulse current, width and repetition rate; upon changing to a new beam mode, the BCM FW reads/sets new MPS thresholds corresponding to that mode (lookup table in the FPGA); mode no. and definition based on **ESS-0038258**

4. Destination mode (~~EVR over backplane~~ -> EPICS): beam destination

5. Calibration announcement (~~EVR over backplane~~ -> EPICS): ACCT auto calibration starts at a well-defined time after receiving the announcement.

BCM-FBIS interface

- The electrical and mechanical interfaces are defined in **ESS-0105298**
- The RJ-45 OUT port (LVDS) on the Struck SIS8300-KU is planned for the BCM-FBIS interface.
- The interface includes BCM_READY, BEAM_PERMIT as well as a Serial Data Link. The Serial Data Link will be used for sending redundant ready and beam permit signals plus other information including beam and destination modes.
- A prototype FBIS unit has been provided by the MPS group as is currently being used for the BCM/Timing/FBIS tests.



Differential ACCT pairs

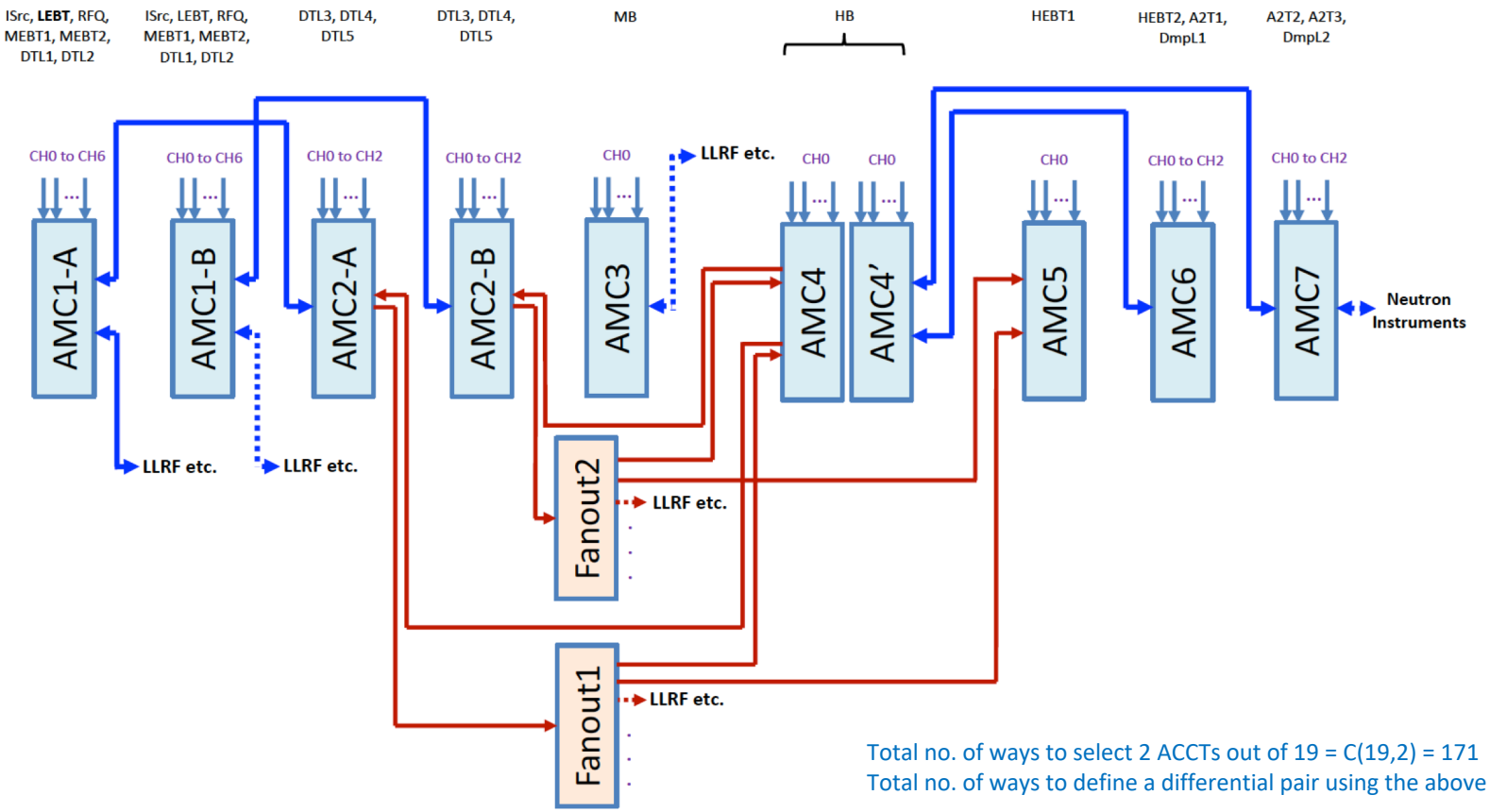
Critical ACCT pairs for machine protection as defined by the MPS group:

BCM A	BCM B	Comments	Required AMC connection
BCM before RFQ	BCM after RFQ	Required early on (during commissioning)	AMC1
BCM after RFQ	BCM after DTL		AMC1 - AMC2
BCM after DTL	BCM after medium beta		AMC2 - AMC3
BCM after DTL	BCM after high beta	Only to be made available after installation of the high beta cavities.	AMC2 - AMC4
BCM after medium beta	BCM before target		AMC3 - AMC7
BCM after medium beta	BCM before beam dump		AMC3 - AMC7

Considerations for differential current measurement with the BCM

- The ACCT distance in the critical differential pairs ranges from a few meters to more than 300 m.
- In the differential pairs where the two ACCTs are not connected to the same crate, a low-latency optical link will be used for sending the ACCT data from the upstream carte to the downstream one.
- A fine delay mechanism will be used to compensate the propagation delays of the differential pulses, hence avoid unwanted beam stops particularly during the pulse rise/fall times.
- In the differential pairs where the two pulses have different widths and/or different rise/fall times, the BCM FW deactivates the differential interlocks during short intervals around the pulse rise/fall times to avoid false beam aborts.
- The differential interlock consists of a fast (integration time of ~1 us), medium (integration time of ~100 us) and a slow (i.e. integration over the whole pulse width) algorithm to be able to detect large and sudden as well as small and persisting losses.

BCM optical cabling diagram

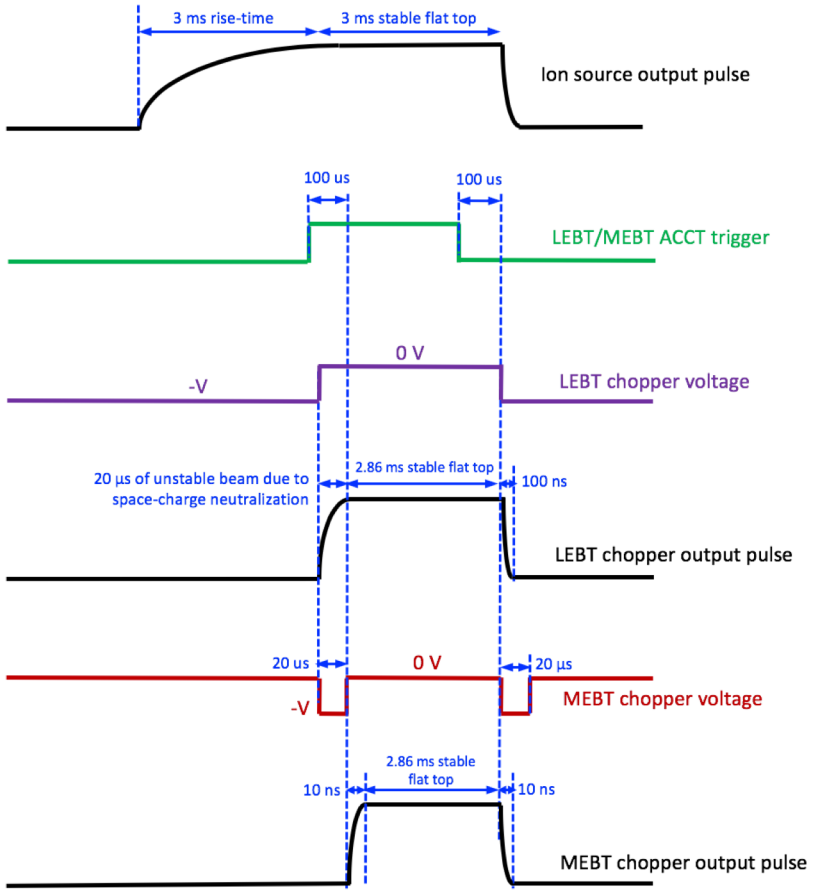


Total no. of ways to select 2 ACCTs out of 19 = C(19,2) = 171
Total no. of ways to define a differential pair using the above scheme = 57

↔ ⇠⇢	Full-duplex transmission using 'twin' optical cable
→ ⇢	Full-duplex transmission using 'single' optical cable
A	Main crate
B	Redundant crate
'	Extra AMC hosted by the same crate

RFQ and the MEBT chopper losses

- ‘Normal’ losses of the RFQ (up to ~30%) should be taken into account for all the ACCTs downstream to the RFQ.
- The MEBT chopper will cut off up to 20 us from the start of the pulse. The resultant pulse width difference should not then cause an unwanted beam abort in the differential pairs with one ACCT being upstream and the other downstream of the MEBT chopper.
- Special FW blocks are foreseen for the RFQ and the MEBT chopper. False beam aborts will be avoided by relaxing/disabling some interlocks during short time intervals.



Setup for Timing+FBIS+BCM tests

Mehdi Mohammadnezhad (consultant from SIGMA), Stephane Gabourin (MPS) and Javier Cereijo Garcia (Timing) are giving support for the test setup.

Interlock on too-high beam current

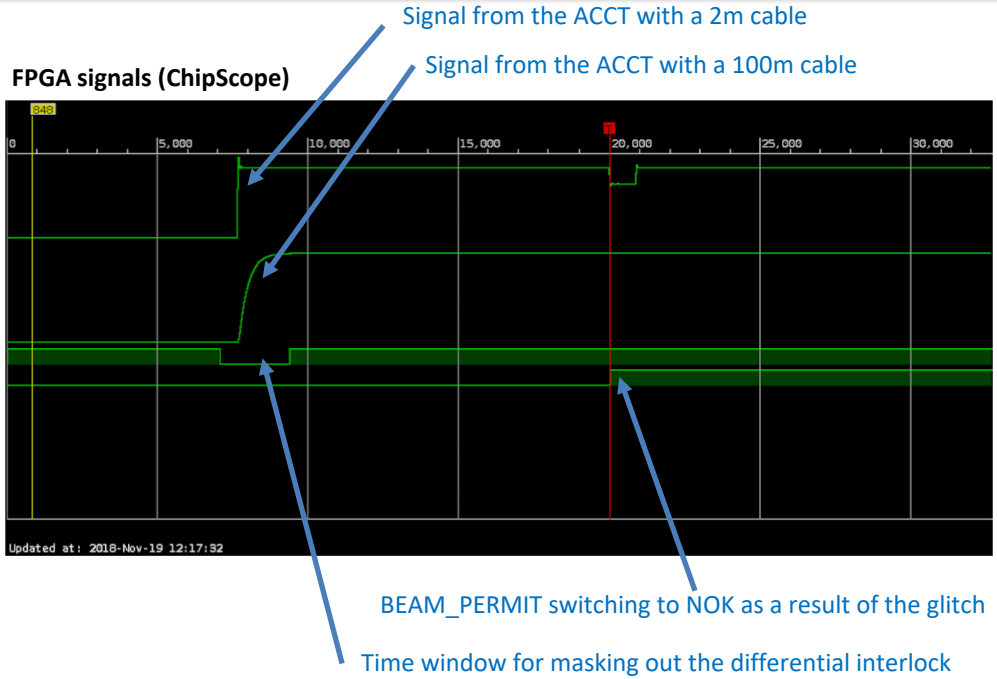
- The total BCM response time from the moment that the extra current (i.e. glitch) goes through the toroid until the moment that the BEAM_ABORT signal switches on the SIS8300-KU output port is measured at **1.02 us**.
- From the total delay 0.47 us is due to the toroid, ACCT cable and the FE unit.
- The agreed BCM response time with the MPS group is 1-2 us.

Interlock on errant and too-low beams

Interlock on errant beam

Interlock on too-low beam

Interlock on differential currents



- The differential interlock tests were done with the first ACCT cable being 2 m and the second ACCT cable being 100 m (about the worst case).
- The cable length difference causes a significant difference between the time constant of the two ACCTs, and that results in large negative/positive spikes in the difference signal at the pulse rise/fall times.
- Two time windows (fully configurable in the FW) are used to mask out the (false) interlocks at the pulsed rise and fall times.
- The difference in the arrival time of the two pulses in the downstream crate was compensated using a fine delay in the BCM FW.
- The FPGA adds very small delay (only a few clock cycles) to the differential interlock response time (including the optical fiber link) compared to the interlocks on a single ACCT sensor.

Issues / next steps

- Support from ICS needed for the new BCM IOC, EPICS integration and GUI (kick-off meeting planned on Nov. 22nd).
- A few small bugs in the BCM FW were identified and fixed during the tests.
- EVR in the second crate not operational yet (needs new EPICS environment from ICS – work in progress).
- Serial Data Link not fully operational yet (work in progress).
- Destination mode information from the Timing System and interlock masking in the BCM FW (based on a selected destination mode) not fully operational yet (work in progress).
- Optical fanout module needed to fully test/verify the optical cabling scheme including future BCM signal transmission to other systems.