

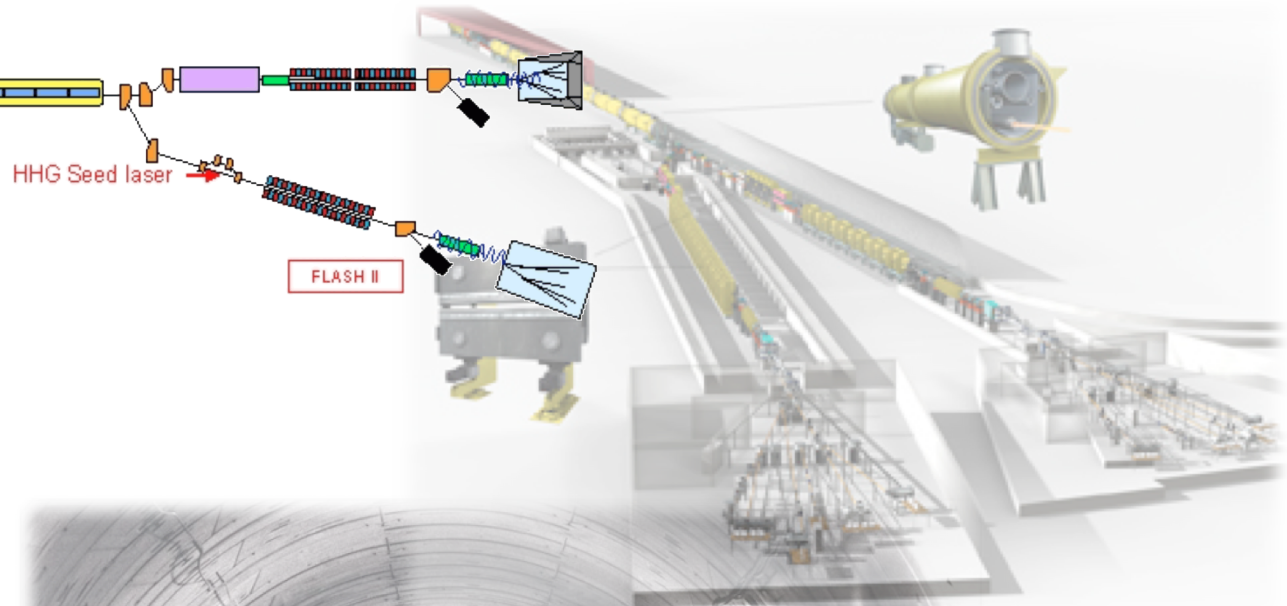
XFEL-MPS

Machine Protection for XFEL and FLASH II

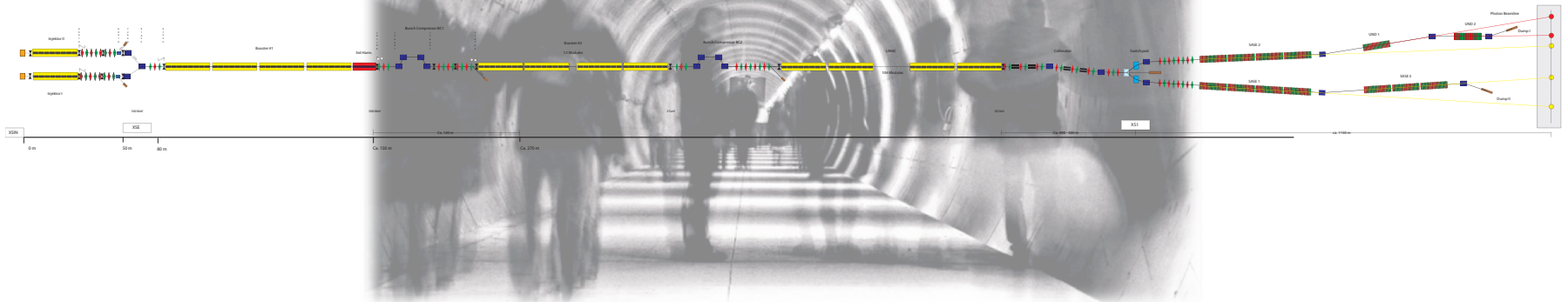
PLC Workshop Lund, 29.-30.08.2013



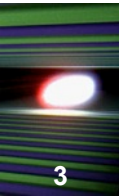
FLASH 2 and XFEL accelerators



Overall length
FLASH: 500m
XFEL: 5.4 km

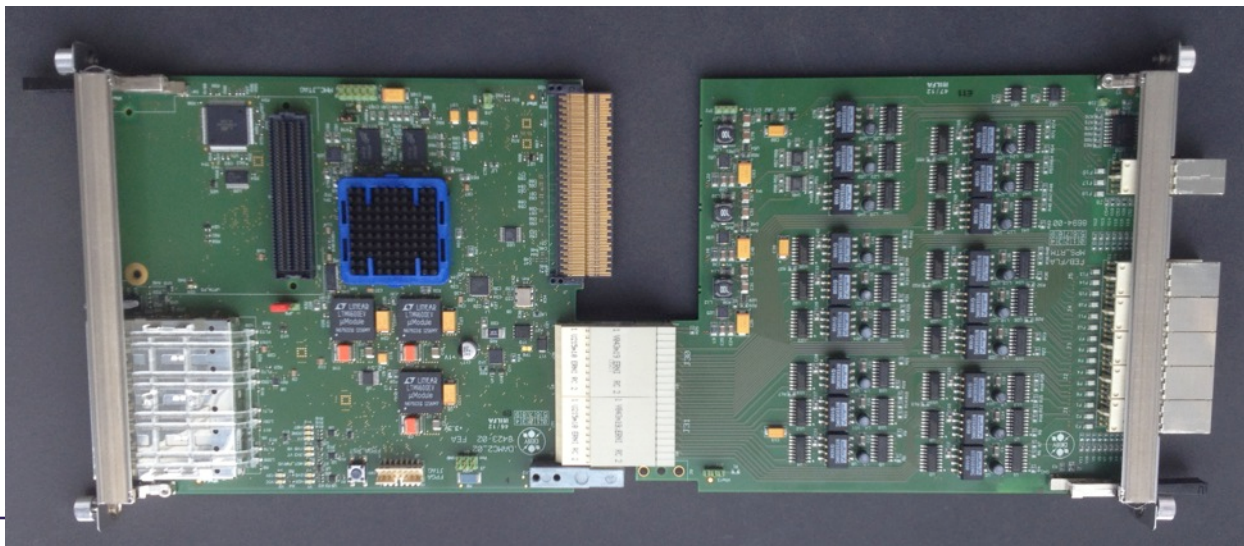
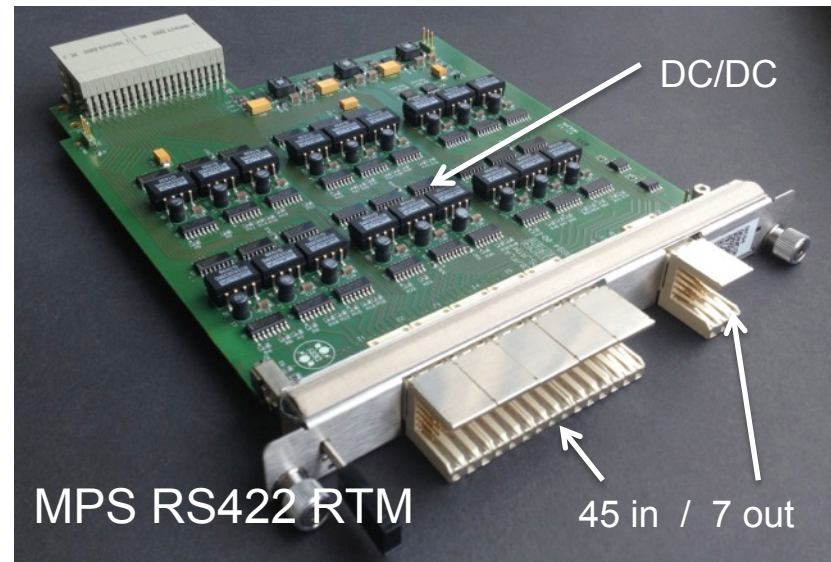
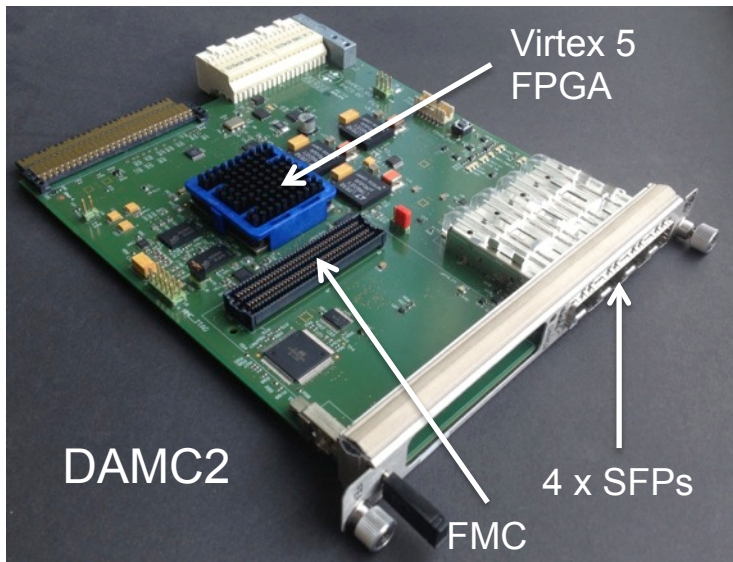
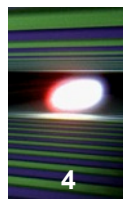


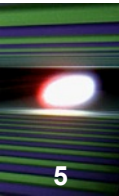
Why no PLC for MPS in XFEL and FLASH2?



- Speed
- Same technology everywhere in XFEL
- Same Hardware
- Homogenous general concept
- μ TCA technology
- Maintenance must be easy (μ TCA advantages)
- No distinction between fast and slow inputs, same priority for all
- Remote FPGA maintenance via IPMI bus (I²C) or PCIe

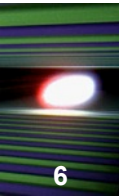
μTCA components



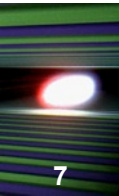


- Scalable
- same firmware in every DAMC2
- Every DAMC2 slave holds all information of all prior connected slaves (debugging)
- Every slave can be connected to the timing system
- Configurable – NOT programmable
- Every slave can hold one I2C driven FMC Dosimetry board
- Stand alone system, independent from control system
- Calculation of thresholds (analog / digital) are done outside MPS in connected systems

General MPS features at DAMC2

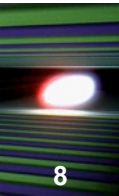


- 45 RS422 external input channels, 100 ns min. alarm signal length
- 3 internal input channels for FMC and Backplane alarms
- 7 RS422 output channels
- I2C support to FMC
- 4 SFP I/O fiber optic lines (0-4 Inputs, 0-4 outputs)
- Addressable up to 64 Sections, each equipped with 64 DAMC2 MPS modules
- Fast internal RS422 link from in- to outputs
- Debug Register
- LED status indicator (heart beat, server connection, initialization)
- Settings checked by DOOCS server



- Options for each input channel:
 - Enable / disable inputs
 - Test input
 - Check functionality of connected systems between Macro Pulses
 - Pulse counter within a given time, both configurable
 - Beam Mode generation
 - Section Pattern generation
 - Alarm Type generation
 - Save each Alarm into DOOCS history

Output Channel MPS features

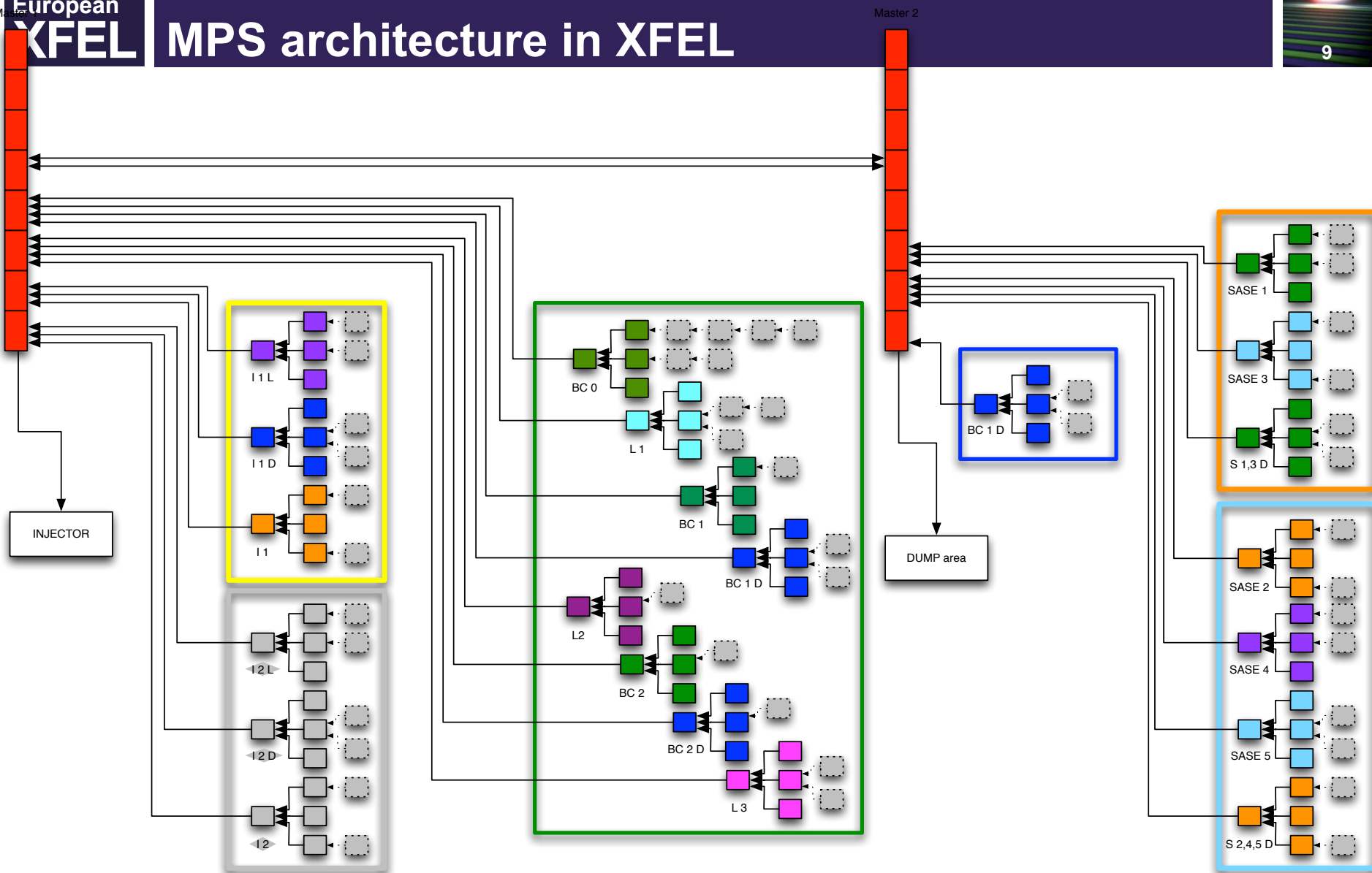


- Options for each output channel:
 - Enable / disable
 - Test output
 - Fast output line configuration on same DAMC2 board
 - Save each action into DOOCS history

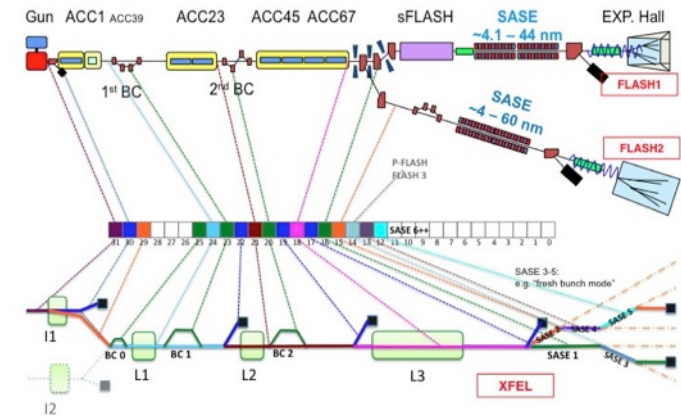
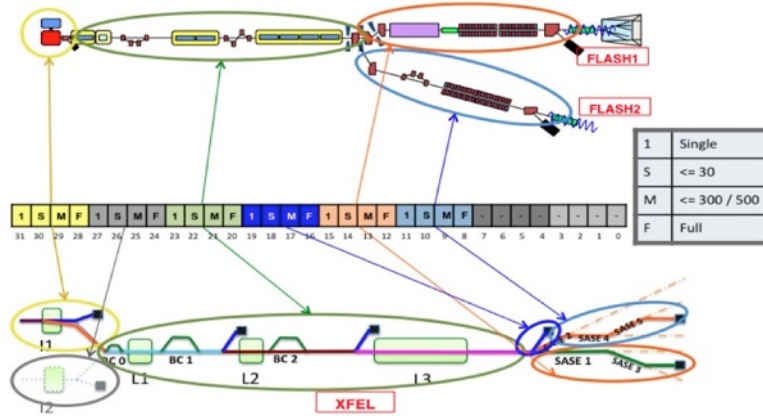


MPS architecture in XFEL

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Information structures, protocol priority, pre-processing



Beam Modes

63-52	51	50-48	47-40	39-32	31-0
Sec 63-58	Addr 57-52	CNT	spare	ALARM Type	BEAM Modes
FFF	P	3	8 bit	8 bit	32 bit
12 (6+6)	1				

Section Pattern

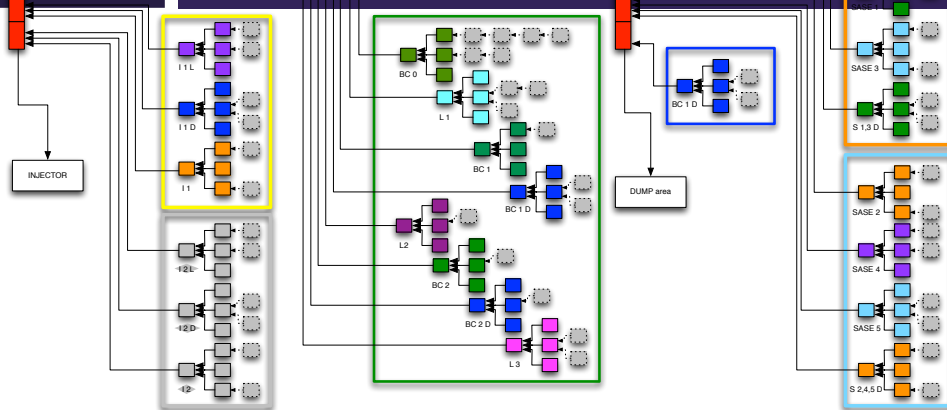
63-52	51	50-48	47-40	39-32	31-0
63-58	57-52	CNT	spare	spare	SECTION PATTERN
FFE	P	3	8 bit	8 bit	32 bit
12 (6+6)	1				

Slave Info

63-52	51	50-48	47-0
63-58	57-52	CNT	single SLAVE information
000 - FFD	P	3	48 bit
12 (6+6)	1		

How it works, priority protocols

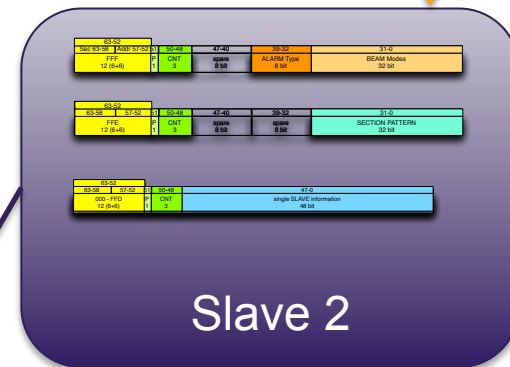
11



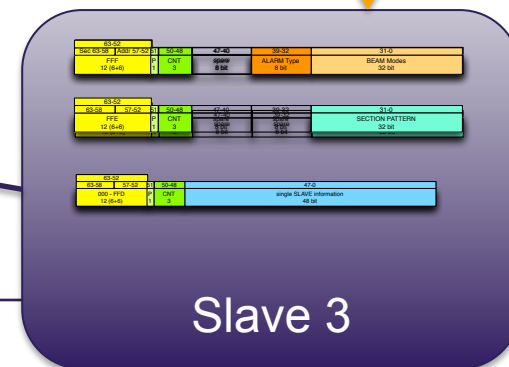
S. Karstensen Created on Fri Feb 08 2013 Modified on Mon Aug 19 2013

- 1.) Beam Modes **very high**
- 2.) Section Pattern **high**
- 3.) Slave info **low**

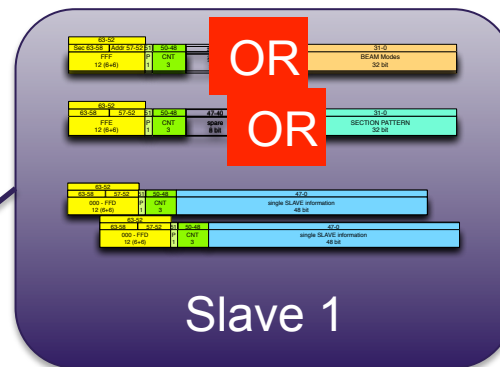
Alarm



Alarm



Slave 3

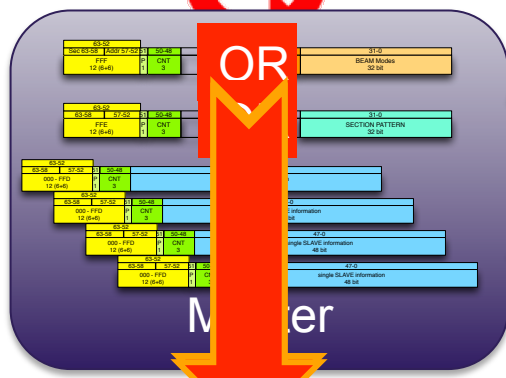


Slave 1

timing



OR



Master

ALARM out

Configuration Panel for FLASH 2

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mps_flash2_main_static_config.xml

Static Config - FLASH2 - μ TCA MPS

Slave 4 Slave 3 Slave 2 Slave 1 Master

Input names: Inputs enabled: Input simulations: Inter-macro-pulse checks: Check count time resets: Input flicker counter thresholds: Flicker counter window size: Fast lane out/ config: Alarm transfer config: Beam Modes bit config: Section Pattern bit config:

0 7 15 23 31 39 47

BLM018 BLM019 CnvOK012 DOSI012 0 DOSI012 1 DOSI012 2

TPS012 0 TPS012 1 TPS012 2 TPS012 3 TPS012 4 TPS012 5

BPM023

Board reset!

States

- Reset pending
- Initial config uploaded
- Config changes uploaded

Status

- PCle communication
- Firmware conformity
- FPGA memory

Acknowledge

OK!

Out/ names: 50K013

Out/s enabled:

Digital outputs

Out/s:

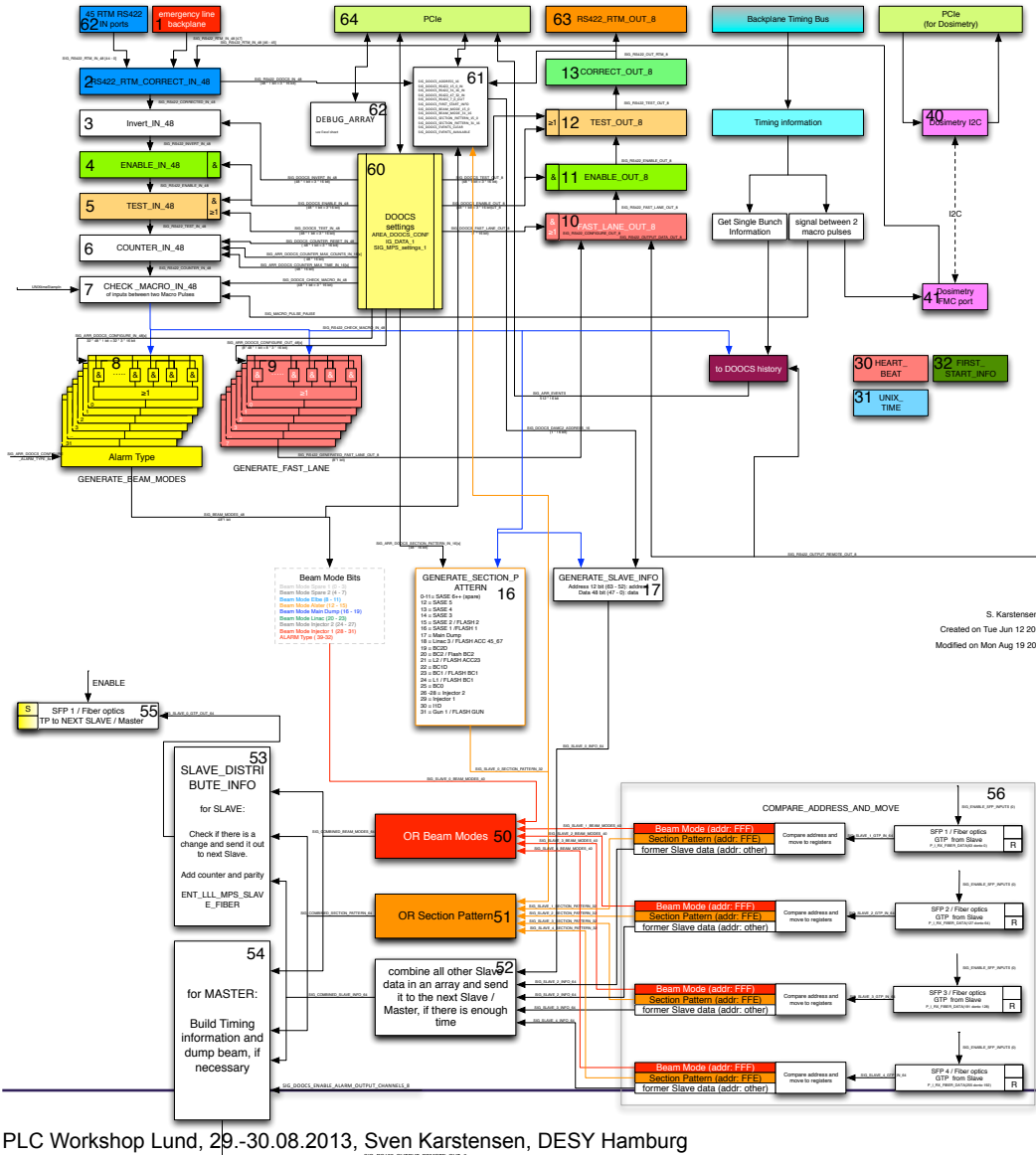
Beam Modes output

Section Pattern output

Offset: 0

MPS program architecture

MPS SLAVE structure



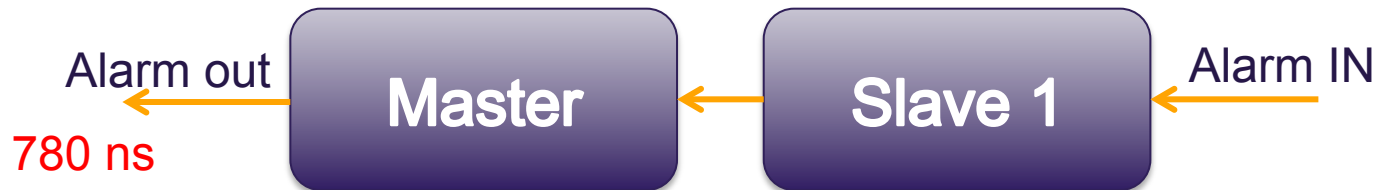
- Numbers in drawing corresponding to chapters in FPGA code
- Excel Sheet includes all addresses

Latency (August 2013)

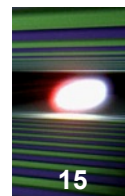
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Fiber optics: unattended (5 ns/m)
Speed: 1.25 GBps

Latency between Master and
Slaves will be improved.
Factor 3 is aspired.



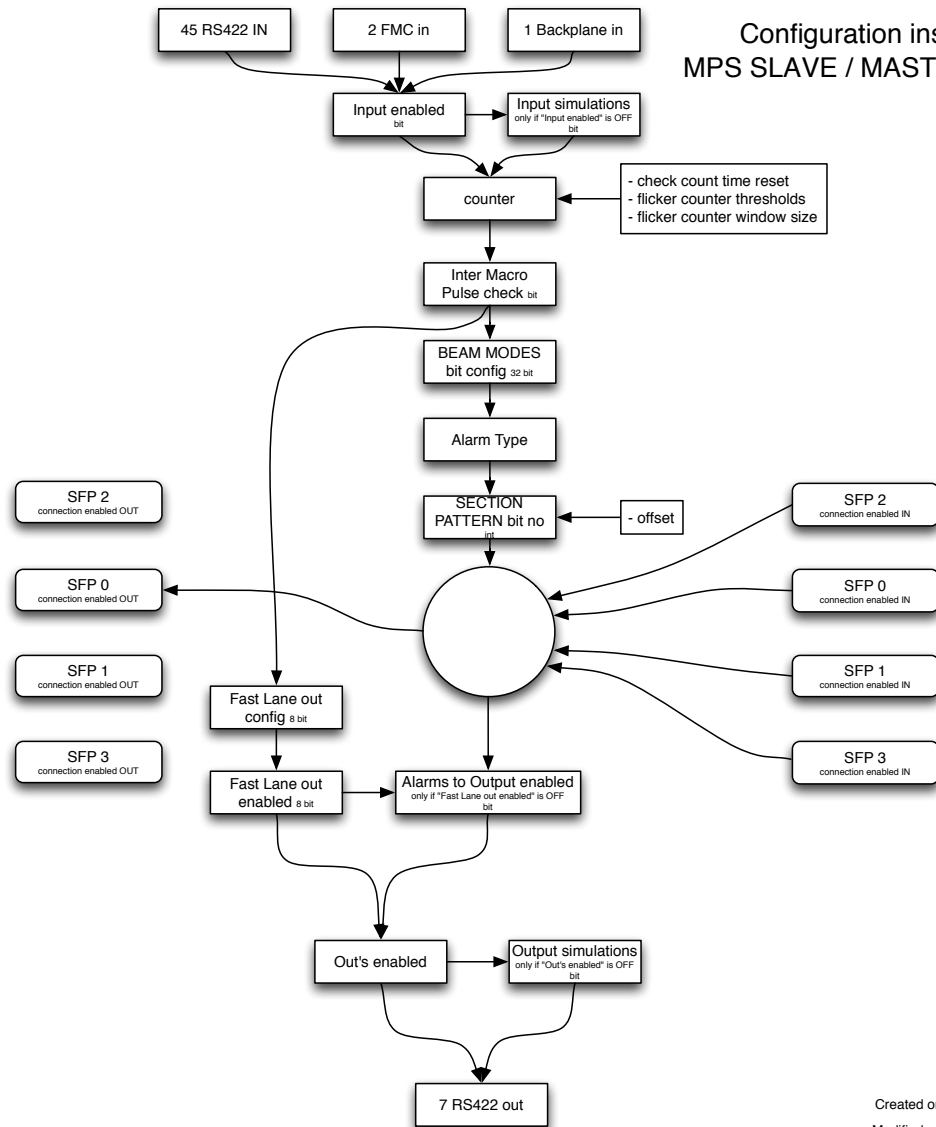
Reaction Times in XFEL



Beam loss location	Distance from injector	Distance from dump	# of lost bunches
Injector	0 m	-1970 m	0
BC1	160 m	-1810 m	7
BC2	360 m	-1640 m	15
Linac center	1040 m	-930 m	44
Linac end	1650 m	-320 m	69
Beam distribution	2010 m	40 m	2
Last undulator	3010 m	1040 m	44

- ~ 50 bunches are inside accelerator
- Signal transport from dump to injector 20 μ s (2000m)
- ~ 50 bunches generated before laser is blocked
- Using beam dump kicker reduces the number of lost bunches inside SASE undulator sections.

Configuration Instruction



S. Karstensen

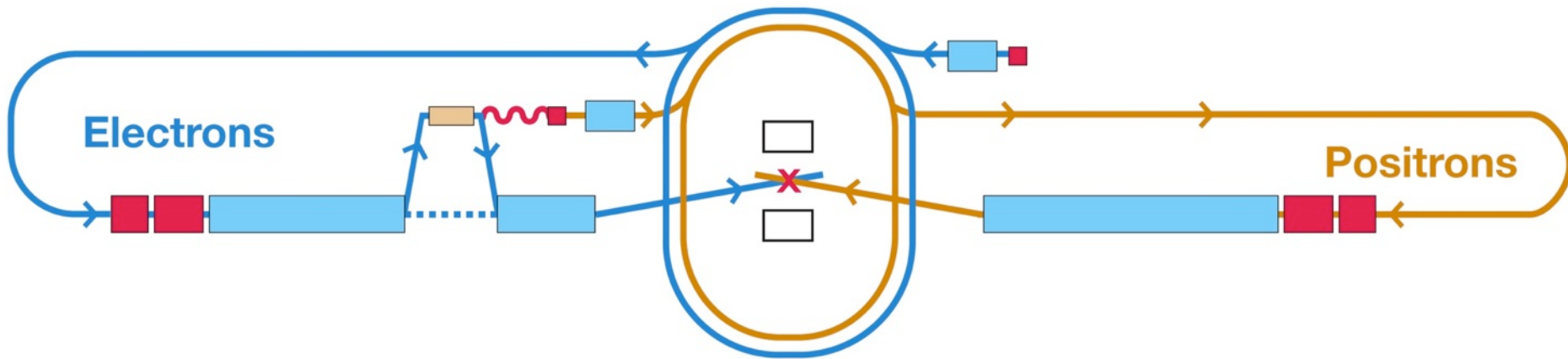
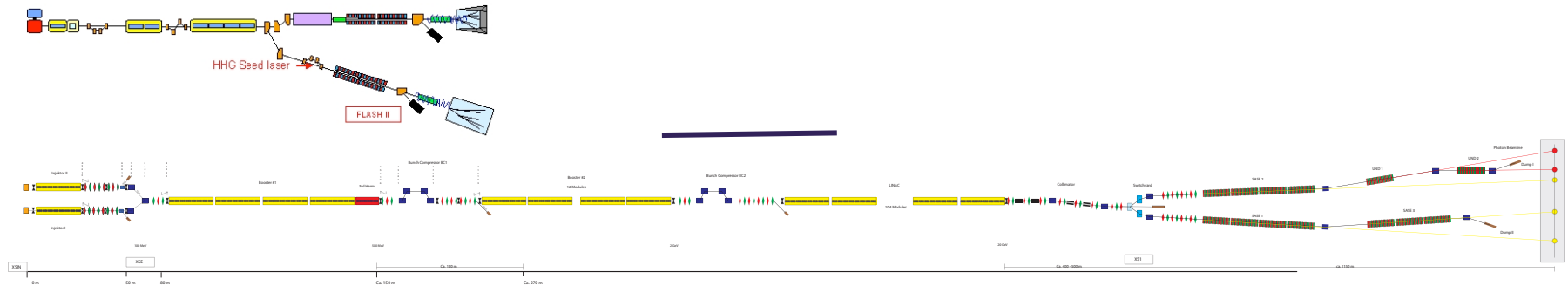
Created on Fri Aug 23 2013

Modified on Wed Aug 28 2013

FLASH II, XFEL, ILC

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scalability



Thank you

