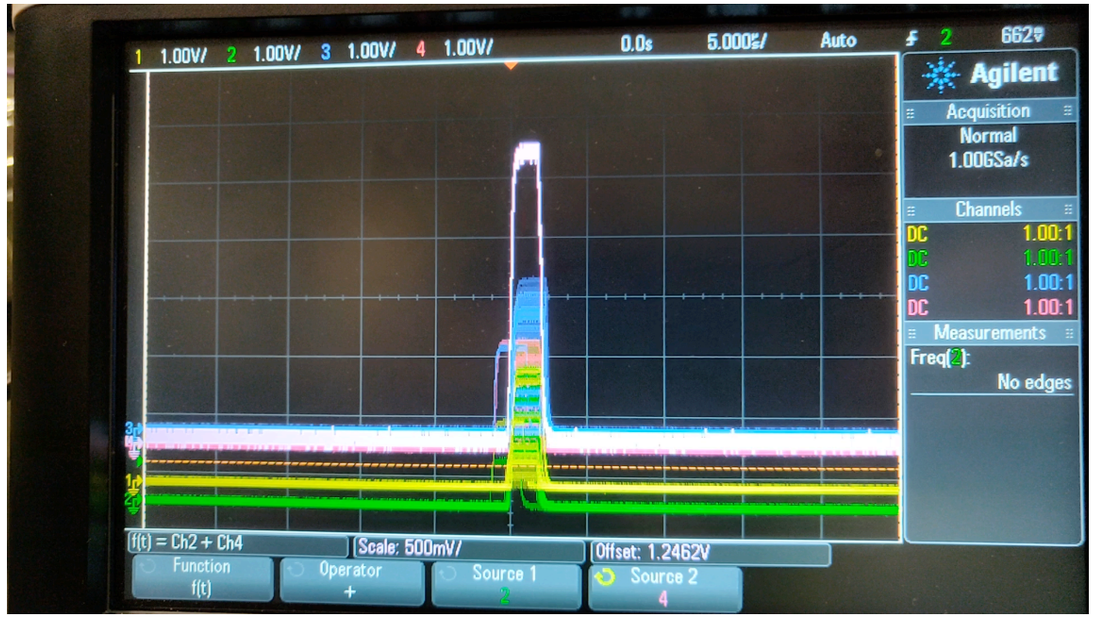
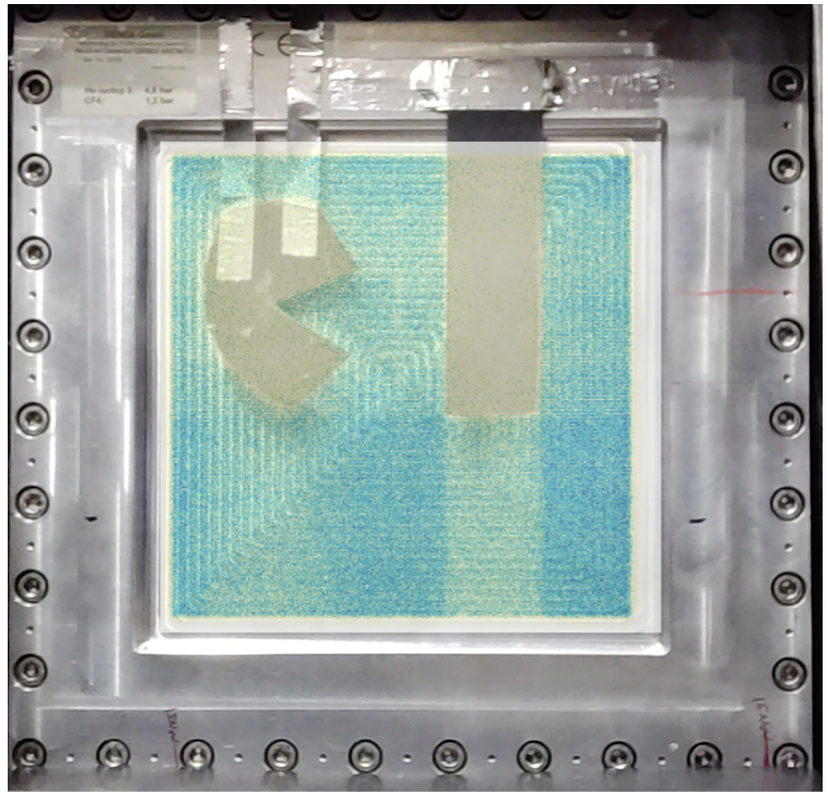
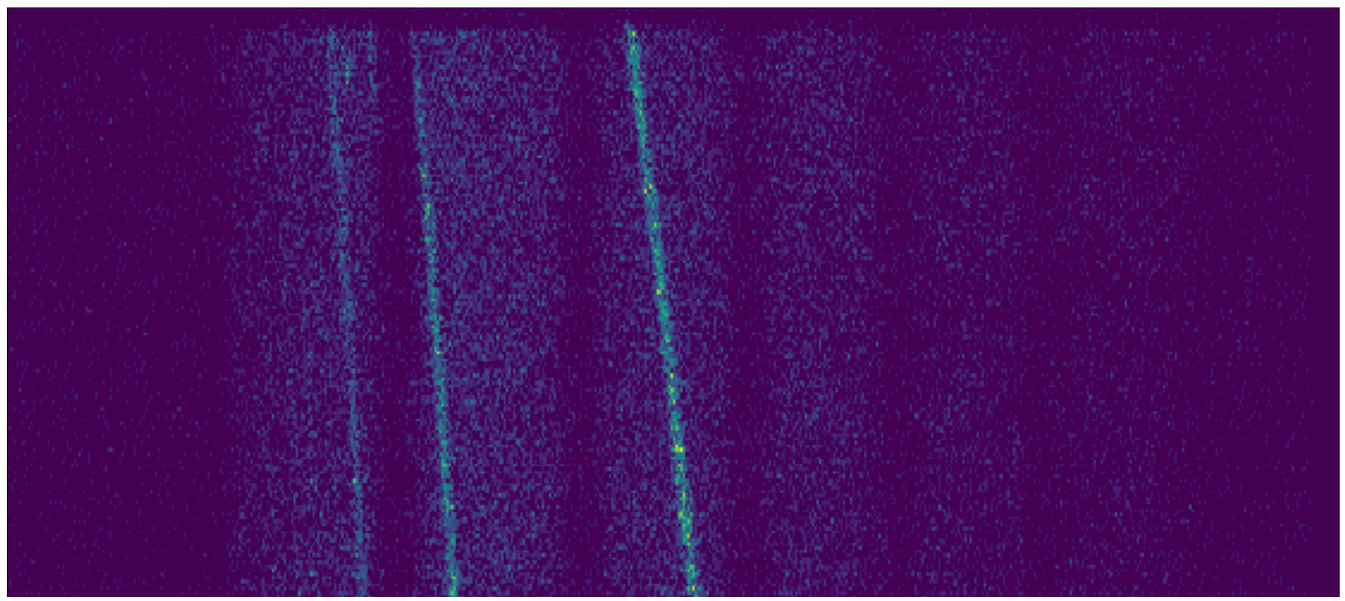
EPICS Control - Lessons from V20 and Way Forward

HZB V20 Results

Data processing pipeline from start to finish

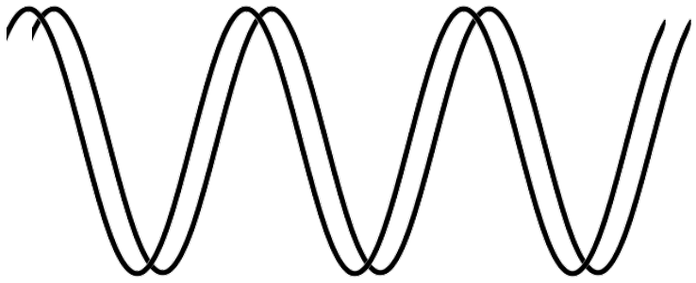






Success!

Lessons learned from V20 test



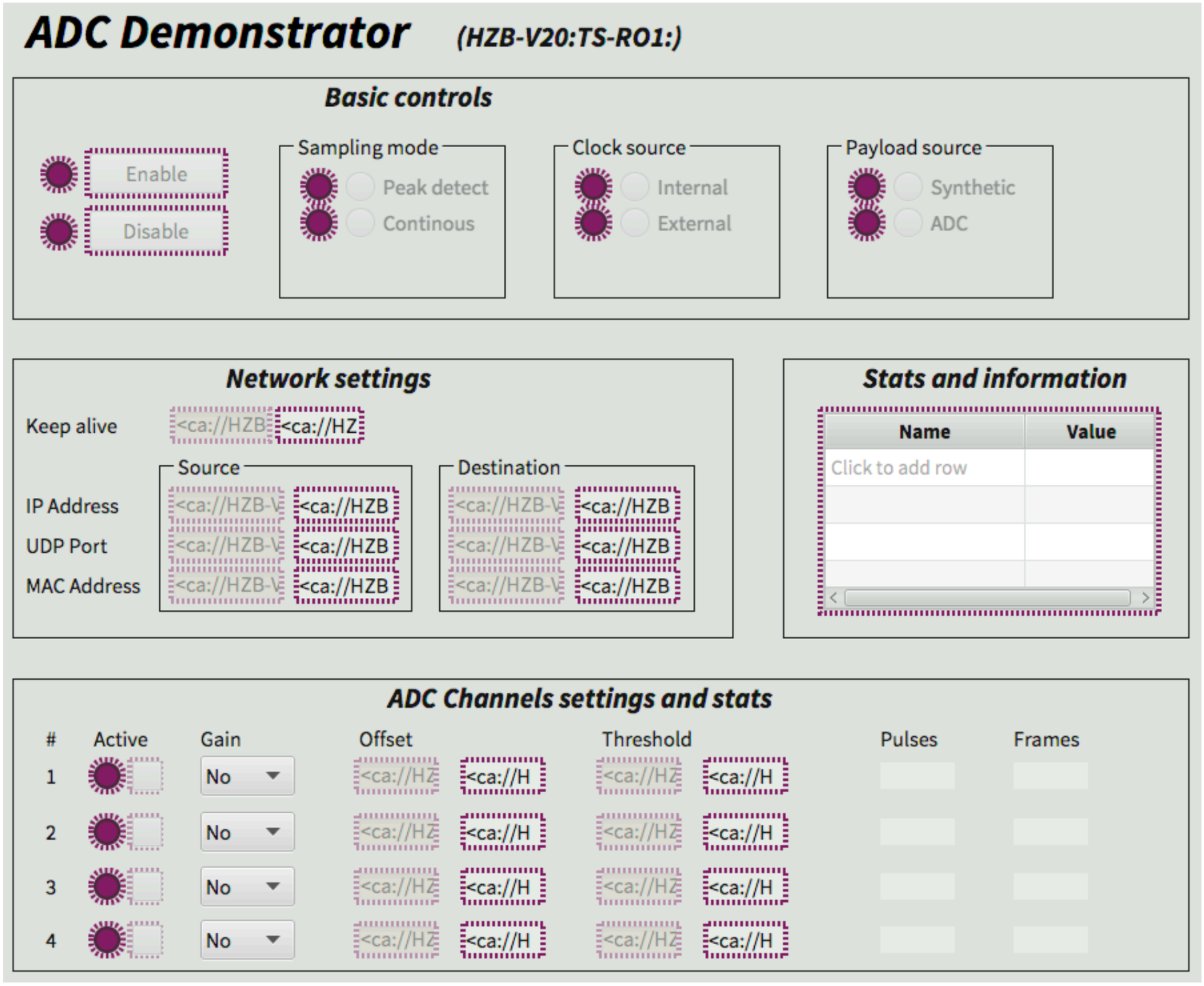
- We need a good EPICS interface for control/configuration of readout system
- We need to be able to verify that the readout hardware is synchronised to the timing system
- We need to be able to test the readout system without access to the timing system

Configuration of the FPGA

```
0 git_hash LW
1 build_time TIME
2 device_id_h LW
3 device_id_m LW
4 device_id_l LW
5 loopback LW
6 rst_vec LW
7 adc_chsel LW
8 adc_dec LW
9 adc_bypass_zs LW
10 adc_thresh_0 LW
11 adc_thresh_1 LW
12 adc_thresh_2 LW
13 adc_thresh_3 LW
14 adc_rhold_b2 LW
15 adc_fhold_b2 LW
16 adc_sampsb_b2 LW
17 adc_sampsa_b2 LW
18 adc_mingap_b2 LW
19 eth_src_mac MAC
21 eth_dst_mac MAC
23 ip_src_addr IP
24 ip_dst_addr IP
25 udp_src_port LW
26 udp_dst_port LW
27 pkt_timeout LW
28 ch0_gain GAIN
29 ch1_gain GAIN
30 ch2_gain GAIN
31 ch3_gain GAIN
32 ch0_offset OFFSET
33 ch1_offset OFFSET
34 ch2_offset OFFSET
35 ch3_offset OFFSET
36 adc_spi LW
37 si570_base LW
38 si570_data LW
39 si570_trig LW
40 led_sel LW
41 pulse_cnt_01 LW
42 pulse_cnt_23 LW
43 frm_cnt_01 LW
44 frm_cnt_23 LW
45 pkt_cnt LW
46 ch01_snap LW
47 ch23_snap LW
48 status_0 LW
49 status_1 LW
50 status_2 LW
```

- ~50 registers
- ~50 functionalities
- Recent improvements to EPICS interface

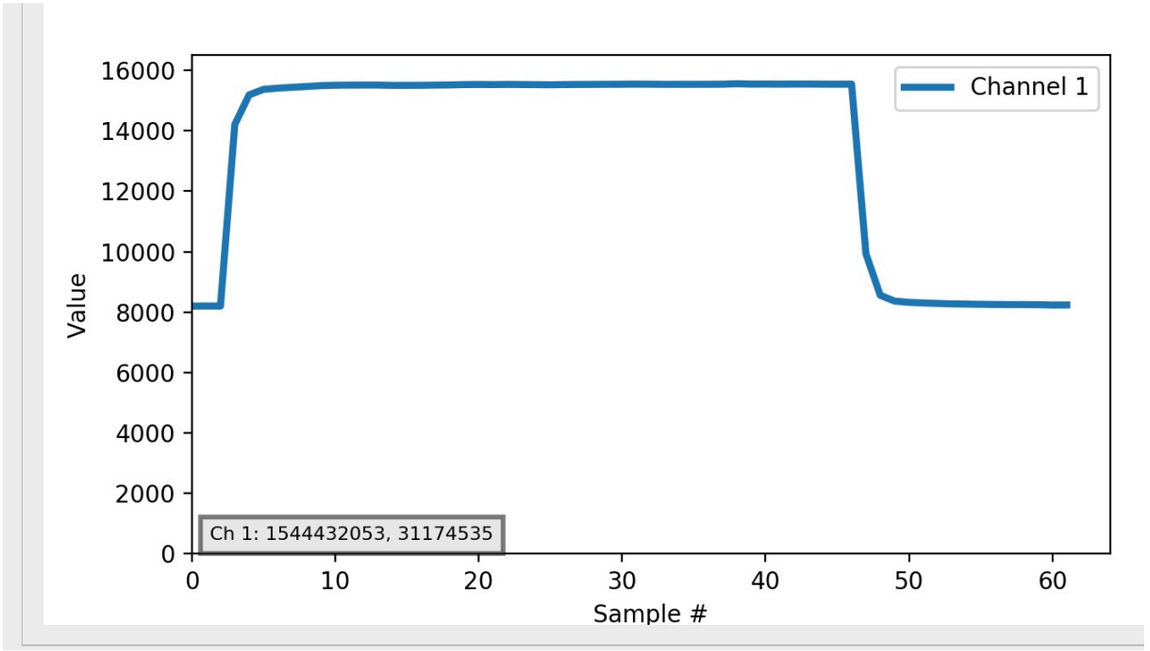
Configuration of the FPGA



Time synchronisation

Test at HZB

Event time:
2018-12-10
08:54:13.708082916

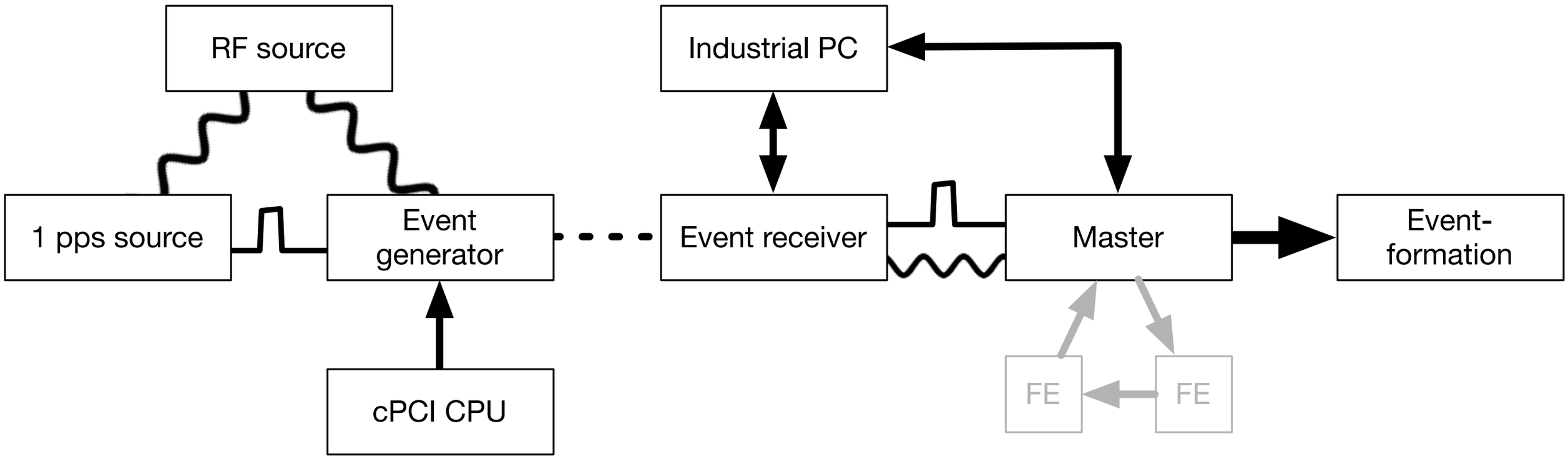


1. Pulse analog input of ADC using EVR
2. Determine timestamp of pulse at EVR
3. Determine timestamp of pulse at ADC
4. Compare timestamps

- Result: The ADC ***might*** have been ~7 µs out of sync with the timing system

Time synchronisation

Possible failure locations



Requirements for future tests

- Use internal oscillator without updating the firmware
- Update time counter without access to timing hardware
- We need to be able to test the readout system without access to the timing system
- Minimal to no set-up should be required to get the system up and running