NBLM CONTROL SYSTEM DESIGN

VERSION-2.0 2019/02/01

	REDACTEUR ***Edited by***	**VERIFICATEURS** ***Reviewed by***	**APPROBATEUR** ***Approved by***
NOM Prénom ***Name***	Victor Nadot Yannick Mariette Quentin Bertrand	Françoise Gougnaud Thomas Papaevangelou Laura Segui Tom Joannem	ESS-ERIC
Date et signatures ***Date and visas***			

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V1.1	2018/01/11	Mariette	4.4/19	Adding remark
V1.2	2018/05/18	Mariette/Nadot	All/All	Adding acronyms in the table. Specifying the scope, the context. Adding a document in “Related documents”. Removing “Distribution” chapter. Chapter “FPGA firmware specification” is renamed in “FPGA firmware specifications (neutron detection algorithm only)”. This chapter has completely been re-written. Removing sub-chapter “FPGA interfaces” in this chapter.
V2.0	2019/02/01	Mariette/Nadot/Bertrand	All/All	Renaming and updating the document to only keep the Control System scope (no firmware specification)

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1. Introduction

1.1. Purpose

This document describes the design for the neutron sensitive Beam Loss Monitor (nBLM) control system.

1.2. Scope

CEA ESSI is in charge of supplying the control system of nBLMs and the first version of FPGA specifications for the neutron detection.

First FPGA specification has been delivered with the document [8]. Since these document release, the neutron detection specifications has been completed and integrated in the ESS ERIC document [9].

So this document only describes the design of the nBLM Control System.

1.3. Abbreviations, acronyms and definitions

Name or acronym	Definition
ADC	Analog to Digital Converter
ADU	Analog to Digital Unit
AMC	Advanced Mezzanine Card
API	Application Programming Interface
BEE	Back-End Electronics
BI	ESS Beam Instrumentation department
BIS	Beam Interlock System
BOY	Best OPI, Yet
CA	Channel Access
CEA	Commissariat à l'Energie Atomique
CSS	Control System Studio
CU	Cooling Unit
DMA	Direct Memory Access
DOD	Data On Demand
E3	New ESS EPICS Environment
EEE	ESS EPICS Environment
EMMC	Enhanced Module Management Controller
ESS	European Spallation Source ERIC
EPICS	Experimental Physics and Industrial Control System
ESSI	ESS Irfu project
FEE	Front-End Electronics
FPGA	Field Programmable Gate Array
GUI	Graphical User Interface
HEBT	High Energy Beam Transport
HV	High Voltage
HWR	Half Wave Resonator

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I/O	Input / Output
ICS	Integrated Control System
IOC	Input Output Controller
LCS	Local Control System
LINAC	Linear Accelerator
LV	Low Voltage
MCH	MTCA Carrier HUB
MCMC	MicroTCA Carrier Management Controller
MEBT	Medium Energy Beam Transport
MMC	Module Management Controller
MPS	Machine Protection System
MPV	Most Probable Value
MTCA	Or µTCA: Micro Telecomunications Computing Architecture
nBLM	neutron sensitive Beam Loss Monitor
OPI	OPerator Interface
PDR	Preliminary Design Review
PM	Power Module
PV	Process Variable
RTM	Or µRTM: Rear Transmission Module
SAR	System Acceptance Review
SoW	Scope of Work
TBC	To Be Confirmed and/or yellow highlight
TBD	To Be Defined and/or yellow highlight
TBW	To be Written and/or yellow highlight
TOT	Time over threshold

1.4. Related Documents

	Name of reference document	ESS reference
[1]	nBLM Project PDR1.1	CHESS, ESS-0087794, 2016
[2]	nBLM System PDR1.2	July 2017
[3]	ESS CEA IKCA – Schedule AIK 7.9	CHESS, ESS-0052571, 2016
[4]	ESS_IKC_BLM_Control_2017-10-04	
[5]	nBLM system risk analysis	
[6]	Modes covered by nBLM system	
[7]	Requirements for nBLMs control	
[8]	“nBLM Control system design and neutron detection specifications” version-1.2 2018/05/18	
[9]	ESS-0044364-nBLM-specs-v4.0_15.01.2019.pdf	https://jira.esss.lu.se/browse/BIG-1245
[10]	nBLM Firmware – Software Interface	https://confluence.esss.lu.se/display/HAR/nBLM+Firmware+-+Software+Interface#nBLMFirmware-SoftwareInterface-Circularbufferparameters
[11]	180613SDREVB CEA SACLAY MAIN RACK RACK C.pdf	
[12]	nBLM_CDRfinal_ReportTests2.docx	

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1.5. Context

ESS is a proton accelerator. Fast neutrons are generated when the proton beam interacts with the matter, thus the neutron rate gives a measurement of beam loss.

The beam loss measurement is mandatory in order to:

- Ensure the accelerator security with a fast beam stop in case of a beam loss accident
- Contribute to human safety with a low level line activation (<1 W/m)

The purpose of an nBLM detector is to be sensitive to fast neutrons and insensitive to unnecessary X and γ rays and thermal neutrons.

An nBLM detector could be a “fast” detector or a slow “detector”, the packaging (polyethylene for the slow detector) is different. From the CS view there are no difference.

The nBLM detector is a Micromegas detector as defined in documents [1] and [2]. It is a gaseous detector with a gas chamber. There is one input and one output for the gas (He+10%CO2) for each detector.

Each Micromegas detector also needs to be powered with 2 high voltage inputs, thus 2 high voltage channels are needed per nBLM detector.

Moreover the preamplifier in the FEE for a nBLM detector needs to be powered with low voltage.

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2. Hardware description

2.1. Facilities and interfaces overview

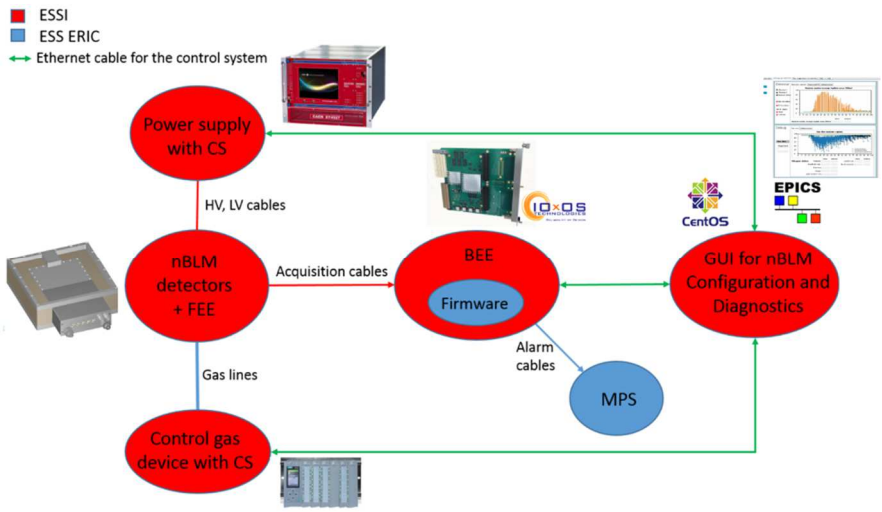

Figure 1: Facilities and interfaces overview for one nBLM

Remark: The FPGA firmware development inside the BEE is not in the scope of ESSI

2.2. Hardware devices involved in the nBLM control System

The Control System must manage the slow control of the HV, LV, and gas devices. It also manages the FPGA settings and acquisition.

2.2.1. Hardware architecture for the gas control

Monitoring/PLCs/instrumentation architecture for the gas is divided into 3 subsets: Gas Storage (GS), Gas Distribution (GD) and Gas DTL Line (GDTL).

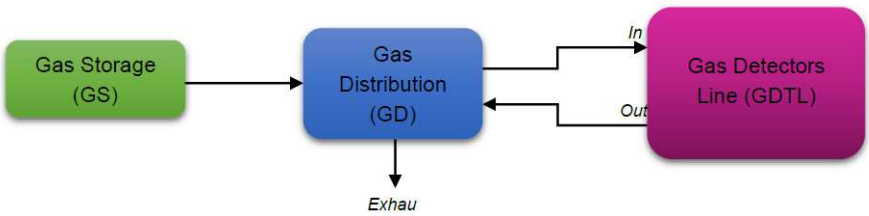

Figure 2 : Gas subsets

The hardware architecture complies with ESS standard devices:

- Siemens S7-1500 CPUa
- Siemens Input/output cards
- Siemens ET200SP remote I/O

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These devices, sensors and valves are set in 3 distribution chassis and 1 main chassis (see the figure below).

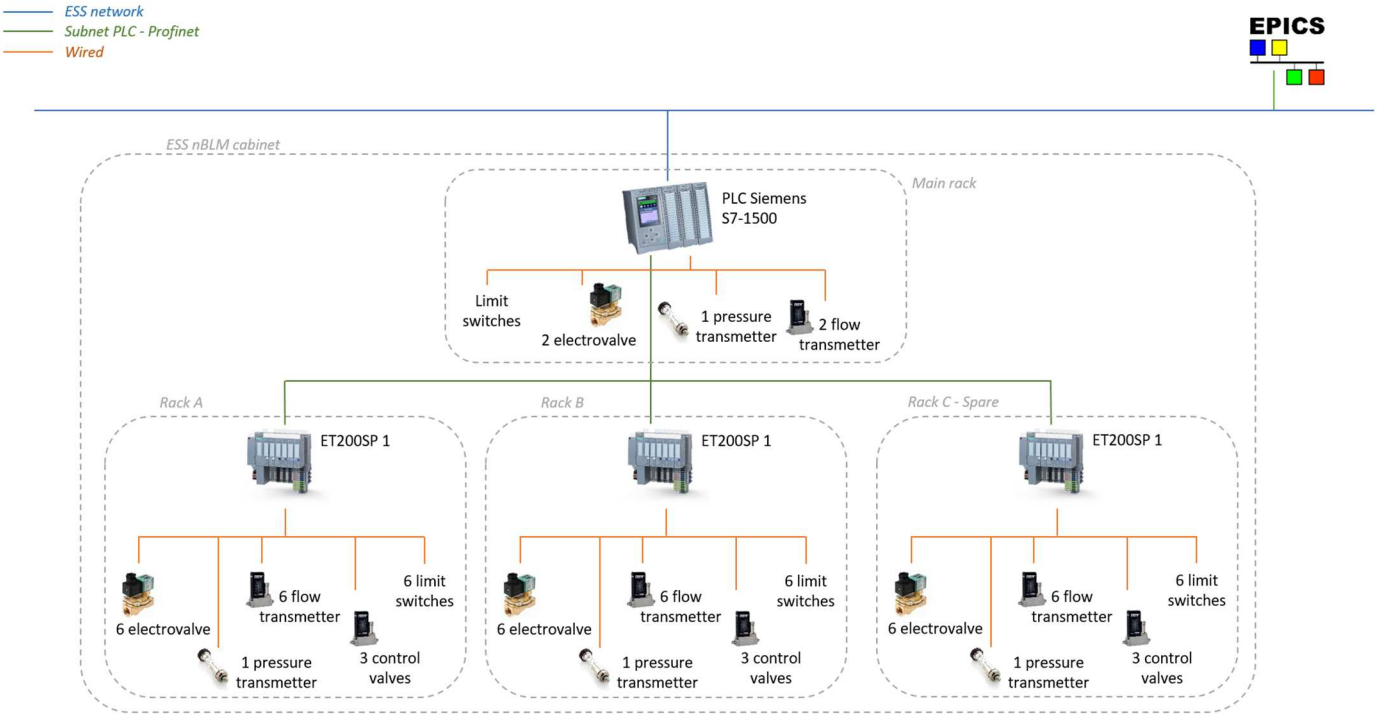

Figure 3: Gas devices architecture

Input cards acquire the sensor pressure values and valves limits switches. Flow valves are controlled by digital output cards. Flow measurement and flow control valves are also monitored/controlled by input and output cards.

The first proposed solution of Profibus DP has been removed from architecture: Indeed a minimum length of 1 meter cable for a Profibus DP is required for each flow transmitter, it means 6 meters of tough cables in one rack. Moreover one Profibus communication card is also needed. So it was a quite expensive solution and it could not fit in the rack.

The PLC manages the gas interlock.

In *Figure* 4 we can see the power supply, the CPU, analog and digital I/O cards and ET200SP remote I/O. They fit into a DIN-rail.

Figure 4 *: PLC system for the gas control, with the CPU, I/O cards and ET200SP remote I/Os*

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2.2.2. Hardware for High Voltage and Low Voltage

To control high and low voltages, the CAEN SY4527 crate has been chosen:

- To supply the Mesh and Drift voltages of each detector, A7030 modules (3kV/2nA) will be plugged inside the crate. Each A7030 module can control 48 channels (24 detectors).
- To supply the low voltages of the pre-amplifiers, A2519 modules (15V/5A) will be plugged inside the crate. Each A2519 module has 8 channels.

The SY4527 crate has 16 slots to plug either low voltage or high voltage module. A CPU board manages the control of these modules. It also provides an EPICS IOC that we plan to use for the control system.

2.2.3. Hardware for data acquisition

All hardware and facilities excepted FMC boards are provided by ESS ERIC. FMC board are provided by ESSI. The hardware used are in compliance with the standards set by ESS ICS.

We use an MTCA crate with a power module, an MCH board and several AMC board: the IOxOS IFC1410 board.

2.2.3.1. MTCA crate

MTCA = µTCA: Micro Telecommunications Computing Architecture

A cooling unit, a power module, a backplane and an MCH board are the basic minimum configuration.

Communications between AMC and MCH are done through the backplane.

The adjacent figure shows the board architecture.

MCMC : MicroTCA Carrier Management Controller
MCH : MTCA Carrier HUB
MMC : Module Management Controller
AdvancedMC : AMC : Advanced Mezzanine Card
EMMC : Enhanced Module Management Controller
PM : Power Module
CU : Cooling Unit
µRTM : MicroTCA.4 Rear Transition Module

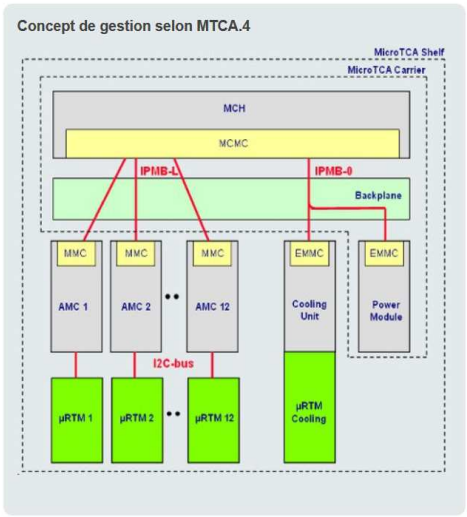

Figure 5 : MTCA architecture

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2.2.3.2. MCH board description

This board configures and manages the communications in the backplane.
It also controls temperature and power of AMC boards

2.2.3.3. AMC boards IOxOS IFC1410

IOxOS Technologies provides the IFC1410, an MTCA.4 Intelligent FMC Carrier in AMC form factor featuring a NXP QorIQ T Series PowerPC processor and 2 FPGA: Xilinx Artix-7 and Kintex UltraScale devices. The IFC1410 can carry 2 FMC boards. A µRTM can also be connected to the IFC1410 using the backplane connectors.

On one FMC port we connect a compatible ADC3111 acquisition boards.

The FPGA is connected to 2 DDR3 memories (512 MB each).

The PowerPC processor has a dedicated DDR3 memory with a size of 2 GB. But it can also accessed via PCIe to the 2 DDR3 memories connected to the FPGA.

2.2.3.4. IOxOS ADC3111 FMC board

Each FMC ADC3111 can read 8 analog signals. The input voltage range is -0.5V to 0.5V.

As the timing response of the detector is very fast (at the precision of ns) and the total duration of a neutron peak is of the order of 100-150 ns, the acquisition sampling frequency of 250 MSamples/s of the FMC board is satisfying.

2.2.3.5. Timing receiver board

We need a timing system to synchronize data acquisition with timing signal as the PULSE ON (14Hz) for example.
For that the Event Receiver board (EVR) with an AMC form factor is used inside the MTCA crate. EVR boards are connected with optic fiber to an Event Generator (EVG).

2.2.3.6. Overview of a possible BEE/MTCA crate configuration for the nBLM

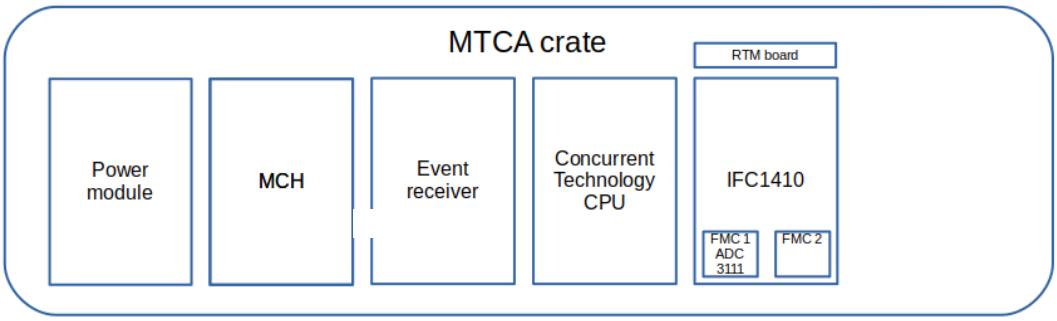

Figure 6 : Possible BEE or MTCA crate for nBLM acquisitions

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3. Software description

The Supervisory Control And Data Acquisition chosen by ESS ERIC is EPICS. The EPICS control is used as a setting and diagnostic tool for commissioning, for beam tuning and for the long term monitoring.

GUI are done under CS-Studio.

As seen in Figure 1, a nBLM detector needs voltage, gas, and acquisition system. These equipment must be controlled in EPICS with an IOC for each:

- a neutron detection IOC running on IFC1410 board
- a HV/LV IOC running on SY4527 crate
- a gas IOC running on centos_x64 (temporary because at the end it will be on the IFC1410 board)

Moreover in accelerator context, we will need timing and synchronization system:

- a MRF IOC

All these IOC must be included in the ESS Epics Environment (EEE).

3.1. Gas Control System

As seen in chapter 2.2.1, a PLC controls the gas management. The main goal of the PLC is to ensure the integrity of the 6 detector lines sets independently. The PLC also manages the gas flow regulation.

3.1.1.PLC process

The PLC performs flow control (PID type) for each set of detectors. It will ensure the security of the detectors by the control of the electro valve. All the controls settings and warning/fault thresholds can be fully adjusted by the user.

The following diagram shows the final gas distribution architecture. The main chassis links the gas storage system with the gas distribution system. Three distribution chassis (two + one spare) deliver the gas for each detectors groups.

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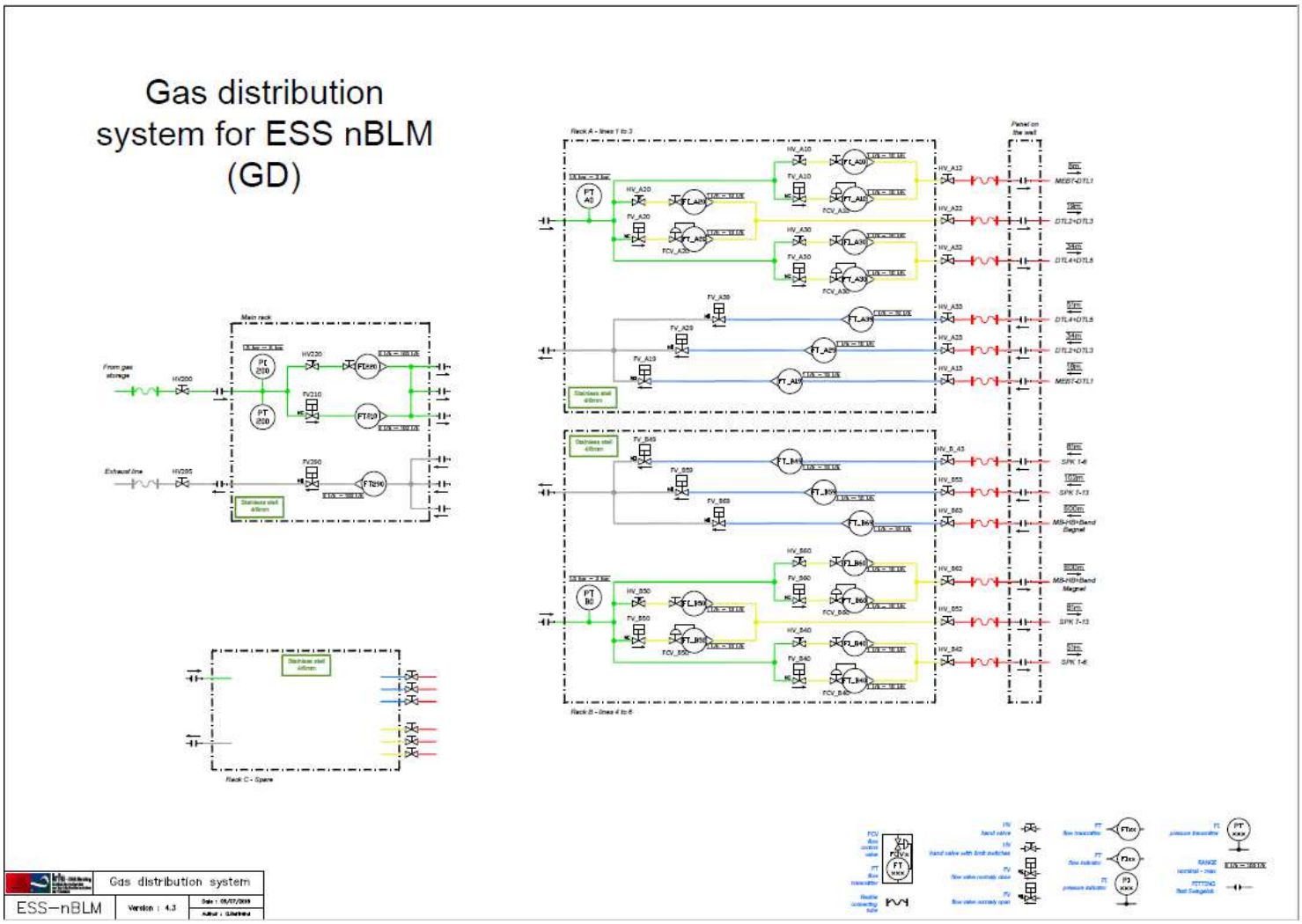

Figure 7 : Gas distribution architecture

The gas system is controlled by Siemens PLC, although we need to pass control parameters to the Control System via Channel Access. There will be 1 main line and 6 gas lines in operation going from the gallery to the tunnel. They will be installed in parallel and each one will provide gas to a group of detectors placed on different locations. Therefore, we are going to monitor the flow per line, and not per detector.

In case of a warning, there is no action on PLC process.
In case of a fault, the PLC will close the flow valve IN/OUT of the line.

All thresholds can be modified through EPICS interface: in user mode or expert mode.

Each detectors lines can be switch together. For example, line MEBT-DTL1 can be connected on “ChassisA-Line1” or “ChassisB-Line2” or “ChassisC-Line3”. It must be indicated to the PLC through EPICS interface. In case of a hardware fault (dead sensors for example), just put the concerned line on a spare line (tubing and soft).

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3.1.2.PVs lists from PLC database

As all gas data must be controlled with EPICS, here is the PVs list for the gas system. The first table is for the distribution gas line and the second table is for the main gas line.

Maybe warning or alarm names will be modified (TBC).

Name	Type	Update rate	PV type	eed expert ?	min	max	unit	Comments
I/O								
*PLC-Liney:Prs	Input	1 Hz	scalar	-	0	5	bar	
*FT-xy0:Flw	Input	1 Hz	scalar	-	0	10	L/h	
*FT-xy9:Flw	Input	1 Hz	scalar	-	0	10	L/h	
*PLC-Liney:GapFlw	Internal	1 Hz	scalar	-	0	10	L/h	
*MV-xy0:Opened	Input	On change	bit	-	false	true	-	Hand valves limit switches
*MV-xy0:Closed	Input	On change	bit	-	false	true	-	
*FV-xy0:PosCmd	Output	On change	bit	-	false	true	-	
*FV-xy9:PosCmd	Output	On change	bit	-	false	true	-	
*FCV-xy0:PosSP	Output	1Hz	scalar	-	0	100	%	
Software errors								
*MV-xy0:MismatchErr	Internal	On change	bit	-	false	true	-	
*MV-xy0:CmdErr	Internal	On change	bit	-	false	true	-	hand valve is opened during auto mode
*FT-xy0:LoErr	Internal	On change	bit	-	false	true	-	
*FT-xy0:HiErr	Internal	On change	bit	-	false	true	-	
*FT-xy0:HiHiErr	Internal	On change	bit	-	false	true	-	
*PLC-Liney:GapFlwHiErr	Internal	On change	bit	-	false	true	-	
*PLC-Liney:GapFlwHiHiErr	Internal	On change	bit	-	false	true	-	
*PLC-Liney:PrsHiErr	Internal	On change	bit	-	false	true	-	
*PLC-Liney:PrsHiHiErr	Internal	On change	bit	-	false	true	-	
*PLC-Liney:PrsLoErr	Internal	On change	bit	-	false	true	-	
*PLC-Liney:ErrTripped	Internal	On change	integer	-	0	20	-	Number of tripped error
Error threshold								
*FT-xy0:LoErrTrsh	Internal	On change	scalar	No	0	10	L/h	Lo > LoLo Hi < HiHi
*FT-xy0:LoLoErrTrsh	Internal	On change	scalar	Yes	0	10	L/h	
*FT-xy0:HiErrTrsh	Internal	On change	scalar	No	0	10	L/h	
*FT-xy0:HiHiErrTrsh	Internal	On change	scalar	Yes	0	10	L/h	
*PLC-Liney:GapFlwHiErrTrsh	Internal	On change	scalar	No	0	10	L/h	
*PLC-Liney:GapFlwHiHiErrTrsh	Internal	On change	scalar	Yes	0	10	L/h	
*PLC-Liney:PrsLoErrTrsh	Internal	On change	scalar	No	0	5	bar	
*PLC-Liney:PrsHiErrTrsh	Internal	On change	scalar	No	0	5	bar	
*PLC-Liney:PrsHiHiErrTrsh	Internal	On change	scalar	Yes	0	5	bar	
Error hysteresis timer								
*MV-xy:MismatchErrTim	Internal	On change	integer	No	0	-	s	Time before error tripping
*FT-xy0:LoErrTim	Internal	On change	integer	No	0	-	s	
*FT-xy0:LoLoErrTim	Internal	On change	integer	Yes	0	-	s	
*FT-xy0:HiErrTim	Internal	On change	integer	No	0	-	s	
*FT-xy0:HiHiErrTim	Internal	On change	integer	Yes	0	-	s	

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*PLC-Liney:GapFlwHiErrTim	Internal	On change	integer	No	0	-	s	
*PLC-Liney:GapFlwHiHiErrTim	Internal	On change	integer	Yes	0	-	s	
*PLC-Liney:PrsLoErrTim	Internal	On change	integer	No	0	-	s	
*PLC-Liney:PrsHiErrTim	Internal	On demand	integer	No	0	-	s	
*PLC-Liney:PrsHiHiErrTim	Internal	On demand	integer	Yes	0	-	s	
*PLC-Liney:ShuntErrTim	Internal	On change	integer	Yes	0	-	min	Error-free time at startup
Error ack								
*MV-xy0:MismatchErrAck	Internal	On change	bit	No	false	true	-	
*MV-xy0:CmdErrAck	Internal	On change	bit	No	false	true	-	
*FT-xy0:HiHiErrAck	Internal	On change	bit	No	false	true	-	
*PLC-Liney:GapFlwHiHiErrAck	Internal	On change	bit	No	false	true	-	
*PLC-Liney:PrsHiHiErrAck	Internal	On change	bit	No	false	true	-	
*PLC-Liney:Ack	Internal	On change	bit	No	false	true	-	Line ack
Error bypass								
*MV-xy0:MismatchErrBypass	Internal	On change	bit	Yes	false	true	-	
*MV-xy0:CmdErrBypass	Internal	On change	bit	Yes	false	true	-	
*FT-xy0:LoErrBypass	Internal	On change	bit	Yes	false	true	-	
*FT-xy0:HiErrBypass	Internal	On change	bit	Yes	false	true	-	
*FT-xy0:HiHiErrBypass	Internal	On change	bit	Yes	false	true	-	
*PLC-Liney:GapFlwHiErrBypass	Internal	On change	bit	Yes	false	true	-	
*PLC-Liney:GapFlwHiHiErrBypass	Internal	On change	bit	Yes	false	true	-	
*PLC-Liney:PrsHiErrBypass	Internal	On change	bit	Yes	false	true	-	
*PLC-Liney:PrsHiHiErrBypass	Internal	On change	bit	Yes	false	true	-	
*PLC-Liney:PrsLoErrBypass	Internal	On change	bit	Yes	false	true	-	
*PLC-Liney:ErrBypassed	Internal	On change	integer	Yes	0	20	-	Number of bypassed error
Hardware errors								
*FT-xy0:HardErr	Internal	On change	bit	-	false	true	-	
*FT-xy9:HardErr	Internal	On change	bit	-	false	true	-	
*FCV-xy0:HardErr	Internal	On change	bit	-	false	true	-	
*PLC-Liney:PrsHardErr	Internal	On change	bit	-	false	true	-	
Status								
*PLC-Liney:Ready	Internal	On change	bit	-	false	true	-	Ready to use
*PLC-Liney:SoftErr	Internal	On change	bit	-	false	true	-	
*PLC-Liney:SoftWarn	Internal	On change	bit	-	false	true	-	
*PLC-Liney:HardErr	Internal	On change	bit	-	false	true	-	
Flow control settings								
*PLC-Liney:StartReg	Internal	On change	scalar	No	0	-	-	Start flow
*FCV-xy0:Kp	Internal	On change	scalar	Yes	0	-	-	
*FCV-xy0:Ti	Internal	On change	scalar	Yes	0	-	-	
*FCV-xy0:Td	Internal	On change	scalar	Yes	0	-	-	
*FCV-xy0:LimB	Internal	On change	scalar	Yes	0	100	%	
*FCV-xy0:LimH	Internal	On change	scalar	Yes	0	100	%	
*FCV-xy0:AutoManu	Internal	On change	scalar	Yes	false	true	-	
*PLC-Liney:FlowSP	Internal	On change	scalar	No	0	10	L/h	

*: “FEB-050Row:PBI-“ prefix
x: chassis A, B
y: line 1, 2 or 3 for each chassis

Table 1: PVs list for each gas line TBC

Name	Input or output	Update rate	PV type	Need expert ?	min	max	unit	Comments
I/O								
*PT-110:Prs	Input	1 Hz	scalar	-	0	5	bar	
*FT-210:Prs	Input	1 Hz	scalar	-	0	100	L/h	
*FT-290:Flw	Input	1 Hz	scalar	-	0	100	L/h	
*MV-220:Opened	Input	On change	bit	-	false	true	-	

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*MV-220:Closed	Input	On change	bit	-	false	true	-	
*FV-210:PosCmd	Output	On change	bit	-	false	true	-	
*FV-290:PosCmd	Output	On change	bit	-	false	true	-	
Software errors								
*MV-220:CmdErr	Internal	On change	bit	-	false	true	-	if hand valve is opened during auto mode
*PT-110:PrsHiErr	Internal	On change	bit	-	false	true	-	
* PT-110:PrsHiHiErr	Internal	On change	bit	-	false	true	-	
* PT-110:PrsLoErr	Internal	On change	bit	-	false	true	-	
*FT-210:LoErr	Internal	On change	bit	-	false	true	-	
*FT-210:HiErr	Internal	On change	bit	-	false	true	-	
*FT-210:HiHiErr	Internal	On change	bit	-	false	true	-	
*PLC-MainLine:GapFlwHiErr	Internal	On change	bit	-	false	true	-	
*PLC-MainLine:GapFlwHiHiErr	Internal	On change	bit	-	false	true	-	
Error threshold								
*PT-110:PrsHiErrTrsh	Internal	On change	scalar	No	0	5	bar	
* PT-110:PrsHiHiErrTrsh	Internal	On change	scalar	Yes	0	5	bar	
* PT-110:PrsLoErrTrsh	Internal	On change	scalar	No	0	5	bar	
*FT-210:LoErrTrsh	Internal	On change	scalar	No	0	100	L/h	
*FT-210:HiErrTrsh	Internal	On change	scalar	No	0	100	L/h	
*FT-210:HiHiErrTrsh	Internal	On change	scalar	Yes	0	100	L/h	
*PLC-MainLine:GapFlwHiErrTrsh	Internal	On change	scalar	No	0	100	L/h	
*PLC-MainLine:GapFlwHiHiErrTrsh	Internal	On change	scalar	Yes	0	100	L/h	
Error hysteresis timer								
*PT-110:PrsHiErrTim	Internal	On change	scalar	No	0	-	s	Time before error tripping
* PT-110:PrsHiHiErrTim	Internal	On change	scalar	Yes	0	-	s	
* PT-110:PrsLoErrTim	Internal	On change	scalar	No	0	-	s	
*FT-210:LoErrTim	Internal	On change	scalar	No	0	-	s	
*FT-210:HiErrTim	Internal	On change	scalar	No	0	-	s	
*FT-210:HiHiErrTim	Internal	On change	scalar	Yes	0	-	s	
*PLC-MainLine:GapFlwHiErrTim	Internal	On change	scalar	No 1	0	-	s	
*PLC-MainLine:GapFlwHiHiErrTim	Internal	On change	scalar	Yes	0	-	s	
Error ack								
* PT-110:PrsHiHiErrAck	Internal	On change	bit	No	false	true	-	
*FT-210:HiHiErrAck	Internal	On change	bit	No	false	true	-	
*PLC-MainLine:GapFlwHiHiErrAck	Internal	On change	bit	No	false	true	-	
Error bypass								
*PT-110:PrsHiErrByPass	Internal	On change	bit	Yes	false	true	-	
* PT-110:PrsHiHiErrByPass	Internal	On change	bit	Yes	false	true	-	
* PT-110:PrsLoErrByPass	Internal	On change	bit	Yes	false	true	-	
*FT-210:LoErrByPass	Internal	On change	bit	Yes	false	true	-	
*FT-210:HiErrByPass	Internal	On change	bit	Yes	false	true	-	
*FT-210:HiHiErrByPass	Internal	On change	bit	Yes	false	true	-	
*PLC-MainLine:GapFlwHiErrByPass	Internal	On change	bit	Yes	false	true	-	
*PLC-MainLine:GapFlwHiHiErrByPass	Internal	On change	bit	Yes	false	true	-	
Hardware errors								
*PT-110:HardErr	Internal	On change	bit	-	false	true	-	
*FT-210:HardErr	Internal	On change	bit	-	false	true	-	
*FT-290:HardErr	Internal	On change	bit	-	false	true	-	
Status								
*PLC-Gas:Ready	Internal	On change	bit	-	false	true	-	if all lines = ready
*PLC-Gas:SoftErr	Internal	On change	bit	-	false	true	-	if at least 1 line = soft err
*PLC-Gas:SoftWarn	Internal	On change	bit	-	false	true	-	if at least 1 line = soft warn
*PLC-Gas:HardErr	Internal	On change	bit	-	false	true	-	if at least 1 line = hard err
*: “FEB-050Row:PBI-“ prefix								

Table 2 : PVs list for the main line gas TBC

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3.1.3.PLC Factory

PLC Factory have to be used for final control system at ESS. However it wasn't specified to CEA at the beginning of the nBLM project and of the PLC programming process. Like PLC factory is a new tool for CEA that means that CEA PLC expert needs experience, support from ESS and practice to be efficient.

First major issue is that this tool provide a new basic PLC code, so actual PLC code have to be modified to fit with it, what is a complex and time-consuming task. Second major issue is about the PLC – EPICS communication server: CEA PLC expert has to use ESS tools for server definition as CCDB and we are not skilled yet.

A first development from CEA to ESS have to be provided soon (RFQ temperature interlock PLC) and will give knowledge to CEA PLC expert about those tools, issues and time needed for this development part.
Those new tools will need time and feedback from previous development to be used efficiently by CEA PLC expert.

So for tests in Saclay we will use a Saclay version of PLC-EPICS communication server. This allows to implement the PLC process and different equipment (gas and control chassis).

3.2. HV/LV Control System

3.2.1.EPICS database communication for the HV/LV

The SY4527 provides an embedded IOC that starts on SY4527 boot. We don't have access to its EPICS database. This is a problem for naming convention and timestamp:

1. Naming convention: the SY4527 web interface makes it possible to change only the PV prefix. The PV has the following structure (in green: settable field, in red: not settable field): <PREFIX>:<BOARD_NUMBER>:<CHANNEL_NUMBER>:<PROPERTY>. This PV structure does not meet ESS naming convention.

2. Timestamp: the SY4527 IOC is timestamping its PVs with its local time. It seems to be delicate to not have the IOC synchronized with the global time server of ESS machine.

To resolve this problem, we propose to have an intermediate IOC that reads and writes the SY4527 IOC PVs. This IOC would run on the IFC1410 board and it would enable to have custom PV names and PV timestamps synchronized with ESS timing server (see next figure).

To be sure that the value set by user in the graphical interface has been transmitted to CAEN IOC (IOC reboot or communication error could introduce some strange behavior), we added a mechanism of "Read Back Value". This RBV PV is in charge of reading back the set value on the CAEN IOC. From that point, in CS-studio, we are able to inform the user that its command has been taken into effect by the CAEN IOC or not.

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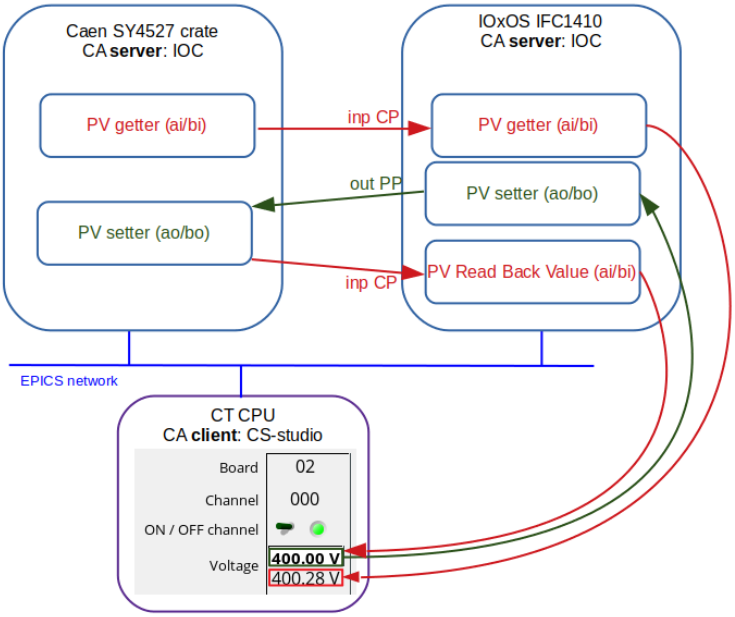

Figure 8 : interposed IOC for the high voltage control

The minor inconvenient of this solution is that the SY4527 PV is still accessible by Channel Access and it doubles the number of PVs for controlling nBLM high voltages.

3.2.2.PV definition for HV/LV

Each detector has two high voltage inputs: one for the mesh and one for the cathode. Control system is identical for both. All the channels are driven individually.

Name	Input or output	Update rate	PV type	Number of elements	min	max	Comments
HV ON/OFF	output	On demand	bit	1	-	-	
HV write voltage	output	On demand	scalar	1	0	?	
HV write max voltage	output	On demand	scalar	1	0	?	
HV write max current	output	On demand	scalar	1	0	?	
HV write offset current	output	On demand	scalar	1	0	?	
HV write ramp up voltage	output	On demand	scalar	1	0	?	
HV write ramp down voltage	output	On demand	scalar	1	0	?	
HV status	input	On change	scalar	1	-	-	
HV read voltage	input	1 Hz	scalar	1	?	?	
HV read current	input	1 Hz	scalar	1	?	?	
HV read card	input	On demand	scalar	1	-	-	
HV read channel	input	On demand	scalar	1	-	-	
HV read temperature	input	1 Hz	scalar	1	?	?	

Table 3 : PVs list for HV per channel TBC

The FEE of several detectors are fed by the same low voltage module. Therefore, control system will be per line and not per detector. The functionalities are the same as the HV.

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Name	Input or output	Update rate	PV type	Number of elements	min	max	Comments
LV ON/OFF	output	On demand	bit	1	-	-	
LV write voltage	output	On demand	scalar	1	0	?	
LV write max voltage	output	On demand	scalar	1	0	?	
LV write max current	output	On demand	scalar	1	0	?	
LV write offset current	output	On demand	scalar	1	0	?	
LV write ramp up voltage	output	On demand	scalar	1	0	?	
LV write ramp down voltage	output	On demand	scalar	1	0	?	
LV status	input	On change	scalar	1	-	-	
LV read voltage	input	1 Hz	scalar	1	?	?	
LV read current	input	1 Hz	scalar	1	?	?	
LV read card	input	On demand	scalar	1	-	-	
LV read channel	input	On demand	scalar	1	-	-	
LV read temperature	input	1 Hz	scalar	1	?	?	

Table 4 : PVs list for LV per line TBC

Notice that for the low voltage, because of the length of the cables of ~50m, we need to give a higher value on the module to have ±5V on the detector.

3.3. Neutron detection Control System

3.3.1.Overview

As seen in the chapter 2.2.3 the BEE is an AMC board IFC1410 and a plug-in FMC module ADC3111.
The FMC module has 8 analog inputs. But, in the relaxed form of the requirements defined in the document [9] the FPGA processes up to 6 nBLM detectors.

The following figure shows an overview for the neutron detection sequencing.

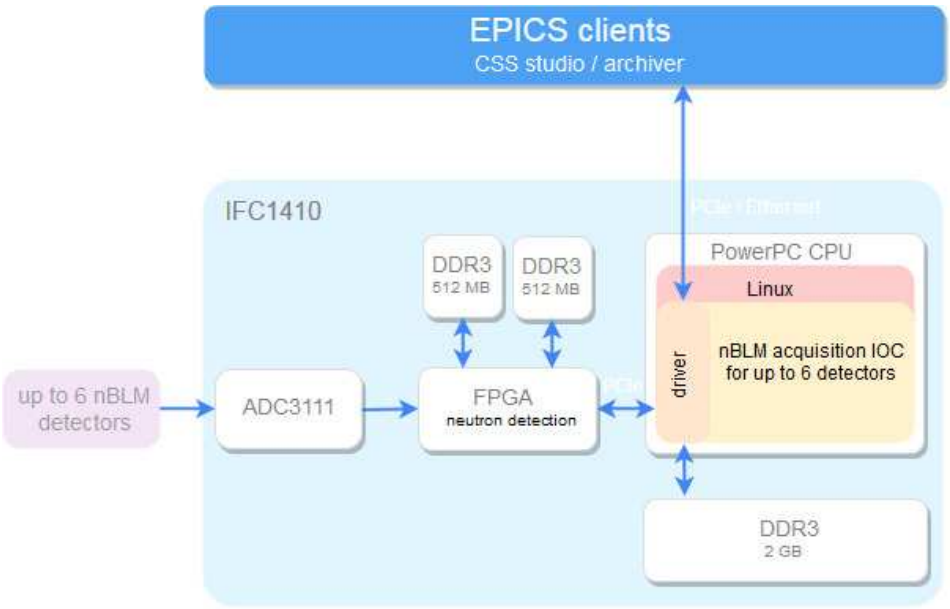

Figure 9 : nBLM detection sequencing

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As seen in chapter 2.2.3.3, the IOxOS IFC1410 card provides a Kintex Ultrascale FPGA and a QorIQ PowerPC processor. In this processor an operating system Linux is running (the Linux root file system is provided by a NFS server). One IOC for neutron detection is compiled and runs into this Linux file system. The IOC manages data from the FPGA, it does calculation, and provides data on the channel access for monitoring. The IOC also provides acquisition files on demand.

When an IFC1410 board startup, a script is executed. This script indicates the address and path of the NFS server. Then the FPGA firmware, the Linux and file system are loaded from the NFS files.
In the NFS root file system the EEE server address is provided for the EEE modules needed by the IFC1410.

Remark: Actually a Concurrent Technology AMC board installed inside the crate assumes to be the NFS and EEE server (see next chapter).

3.3.2.Software architecture

3.3.2.1. Initial scope application

The following Figure shows the software architecture for a scope example application running on the IFC1410 board. Some software parts are provided by ESS/ICS and other by IOxOS.

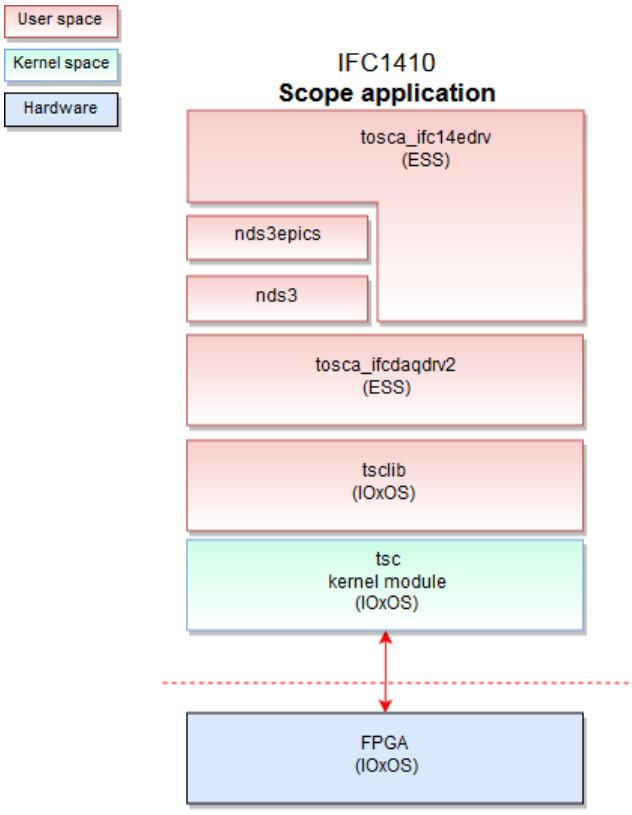

Figure 10 *: IFC1410 scope software architecture*

- The tsc kernel module accesses FPGA registers and memory via the PCIe
- The tsclib is a library which accesses to the tsc kernel module using ioctl
- Tosca_ifcdaqdrv2 is the “driver EPICS” for the “scope application”: It provides high level process function (set decimation, gain, etc.) for several kinds of FMC board
- Tosca_if14edrv is the IOC for the scope. It requires nds3 and tosca_ifcdaqdrv2

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Thus when we run the tosca_ifc14edrv EEE module it requires Nds3, Nds3epics and tosca_ifcdaqdrv2 EEE modules to work.

3.3.2.2. Specific nBLM application

To manage the nBLM neutron detection and acquisition, a custom FPGA firmware is developed by the DMCS laboratory, it uses the IOxOS TOSCA framework. The firmware specifications are described in the document [9].

As the new FPGA firmware is completely different from the one developed for the scope application, we need to modify upper software layer in the software architecture. But lower software layers “tsc kernel module” and ”tsclib” are still functional as the firmware development is done with IOxOS TOSCA framework.

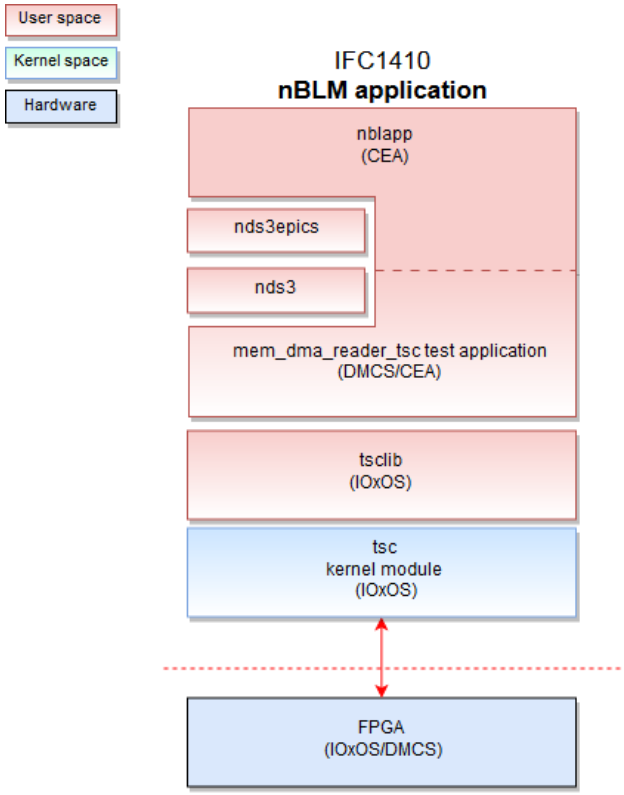

Figure 11 *: IFC1410 nBLM software architecture*

We can see in the previous Figure that the 2 upper layers in the scope application becomes now one software layer (or module) named “nblmapp”.

Indeed, DMCS provided a “not EPICS” application to test the firmware. It works with command lines. Some modifications have been done inside this application to add EPICS part (NDS3 implementation). Hence there are 2 possible compilations, the first one to obtain the initial test application (command line) and the second one to generate the “EPICS application/driver” named “nblmapp”.

Therefore the nblmapp is a module provided by the EEE server and it requires Nds3 and Nds3epics EEE modules to work.

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3.3.3.Software interface with the FPGA firmware

The control registers and algorithm parameters are available on the TCSR interface. All the processing results are stored in two banks of DDR3 memory on the IFC1410 board, logically treated as 14 independent data stream (called Circular Buffer channels). The software in the PowerPC CPU can accessed to the Circular Buffer data via DMA through the PCIe interface. See document [10] for details on software interface with the FPGA firmware.

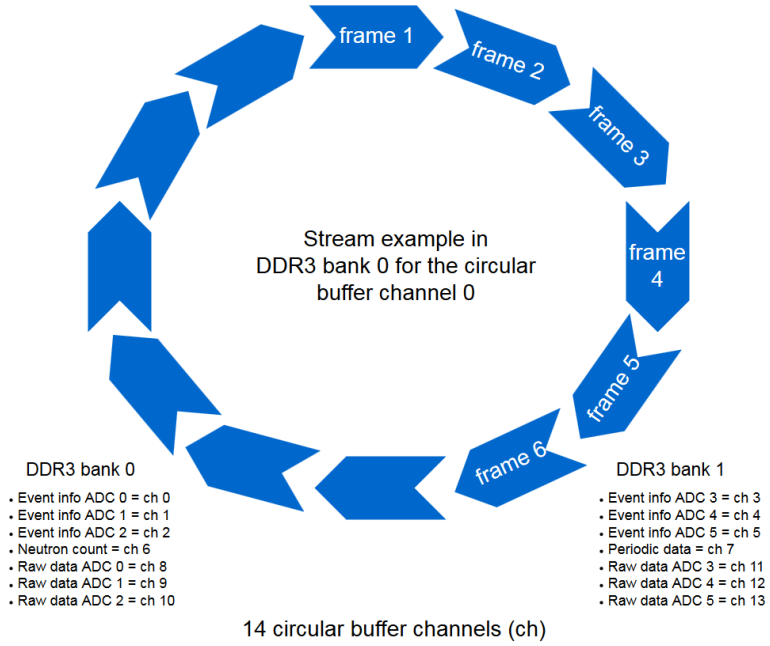

Figure 12 : Example of the circular buffer channel 0 acquisition in the DDR3 bank 0

3.3.4.“nblmapp” module architecture

The actual implementation is described in the Figure 13.
The “mem_dma_reader_tsc” application test reads all active circular buffers at exit of the executable whereas the nblmapp IOC continuously reads periodic data and can read small size of other circular buffers on software demand. The circular buffer channel must be activated for reading it.

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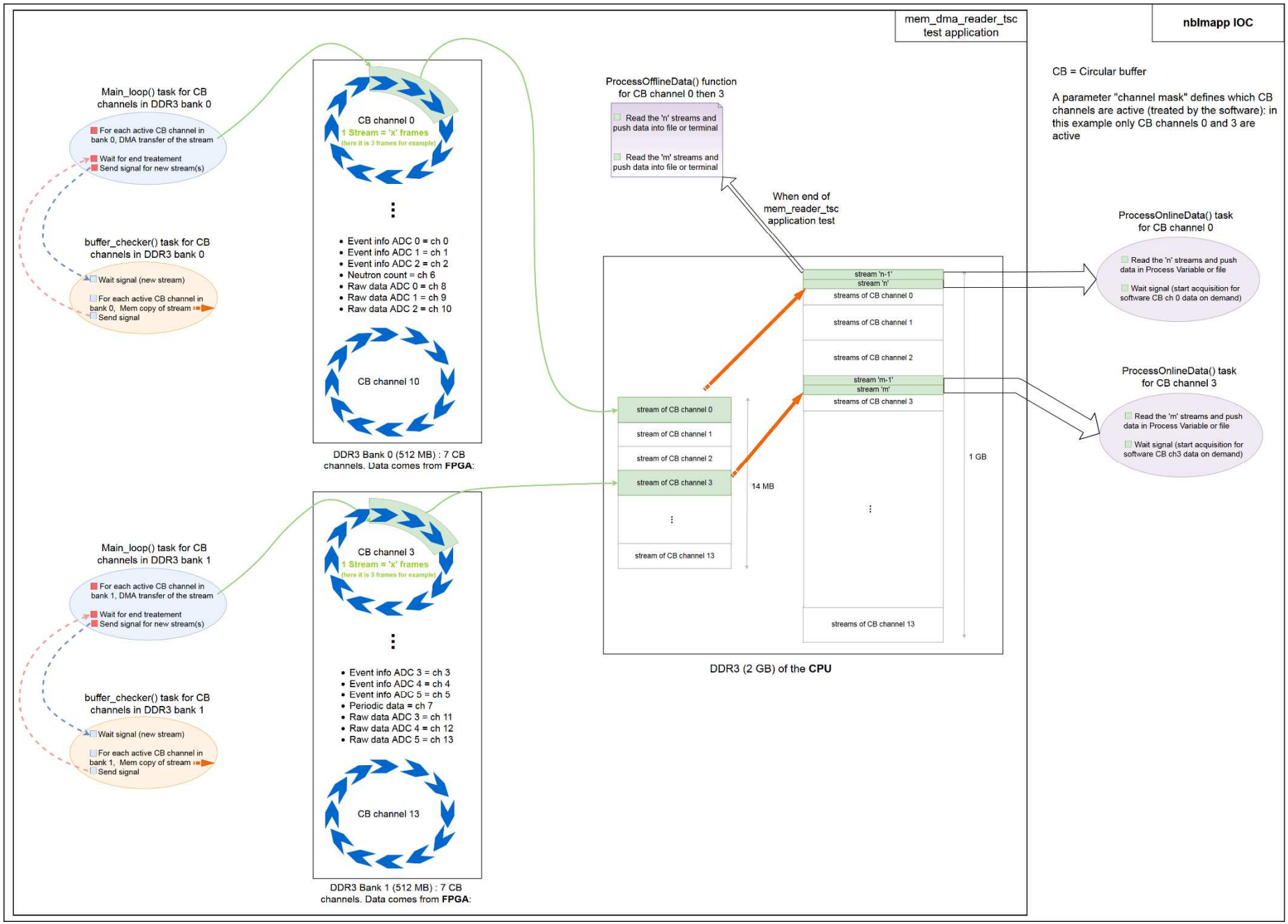

Figure 13 : "nblm" architecture

Once streams of a circular buffer channel has been read in the CPU DDR3, the buffer is erased and start address is re-initialized.

For the circular buffer 7 (periodic data) the ProcessOnlineData() task pushes data as soon data are available in the CPU DDR3. It doesn't wait for signal "start acquisition" as it is a continuous acquisition.

3.3.5.Process Variables definition for neutron detection

Terminologies and definitions are defined in document [9].

3.3.5.1. Input PVs

Input process variables are also defined in the document [9]. For each data a index "ID" is given in this document. The following table suggests input PV name associated to the ID.

"*" mark indicates that the data is global for all channels, thus no mark indicates that data names are duplicated for each channel.

Name	ID reference
lossOverT(1,2,3,4,5,6,7)	1-7
lossOverTnom	8
lossOverBeamOn	9
lossOverBeamOnPerProton	10
lossWin(1,2,3,4)	11-14
lossAvgInWin(1,2,3,4)	15-18
lossVarInWin(1,2,3,4)	19-22
lossMinInWin(1,2,3,4)	23-26
lossMaxInWin(1,2,3,4)	27-30
n_Counts(Avg,Var,Min,Max)	31-34
Q_TOT(Avg,Var,Min,Max)	35-38
Q_Bckgnd(Avg,Var,Min,Max)	39-42
Q_Total(Avg,Var,Min,Max)	43-46
beamPermit*	47
ready*	49
protectionAlgoTypev	51
protection1Win(1,2,3,4)	52-55
protection1AvgInWin(1,2,3,4)	56-59
protection1VarInWin(1,2,3,4)	60-63
protection1MinInWin(1,2,3,4)	64-67
protection1MaxInWin(1,2,3,4)	68-71
protection2Win(1,2,3,4)	72-75
protection2(Avg,Var,Min,Max)InWin(1,2,3,4)	76-91
protection3Win(1,2,3,4)	92-95
protection3(Avg,Var,Min,Max)InWin(1,2,3,4)	96-111
protection4Win(1,2,3,4)	112-115
protection4(Avg,Var,Min,Max)InWin(1,2,3,4)	116-131
protection5Win(1,2,3,4)	132-135
protection5(Avg,Var,Min,Max)InWin(1,2,3,4)	136-151
pedestalOverTnom	152

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noiseOverTnom	153
posSatOverTnom	154
negSatOverTnom	155
Q_TOT_evts(Avg,Var,Min,Max)	156-159
peakTime_evts(Avg,Var,Min,Max)	160-163
TOT_evts(Avg,Var,Min,Max)	164-167
riseTime_evts(Avg,Var,Min,Max)	168-171
AMC_health*	172
SmartTrig	173

Table 5 : Input PVs list for neutron detection TBC

3.3.5.2. Output PVs

In document [9] outputs PV are also defined. For each data a "S_{index}" is given in this document. The following table suggests output PV name associated to the S_{index}.
"*" mark indicates that the setting value is duplicated for all channels.

Name	Sindex reference
T(1,2,3,4,5,6,7)*	1-7
unit*	8
lossWinlength(1,2,3,4)	9-12
lossWinStart(1,2,3,4)	13-16
displayEnable	17-20
pedestalWinlength	21
pedestalWinStart	22
pedestalExcludeEvents*	23
singleNeutronCount	24

Table 6 : Output PVs list for neutron detection TBC

3.3.6.CS-Studio design

Preliminaries views have been designed (see Appendix A) in order to display data from the FPGA firmware with no conversion.

Firmware configuration is also possible but still with raw setting (no conversion).

Circular buffer channels could be enabled or disabled (see chapter 3.3.4), it means that the software doesn't transfer data in the CPU DDR3 when the circular buffer is disabled/deactivated.

3.4. Event receiver (EVR)

Due to the pulsing beam, the neutron counting must be synchronized with the accelerator timing system. Moreover the data timestamping must be also synchronized with the accelerator time. Thus we need an event receiver equipment as the MRF which provides useful functions for NBLM:

- DOD trigger
- timing system (beam mode)
- PV timestamp

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3.5. System status

Each subsystem of nBLMs has different status. It could be by channel, by distribution gas line, etc. and global status by equipment. Here is a list of these different status:

- LV equipment (3 boards):
  - all status per line
  - 1 global status per board
- HV equipment (5 boards)
  - all status per channel (48 channels)
  - 1 global status board
- HV/LV equipment (3 crates)
  - 1 global status of a crate
- gas equipment (3 chassis)
  - all status per line (6 lines-in and 6 lines-out)
  - gas bottle status
  - 1 global status for the gas installation
- MTCA equipment (10 crates)
  - ADC temp (HHigh LOLOw EPICS alarm) per AMC board (17 IFC1410 boards)
  - MCH status: power, temperature, etc.
  - 1 global status per crate including MCH status

A global nBLM device status merges all status of all subsystems used by a nBLM detector. Thus we will have 84 global nBLM device status.

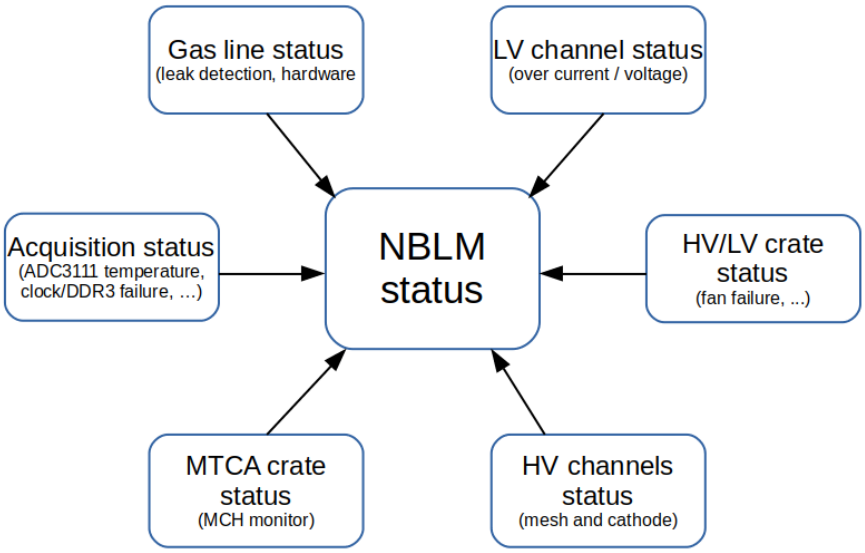

Figure 14 *: status for one nBLM*

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4. Test plan

We are planning to have 2 integration test phases: one at Saclay and one at Lund (vertical integration test). Tests are similar, the location is changing and some equipment, like gas line, are provided by ESS. The goal is to have a fully working detector with all the control system required.

For each phase we will firstly test subsystem individually.

4.1. Individual tests of each subsystem

This section is presenting individual tests we have performed / will perform per subsystem.

4.1.1. High voltage (most advanced test)

Micromegas detectors are quite sensitive to current and voltage variations of the high voltage channels. So it was mandatory to analyze these variations. This section explains how we proceeded and what we provided to carry out these tests. Please refer to document [12] for analysis results.

An EPICS IOC is running on the SY4527 crate and providing for every channel:

- current
- voltage
- warnings (over current, over voltage, …)
- and others information and parameters that was not useful for the tests.

The goal idea is to compute the histogram for current and voltage for each channel to get the channel variations. From a control system point of view, it means to store voltage and current monitors over a long period and then process data to get variations. To do so, we used an EPICS Appliance archiver to store data and the analysis is done in python.

In order to NOT have some misunderstood, here is some terminology:
channel: one of the high voltage channels.
loaded: high voltage channel is loaded when it is plugged to a detector.
run: a specific configuration (some HV channels are loaded and some others not) for a specific time, at least 24 hours, at maximum 72 hours.

4.1.1.1. Hardware

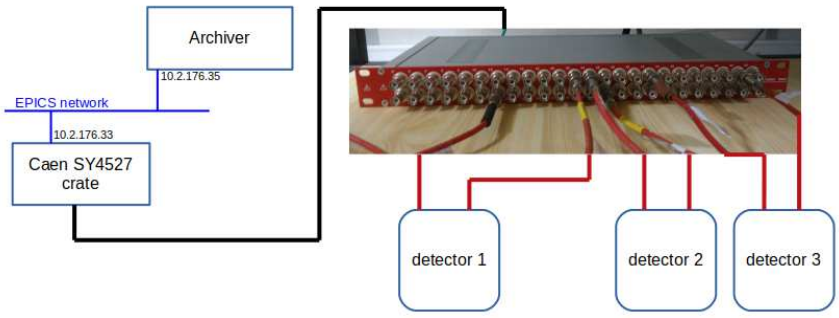

Figure 15 : *High voltage test stand: HV board + Caen SY4527 crate + archiver on the Epics network*

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As a matter of fact, we have only 3 detectors with 2 high voltage connectors each. It means that we can only test 6 HV channels at the same time. The high voltage board has 48 channels, so we need 8 runs (+ 1 run which no load on any channel).

EPICS archiver machine is dedicated to nBLM. It's a light machine, with 8GB of ram and 500GB of HDD.

4.1.1.2. Software

The archiver records every PV value changes. Current and voltage data are not sampled at a specific time by the SY4527 IOC, only changes processes the PV record.
We did different kind of analysis:

- Overview of all channels in time domain. Useful so see signal shapes, alarms and number of measurements.
- Semi-detailed view of all the channels: this script gives you what you really want to know without digging into details: know which channels have the most variations. Figure is below.
- Detailed view: specific analysis of a channel or a run.

The following figure is the result of the semi-detailed script. It shows the channels that have the largest variation in current and voltage. For the analysis of these results, please refer to the document [12].

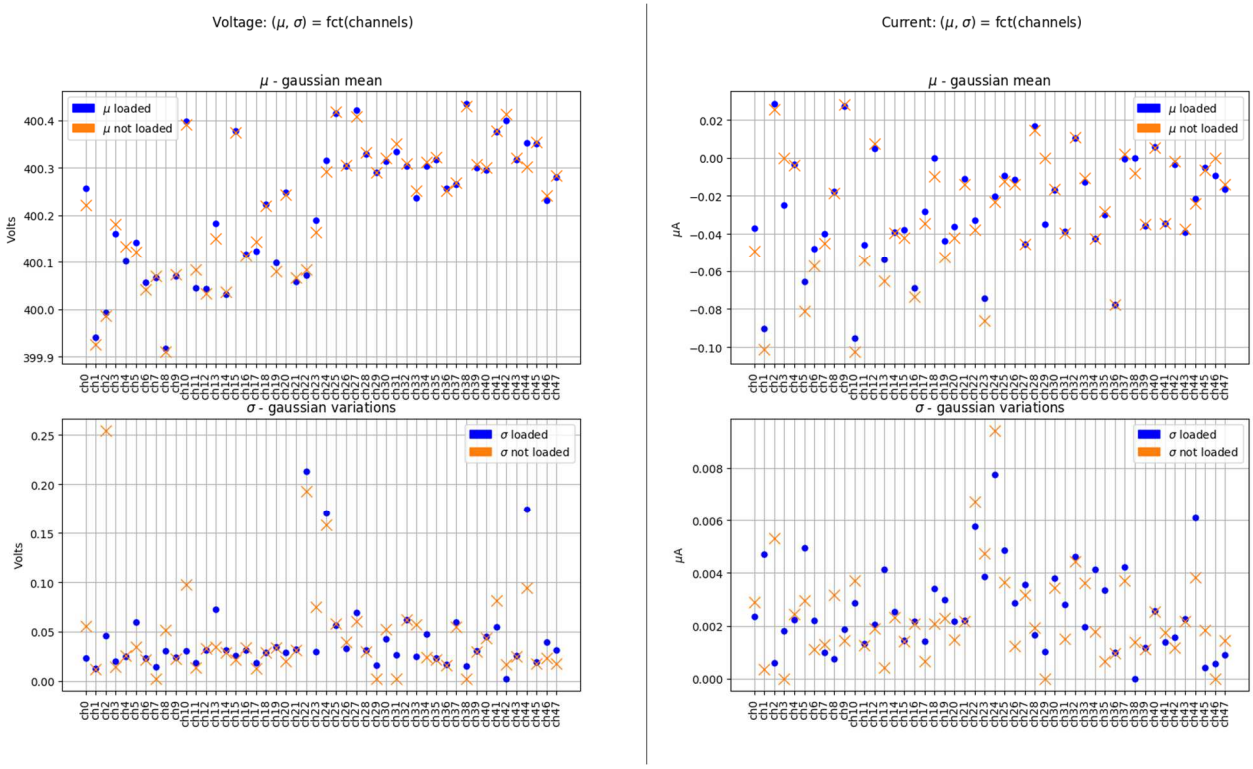

Figure 16 : *Voltage and current variations for HV channels*

Python scripts are available on ESS bitbucket, m-epics-nblm module in *misc/archiver/* folder.

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Every script has the same architecture:

1. configuration: which channel / which run data to process
2. data retrieval from archiver (using json)
3. data processing: mainly histograms
4. data visualization (matplotlib)

To compute histogram, a matplotlib function was used. To choose binning value, I used the datasheet information: voltage monitor resolution is 10 mV whereas current monitor resolution is 2nA. These 2 parameters are defined as constants in the lib file. You can change it if needed.
Moreover, each histogram is normalized: signal integration is equal to 1.

4.1.1.3. High voltage configuration via CS-Studio

To configure HV channels for a run, we provided a CS-studio view to set and get the different parameters: voltage, current, warnings, limitations, ...

Name	CHANNEL0	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 00	on/off	ramping down		400.22 Volt		-0.040 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL01	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 01	on/off	ramping down		399.90 Volt		-0.092 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL02	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 02	on/off	ramping down		400.17 Volt		0.028 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL03	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 03	on/off	ramping down		400.15 Volt		-0.028 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL04	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 04	on/off	ramping down		400.07 Volt		-0.008 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL05	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 05	on/off	ramping down		400.13 Volt		-0.070 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL06	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 06	on/off	ramping down		400.06 Volt		-0.048 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL07	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 07	on/off	ramping down		400.05 Volt		-0.042 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL08	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 08	on/off	ramping down		399.93 Volt		-0.022 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL09	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 09	on/off	ramping down		400.07 Volt		0.024 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL10	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 10	on/off	ramping down		400.43 Volt		-0.098 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL11	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 11	on/off	ramping down		400.04 Volt		-0.048 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL12	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 12	on/off	ramping down		399.96 Volt		0.002 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL13	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 13	on/off	ramping down		400.15 Volt		-0.056 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL14	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 14	on/off	ramping down		400.02 Volt		-0.040 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL15	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 15	on/off	ramping down		400.36 Volt		-0.042 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL16	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 16	on/off	ramping down		400.09 Volt		-0.072 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL17	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 17	on/off	ramping down		400.14 Volt		-0.030 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL18	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 18	on/off	ramping down		400.20 Volt		0.000 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL19	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 19	on/off	ramping down		400.05 Volt		-0.046 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL20	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 20	on/off	ramping down		400.25 Volt		-0.040 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL21	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 21	on/off	ramping down		400.00 Volt		-0.012 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL22	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 22	on/off	ramping down		400.04 Volt		-0.046 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL23	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 23	on/off	ramping down		400.20 Volt		-0.078 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL24	ramping up	Voltage	400.00 Volt	Current	0.24 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 24	on/off	ramping down		400.37 Volt		-0.024 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL25	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 25	on/off	ramping down		400.48 Volt		-0.002 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL26	ramping up	Voltage	400.00 Volt	Current	0.25 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 26	on/off	ramping down		400.26 Volt		-0.004 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL27	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 27	on/off	ramping down		400.38 Volt		-0.038 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL28	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 28	on/off	ramping down		400.31 Volt		0.022 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second
Name	CHANNEL29	ramping up	Voltage	400.00 Volt	Current	0.26 microAm	Max Voltage	500 Volt	Ramp up	20 Vps	OVERCURRENT condition	UNDERVOLTAGE condition
ch 29	on/off	ramping down		400.28 Volt		-0.034 microAm	currentt offset	0.000 microAm	Ramp down	50 Vps	OVERVOLTAGE condition	Trip	2.0 Second

Figure 17 : *CS-studio GUI, to control 48 HV channels (only 30 channels are displayed)*

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Since HV board has 48 channels, it is very fastidious to configure all the channel to the same configuration. So we provided a python script, integrated in CS-studio to set the same config to all channels.

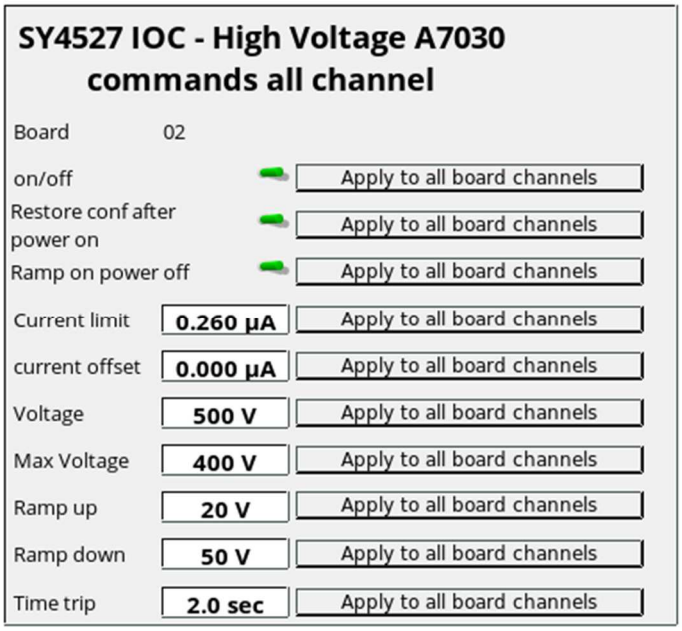

Figure 18 : *Configuration of all the channels*

4.1.2.Gas

We define the following verification procedure for the gas installation:

1) Connect gas chassis to power supply
2) Check digital inputs. Switch 0 to 1 and 1 to 0 and check PLC read back signal with Siemens TIA Portal
3) Repeat 2) for each digital input channel
4) Check analog inputs. Check PLC read back signal and converted signal with Siemens TIA Portal
5) Repeat 4) for each analog input channel
6) Check digital outputs. Control channel with Siemens TIA Portal and check the equipment state
7) Repeat 6) for each digital output channel
8) Check analog outputs. Control channel (3 values: 0%, 50%, 100%) with Siemens TIA Portal and check the equipment state
9) Repeat 8) for each analog output channel

4.1.3.Acquisition

Since IFC1410 and ADC311 are standardized platform for ESS accelerator, it's not in our scope to evaluate the acquisition channel performance (Signal Noise Ratio, etc.). However, we will check ADC channels to see if they are working properly.

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4.2. Integration tests in Saclay of one nBLM

The control of one nBLM requires the control of few elements from devices:

- 2 high voltage channels (one for the drift and one for the cathode)
- 1 low voltage channel
- 1 gas line: 1 distribution chassis
- 1 neutron detection channel

The control system test stand is composed of:

- one MTCA crate
  - one MCH and one power module
  - one Concurrent Technology CPU which is running EEE server for the IFC1410 and host the CS-studio client
  - one IFC1410 with one ADC3111 which is running Lodz firmware and CEA software for neutron detection
  - one MRF system, nothing done yet now
- one CAEN SY4527 crate which controls high voltage and low voltage for nBLM
- one siemens PLC S7-1500 which is controlling gas lines
- one appliance archiver to save PV data during tests.

The test stand is external server independent, it means that the system is standalone and can run anywhere (CEA, ESS, etc.).

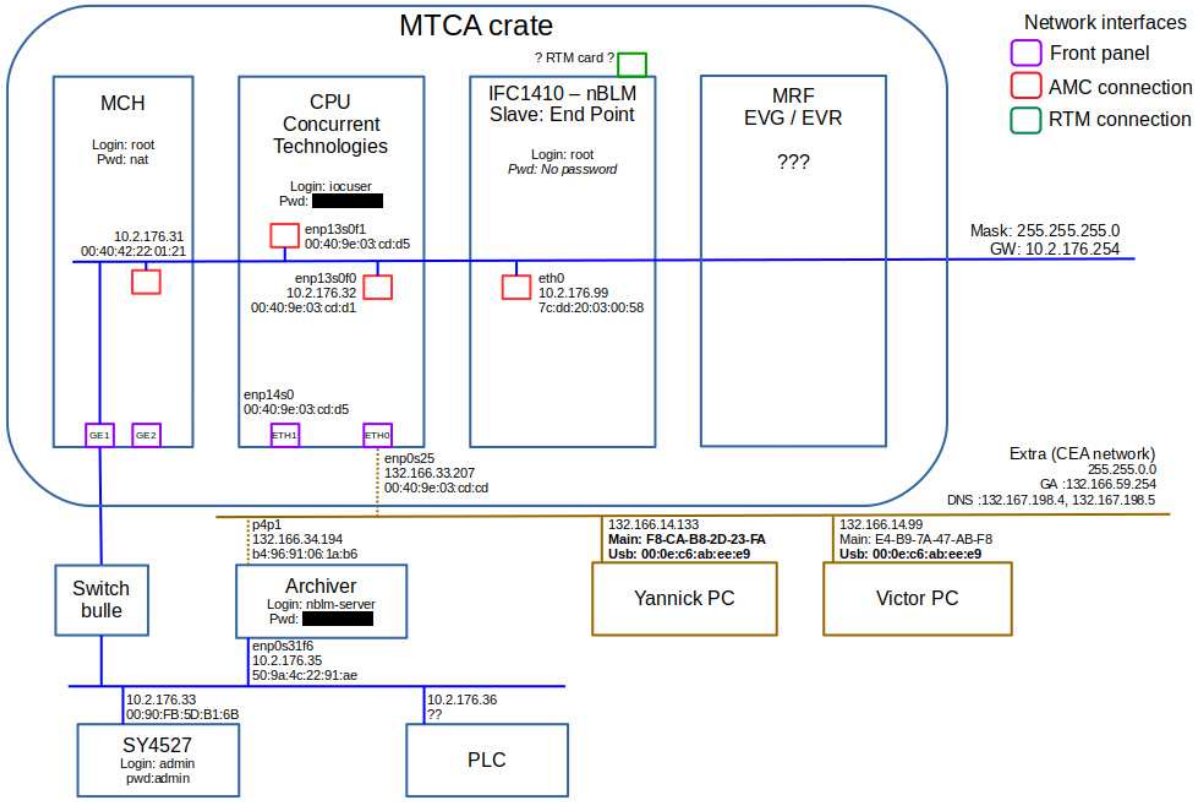

Figure 19 : *nBLM test stand with network interfaces*

For the gas, we will use one chassis and one distribution line at once (see the colored lines in the following figure).

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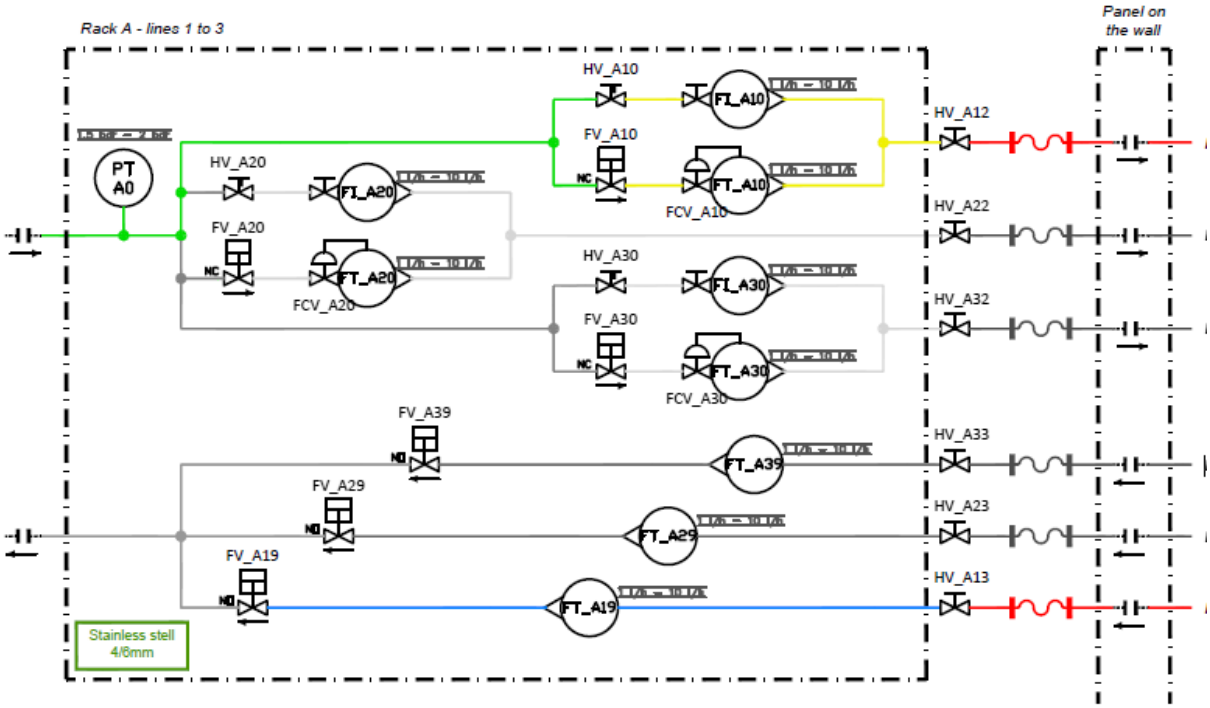

Figure 20 : Distribution gas chassis used for tests *in Saclay*

All the chassis components will be connected to the PLC. With this method, wiring, PLC software, lines switch and EPICS interface can be tested.

As said in chapter 3.1.3, for the Saclay tests we will use a Saclay version of PLC-EPICS communication server.

Over a second phase, we will add and test the main chassis.

4.3. Vertical integration tests in ESS of one nBLM

As mentioned before the tests will be the same but not applied to a test stand. We will use ESS infrastructure and equipment and test one nBLM detector.

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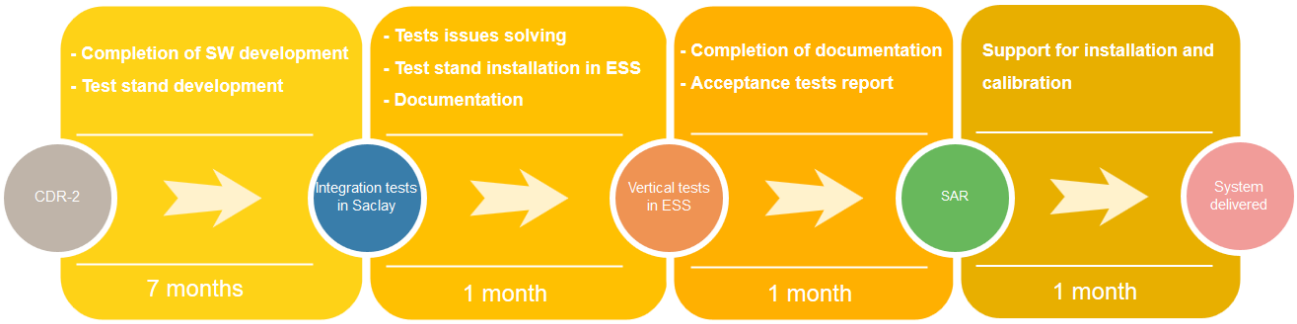
5. Control System planning

This following planning summaries the tasks to do from the control system point of view.



Details of the 2 first phases:

After CDR-2:

- Completion of acquisition development : conversion, file transfer, firmware update adaptation
- MRF development and integration
- Completion of PLC process development
- Software development for PLC gas (communication and database)
- CSS development for a complete system
- Individual test for each subsystem development
- Acceptance tests development
- Saclay test stand preparation : archiver, EEE/alarm server, gas chassis, MTCA

After Integration tests in Saclay:

- Migration to E^3 (depends on complexity and ICS support)
- Migration with PLC factory (depends on complexity and ICS support)
- Correction of issues
- Documentation
- ESS test stand preparation and installation

Moreover, note that each milestone is about 1 to 2 weeks of work.

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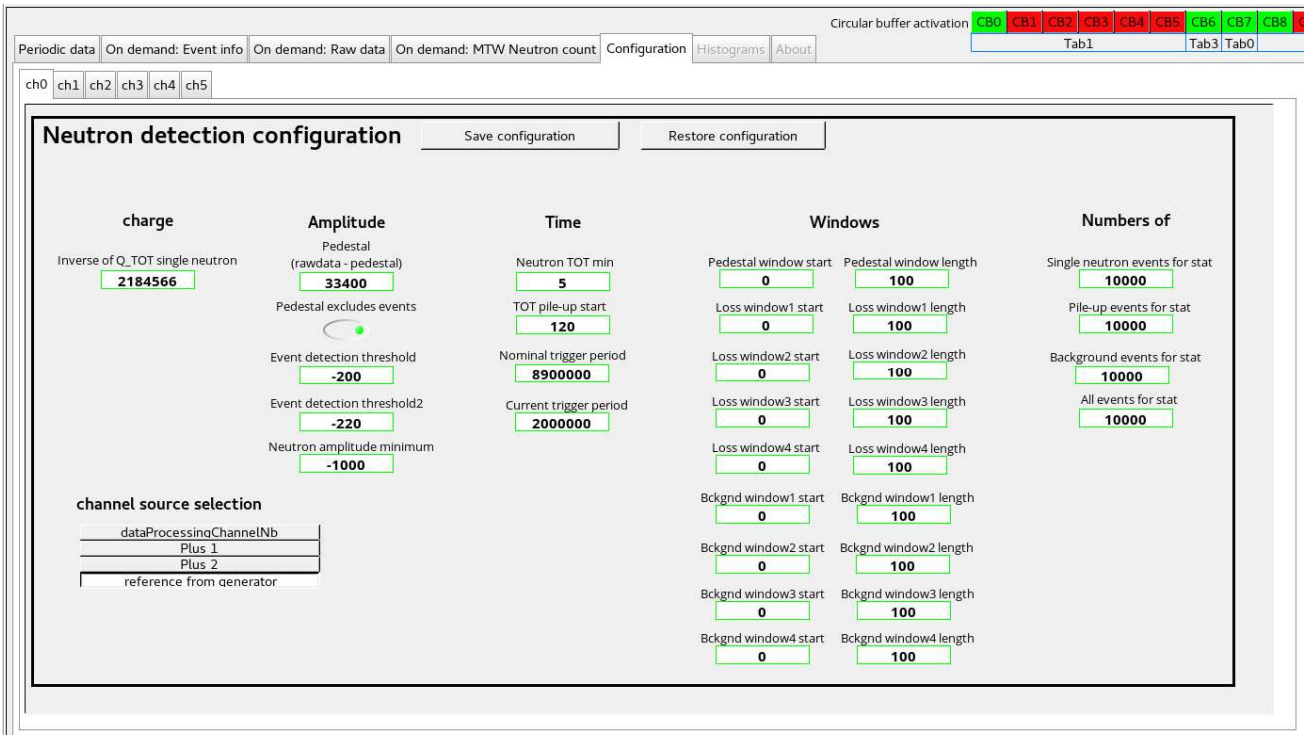
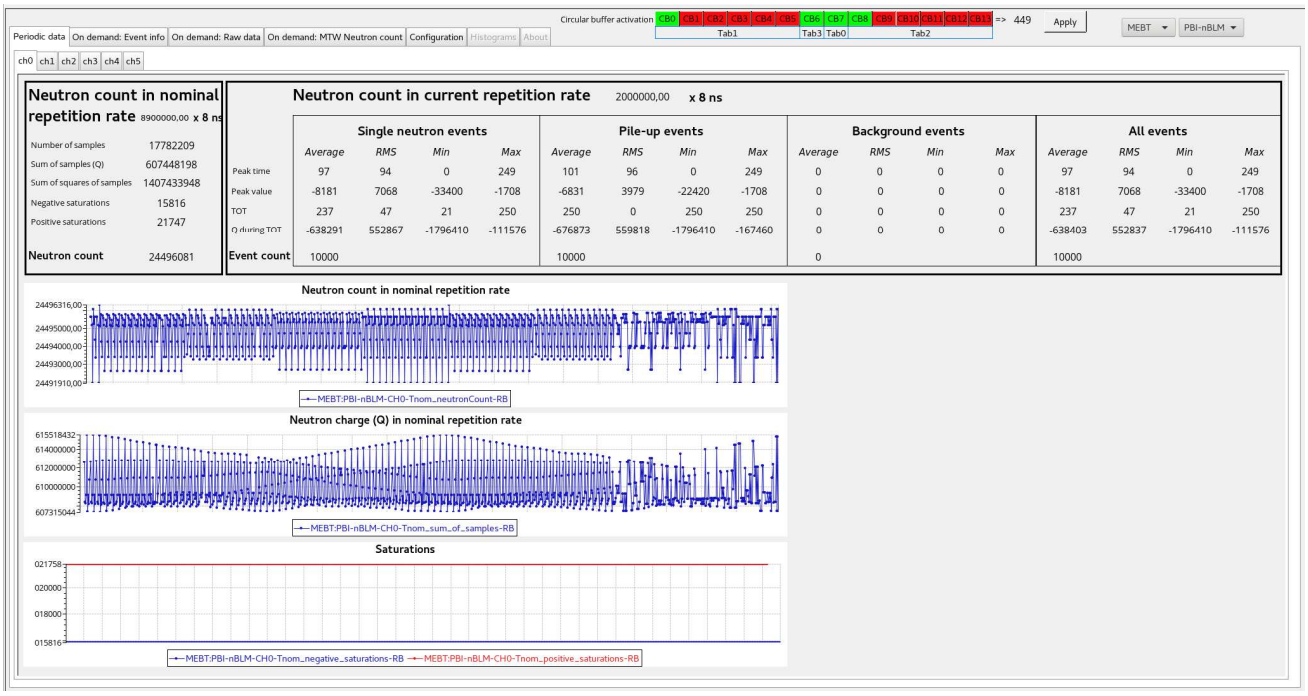
Appendix A - Preliminary CS-Studio view of the nBLM acquisition



Settings



Periodic data

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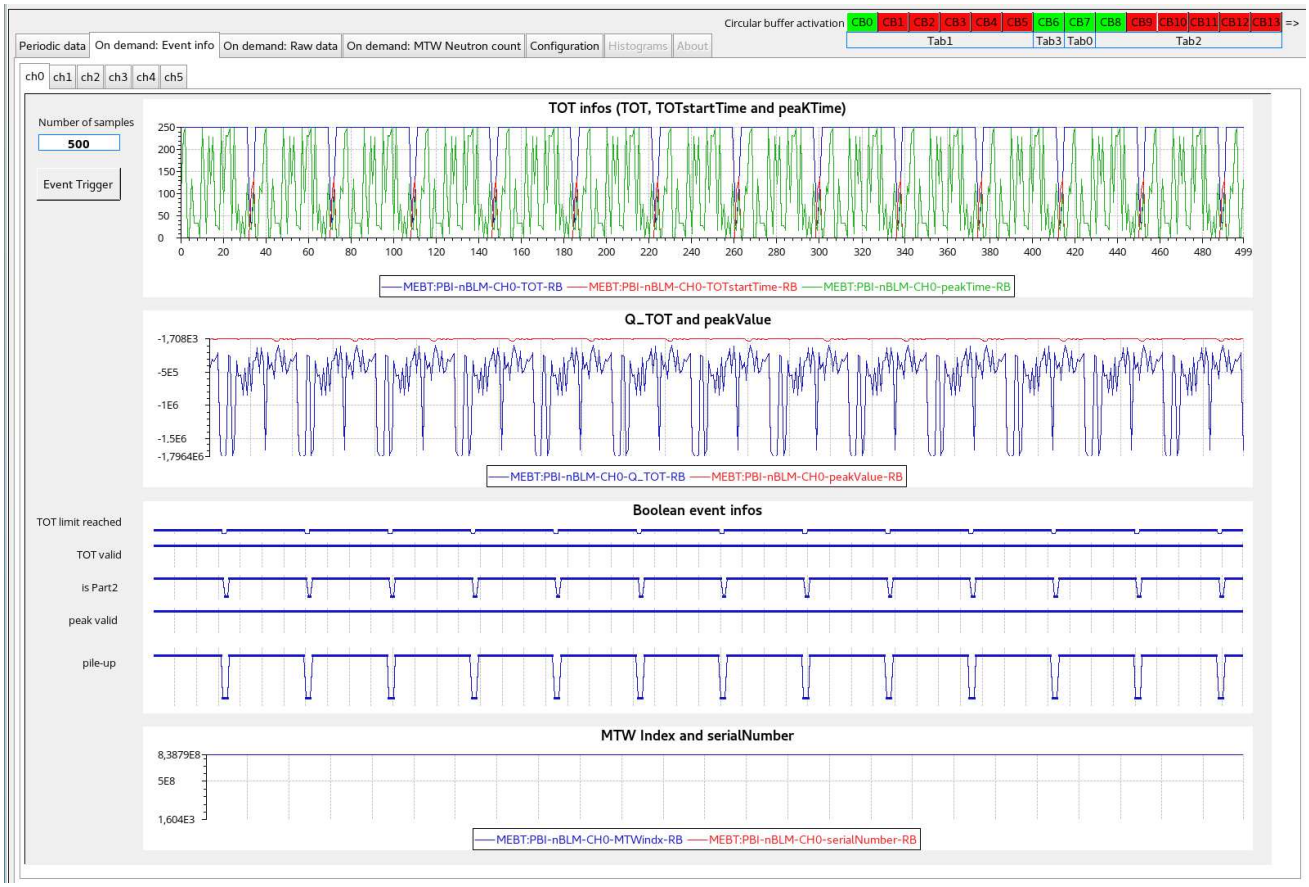
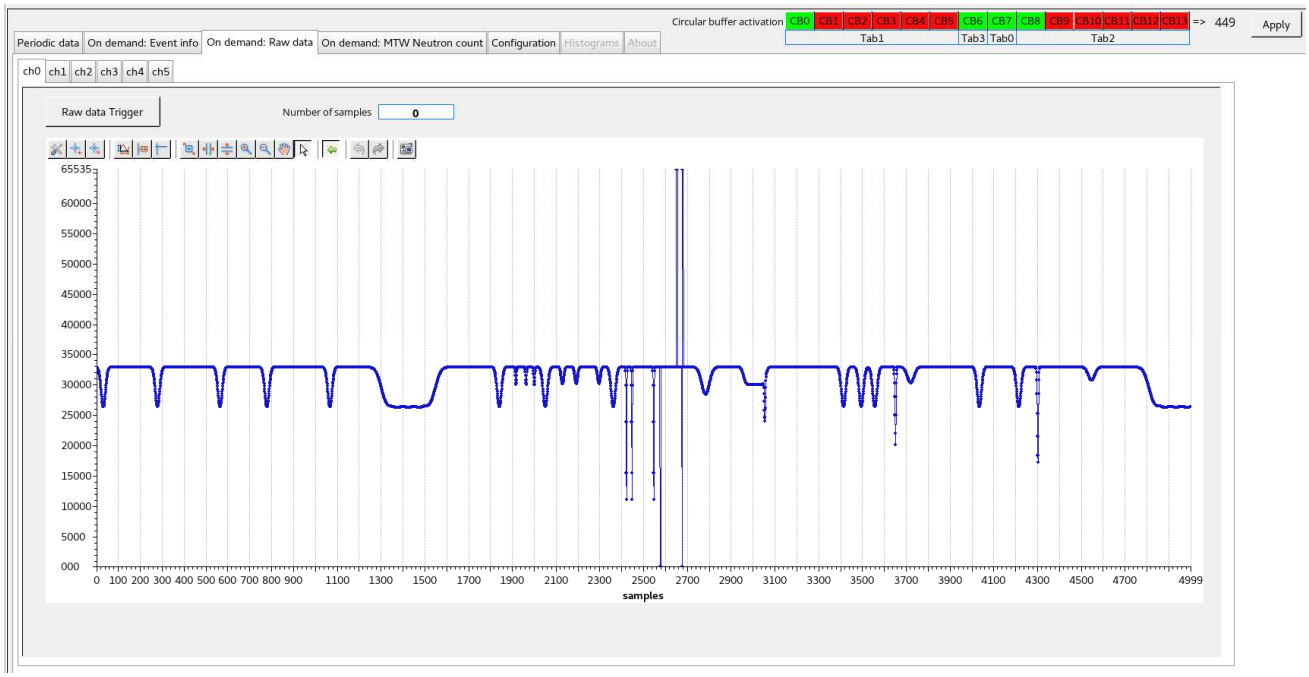


Event info: On demand with the “Event Trigger” button



Raw data: On demand with the “Raw data Trigger” button

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Monitoring Time Window Neutron count: On demand with the “Neutron count Trigger” button

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