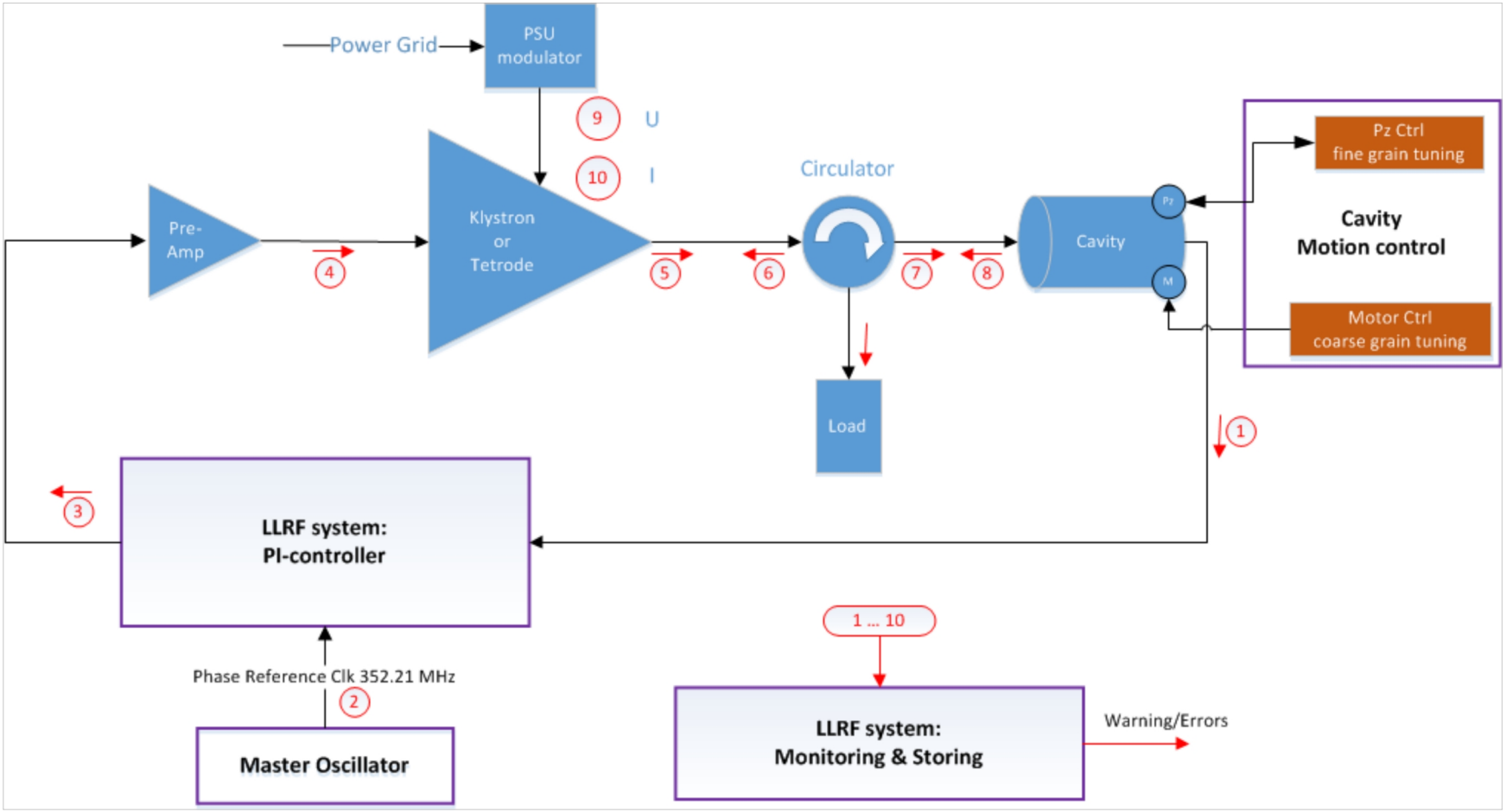
EUROPEAN SPALLATION SOURCE

ESS LLRF System – Baseline

ESS Bilbao CDR, Lund (19-01-15)

Christian Amstutz

LLRF Functionality



MTCA Crate

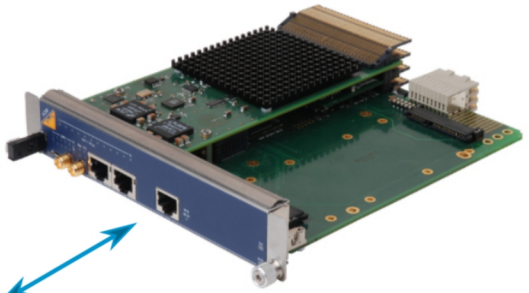
Struck DWC8VM1

Struck SIS8300-KU
(Xilinx Kintex UltraScale)

Concurrent Technologies
AM 90x AMC CPU

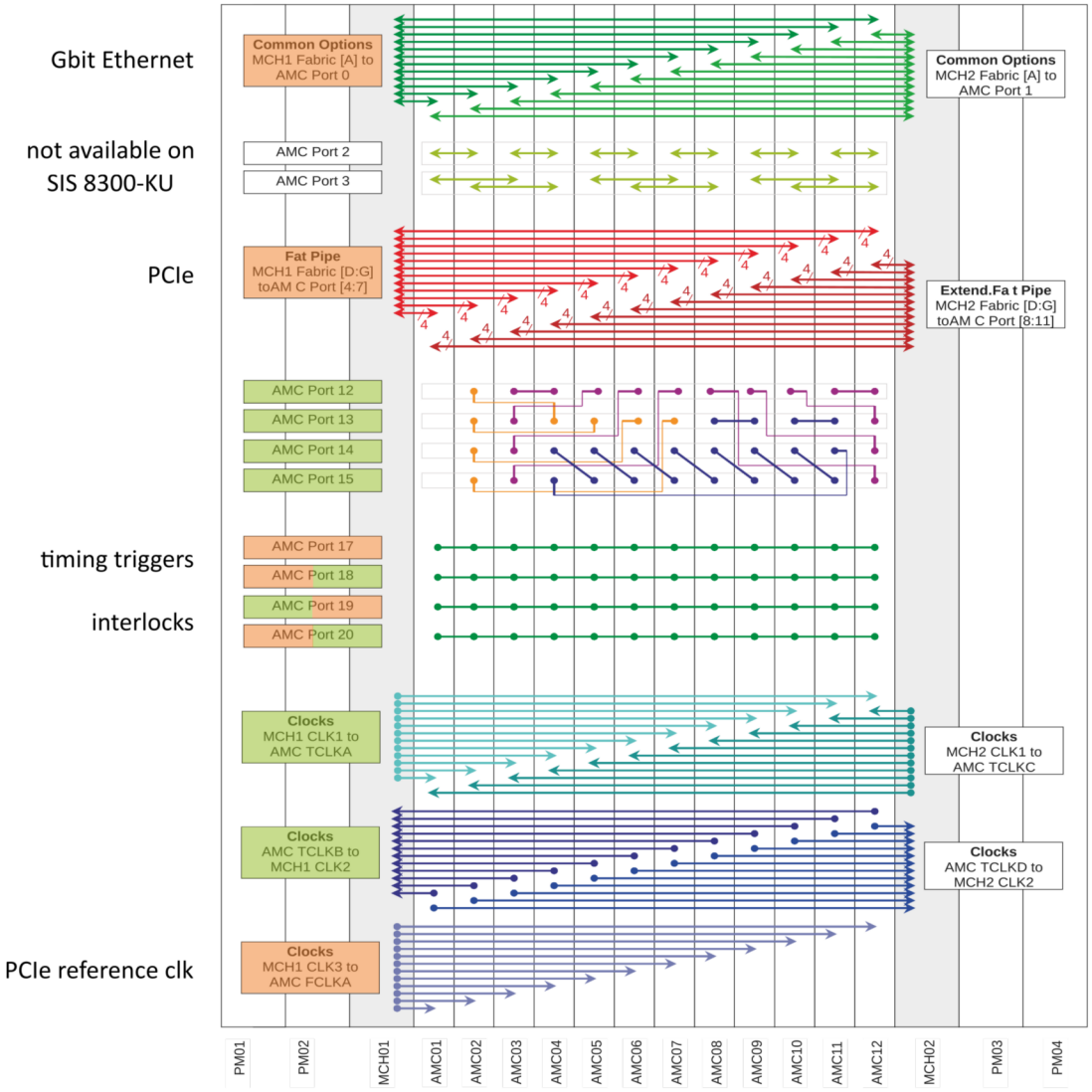
IOxOS IFC1410
(Interlock)

Schroff 12 slot MTCA crate



NAT MCH-PHYS

MTCA Backplane

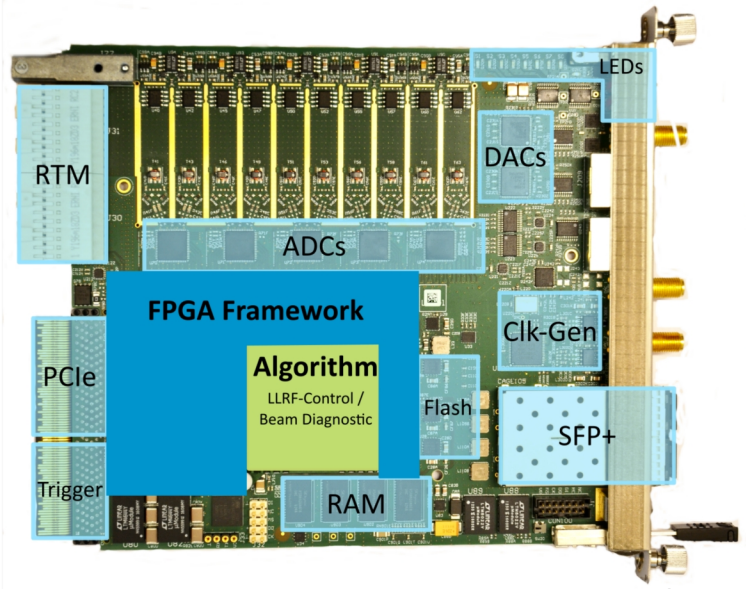


FPGA Framework – What is that?

Purpose: Enable access to the board peripherals

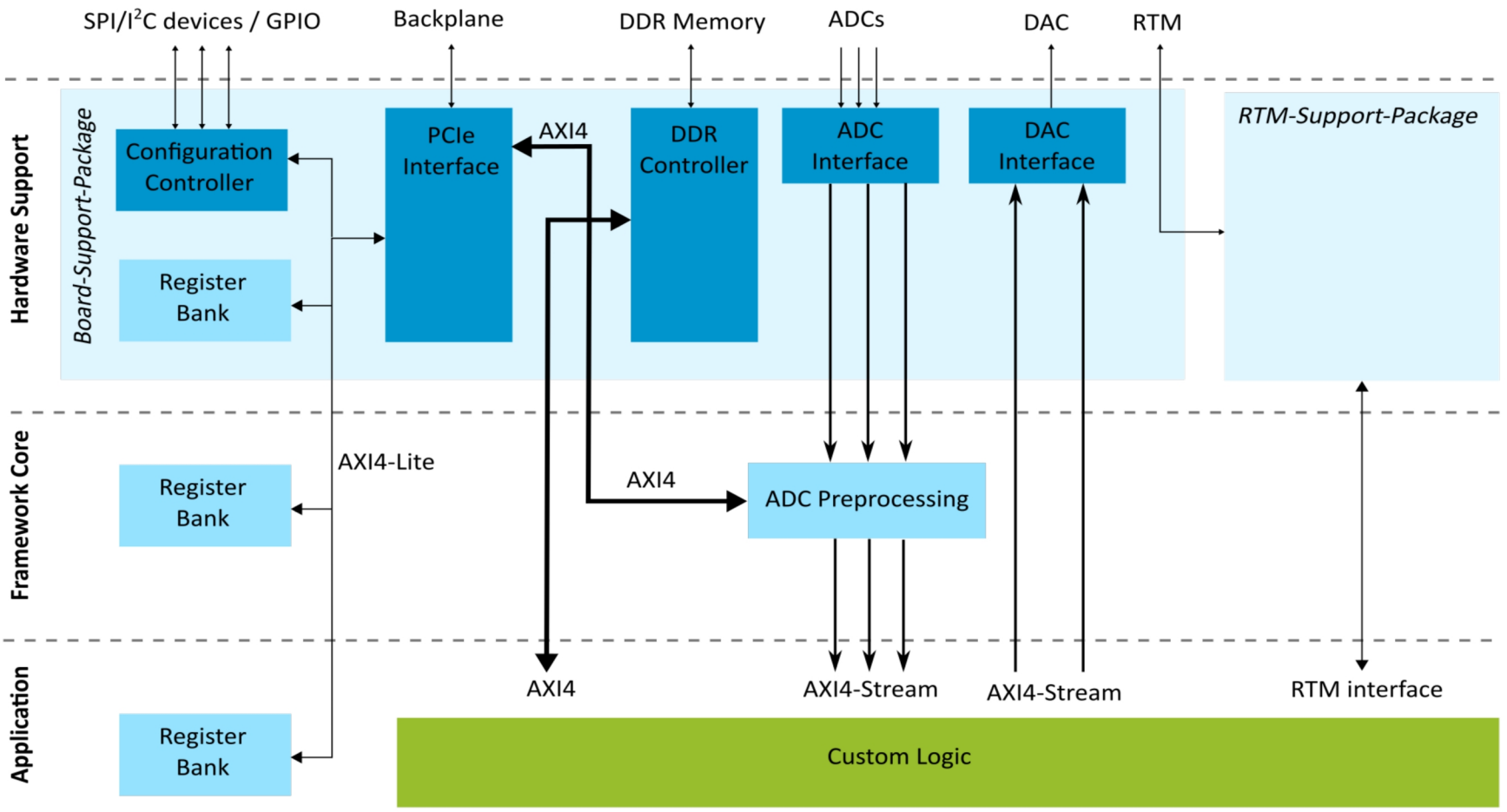
→ Operating system

- Flexibility → Different Boards / Different Applications
- Long-term support → Reduction of dependency
- Re-use of existing IP: Xilinx and ESS
- Application of industry standards → AXI4
- Design Guidelines and build scripts

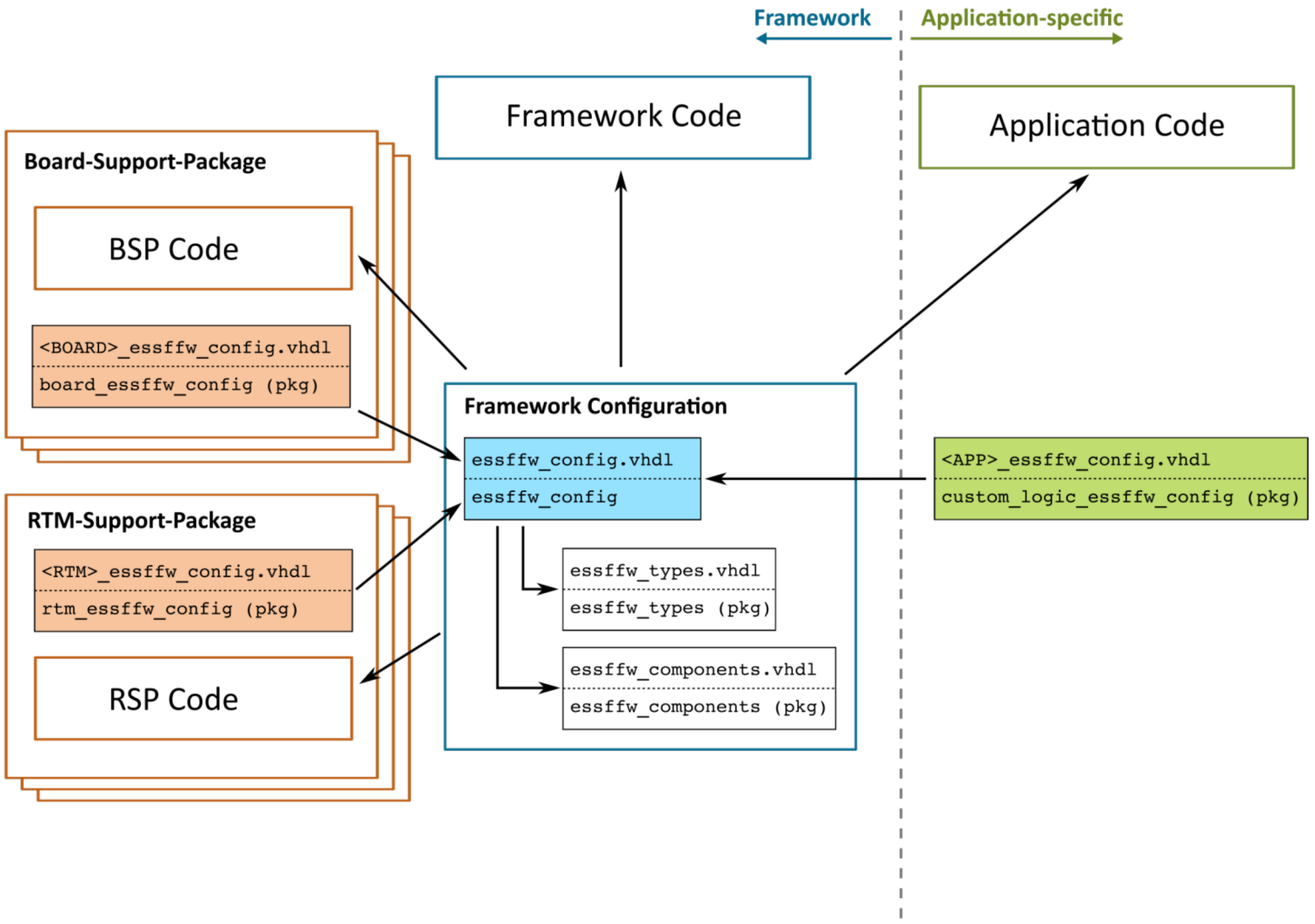


For changes : Approval necessary!

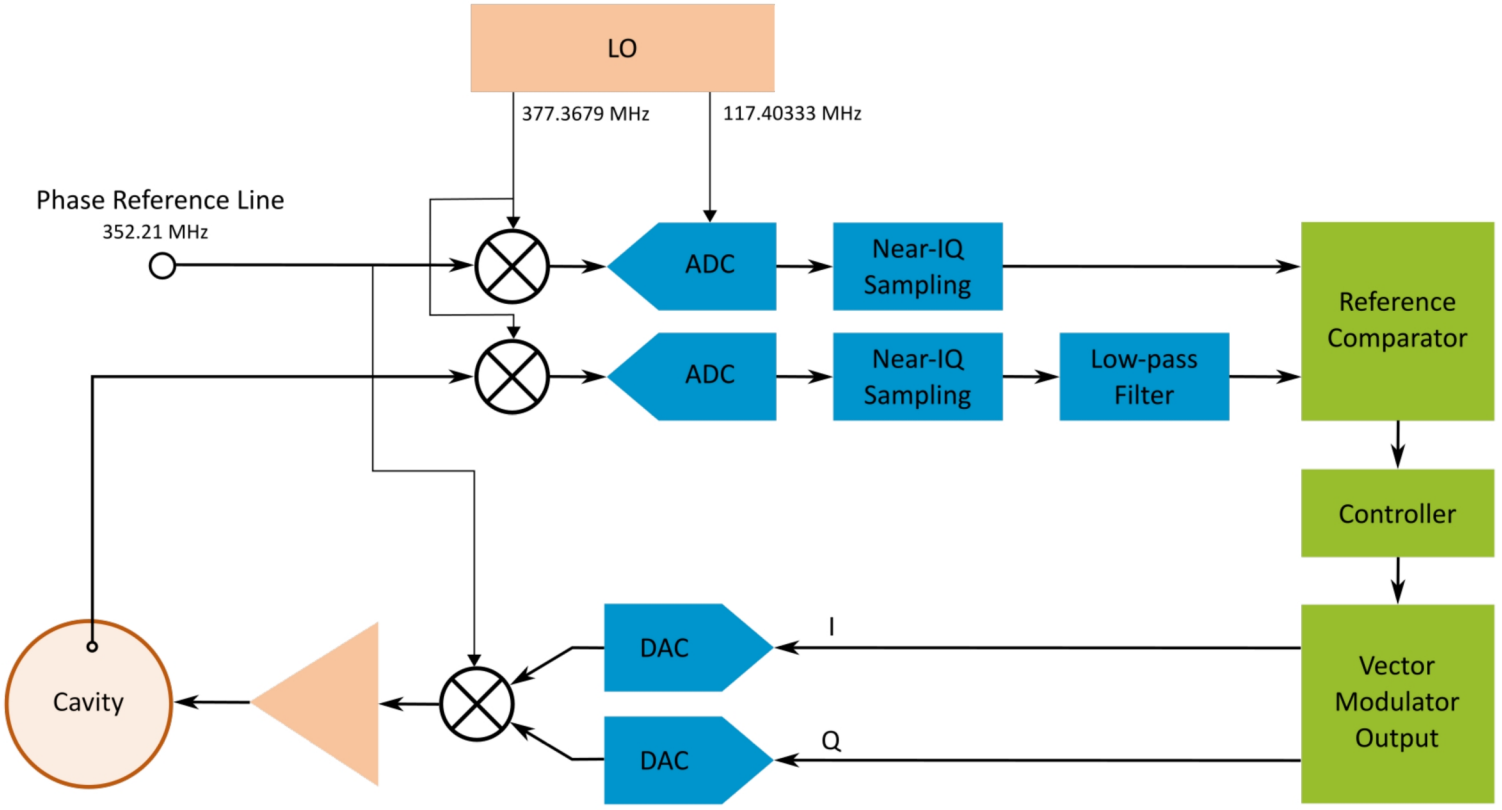
FPGA Framework Structure



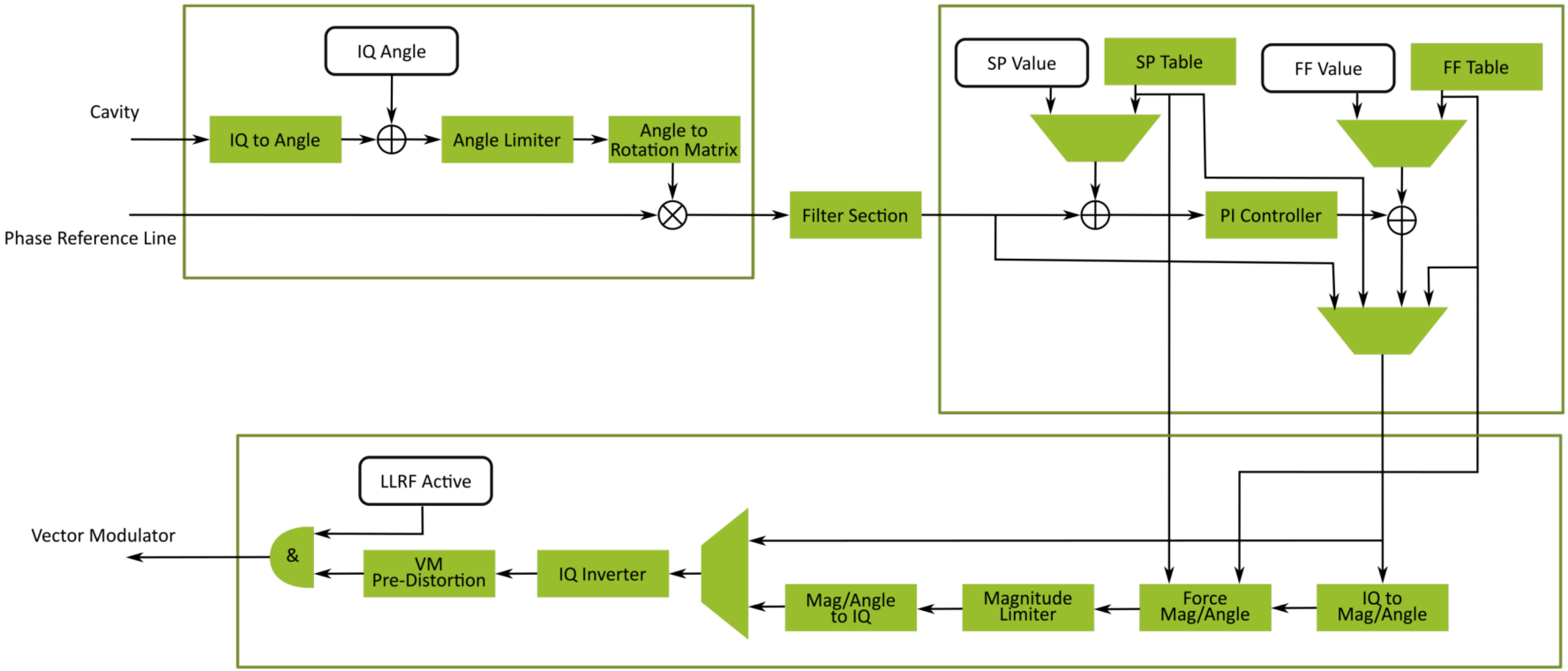
FPGA Framework Configuration



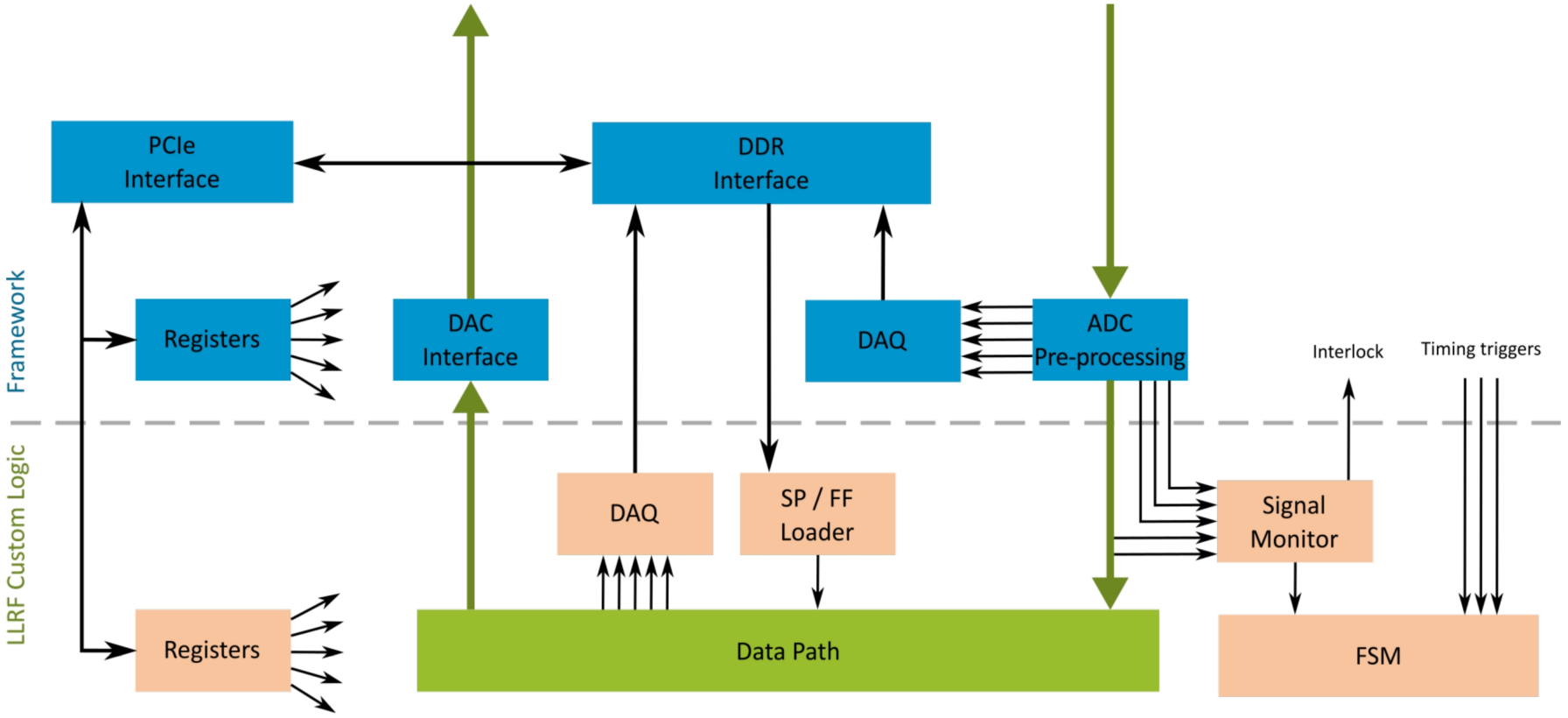
LLRF Signal Processing



LLRF Firmware - Datapath



LLRF Firmware – Support Functions



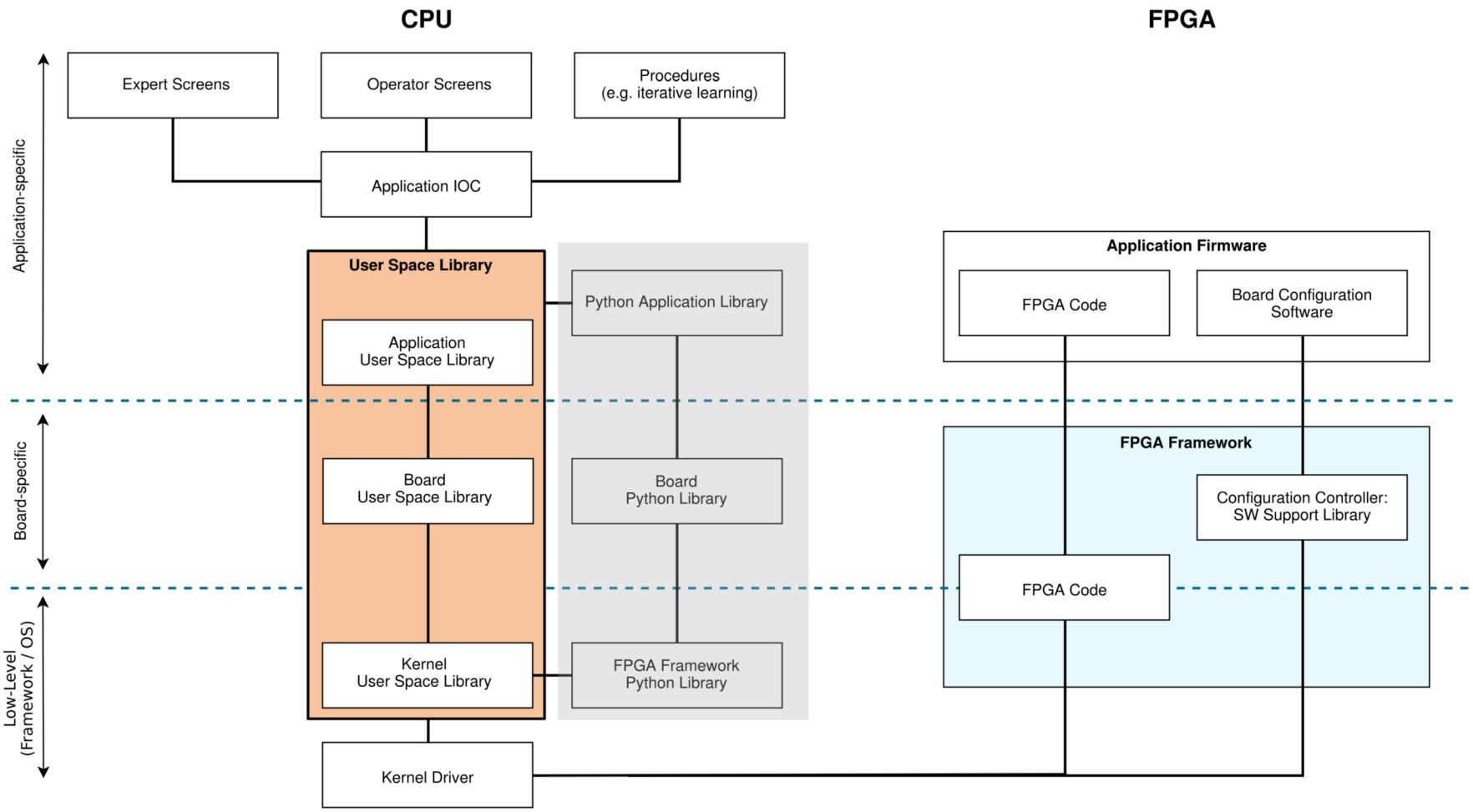
Lund LLRF Firmware: Roadmap

- IQ signal generator ✓
- Open-loop with VM signal ✓
- Closed-loop with PI and feed-forward ✓
- Closed-loop with PID controller
- Closed-loop plus inner loop PI controller
- Closed-loop, inner loop plus linearization

Proposed Firmware Workflow

- Include adaptions to baseline into the same project
- Same Repository / different branch
  - Separate project file
  - Updates to baseline can be easily included
- Design guidelines as defined by the FPGA Framework
- Test benches for different modules

Control System Integration



Summary

LLRF baseline functional in basic version

→ ESS Bilbao changes can be included

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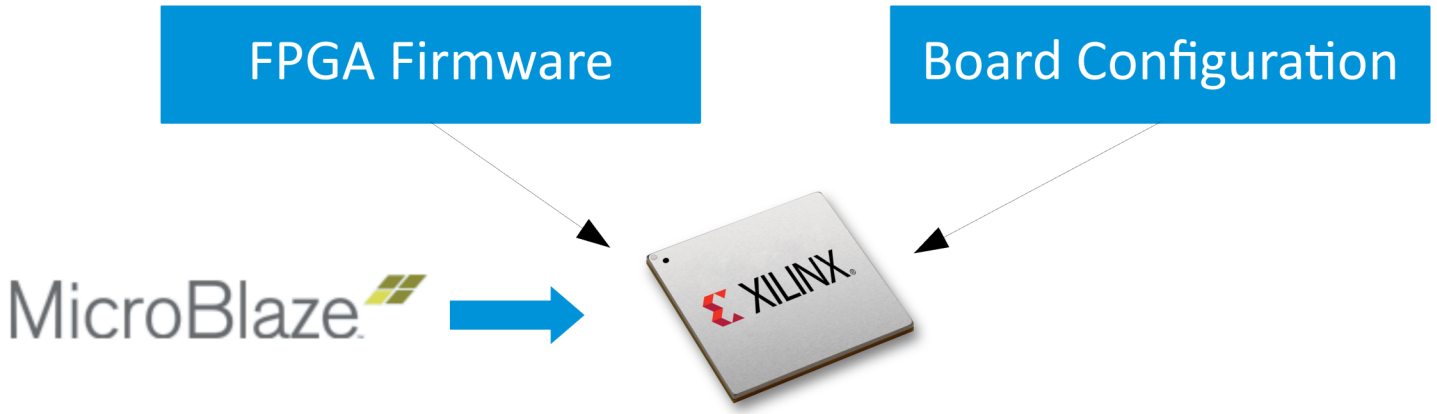
Thank you

Backup

Configuration Controller – Concept

→ Board Configuration is fairly static for one application



- Usage of Xilinx IP blocks for SPI, I2C, GPIO
- Adaptations to the serial protocols (SPI, I2C) made in software
- Separate board configuration from driver functionality

HW/Firmware developer

Software developer

AXI4 Bus

- Part of the open-standard AMBA bus family from ARM
- On-chip interconnect: High bandwidth / low latency
- Highly configurable:
  - Read-only / read-write
  - Width of data lane
- 3 types:
  - AXI4
  - AXI4-Lite
  - AXI4-Stream
- Official bus in Vivado IP Integrator