The ESS WS OFE

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Introduction

Themes:

- OFE specifications
- OFE the final VIT test

OFE Specifications

Current to voltage converter specifications:

- low-voltage noise JFET-input stage
- Power supply -5V to +5V
- High Gain Bandwidth Product 1.6 GHz
- High Bandwidth 275 MHz
- Slew Rate 700 V/µs
- Operating Temperature Range –40° C to 85° C
- Low-Input Offset Voltage ±250 µV
- Low-Input Bias Current 2 pA
- Low-Input Voltage Noise 4.8 nV/√Hz
- Input noise current 1.8 pA/√Hz
- High-Output Current 70 mA
- Sensitivity 1nA/mV

Si Photo Diode (PD) Hamamatsu S1226-44BQ

- Photo sensitivity area 3.6 x 3.6 mm
- Operating temperature -20 to +60 deg. C
- Spectral responce range 190 to 1000 nm
- Peak sensitivity wavelangtht 720 nm
- Photosensitivity 0.36 A/W
- Dark current 10 pA
- Terminal capacitence 500 pF

Avalanche Si Photo diode (APD) Hamamatsu S5544

- Photo sensitivity area 3.0 mm diameter
- Operating temperature -20 to +60 deg. C
- Spectral response range 200 to 1000 nm
- Peak sensitivity wavelangth 620 nm
- Photosensitivity 0.42 A/W
- Dark current Typ 1 nA max 30 nA
- Terminal capacitence 120 pF
- Bias voltage - Gain 0 – 120 V typ 50V DC

Power Supply

- Main power supply (BEmod) -5V --- +5V
- Main current max -100 mA --- +200 mA
- Bias High Voltage (BE) 0 V to max +120V DC
- Operating temperature -30 to +60 deg. C

Mechanical specifications

- Alluminium milled unibody case
- Mechanical dimension 19 inch 2U rack mount case
  W-483mm H-88mm D-50mm
- Weight 1934.35 g

The test equipment

Signal generator: Agilent AFG3252

- Function: pulse
- Frequency: 14 Hz
- Pulse width: 50us
- Amplitude low: 0V
- Amplitude High: 0.8 to 2.5V

Light source for VIT test:

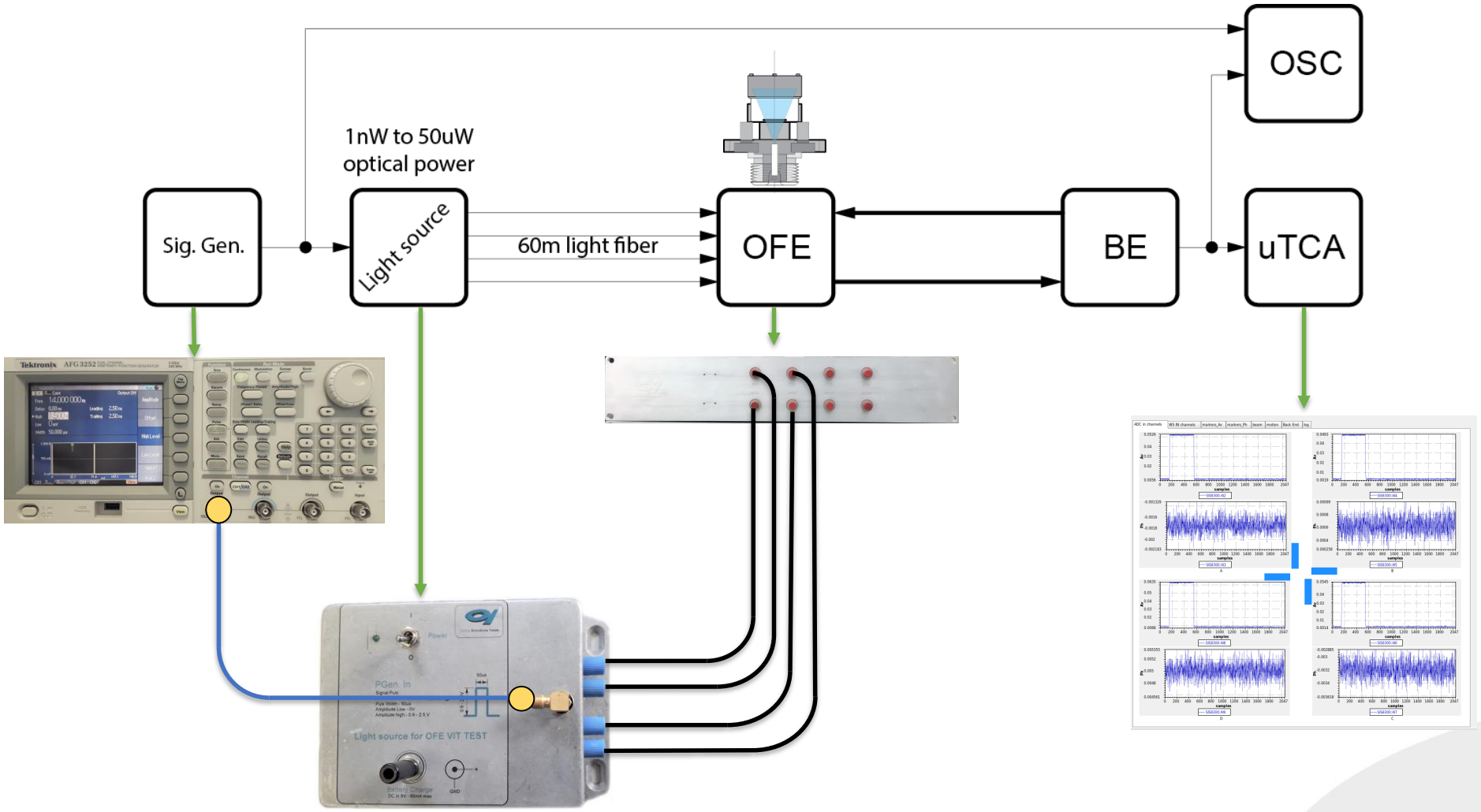
- Pulse generator input: as above
- 4ch optical output: = ~1nW – ~50 uW optical power +- 2.5%

ADC board:

- Struck Si8300-l2, sampling rate 10MS/s

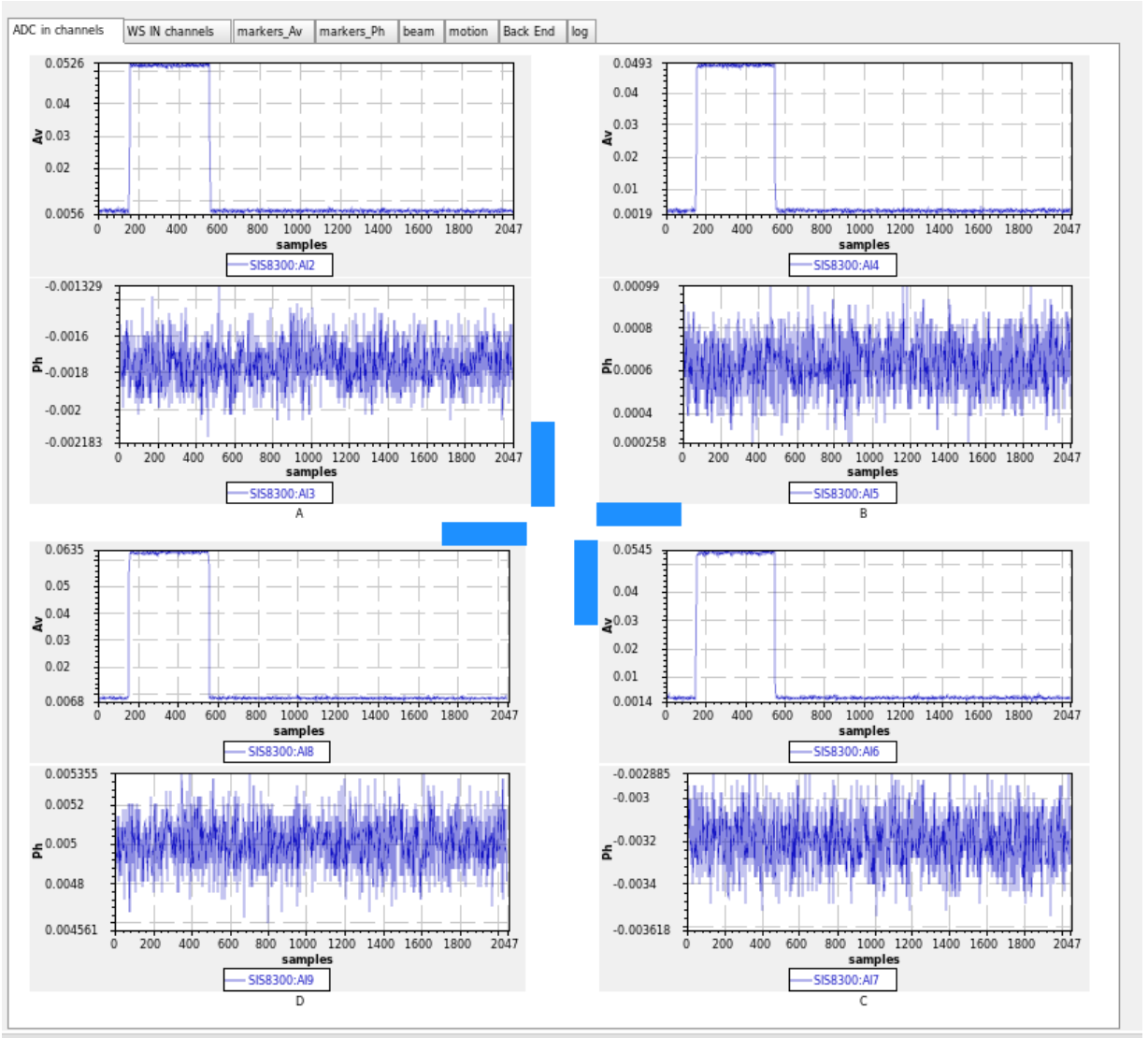
•MTCA.4 (µTCA for Physics Implementation)
•4 lane PCI Express Connectivity
•10 Channels 125 MS/s 16-bit ADC
•10 MS/s to 125 MS/s Per Channel Sampling Speed
•AC and DC Input Stage
•Internal, Front Panel, RTM and Backplane Clock Sources
•Two 16-bit DACs for Fast Feedback Implementation
•High Precision Clock Distribution Circuitry
•Programmable Delay of Dual Channel Digitizer Groups
•Gigabit Link Port Implementation to Backplane
•Twin SFP Card Cage for High Speed System Interconnects
•Virtex 6 FPGA
•Dual boot
•MMC1.0 under DESY license LV91
•2 GByte DDR3 Memory (flexible partitioning scheme)
•In Field Firmware Upgrade Support
•Zone 3 class A1.0, A1.0C or A1.1CO compatible (see below)

The test configuration



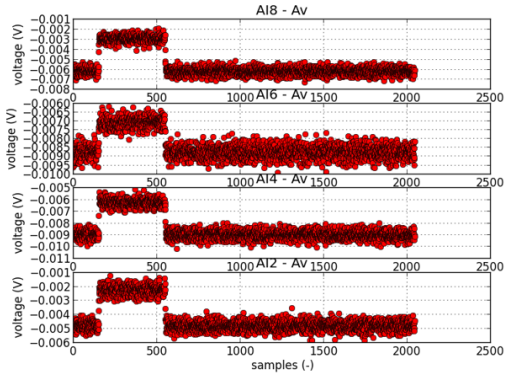
The test

The Struck board acq display results

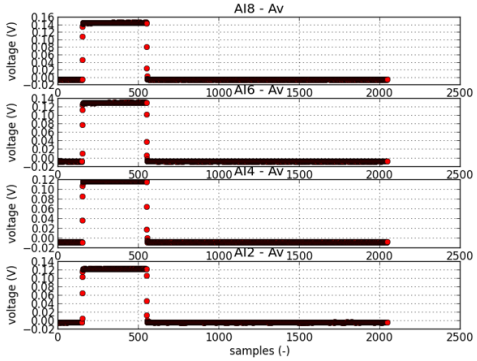


The test

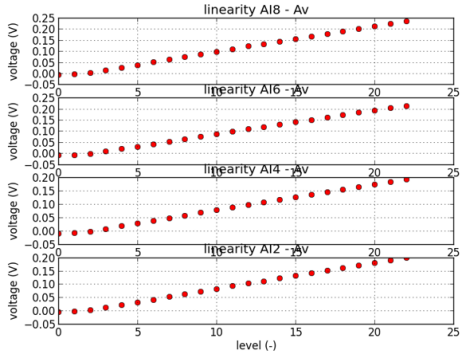
BE-OFEtest-undef 2019-01-30 18_03_48.html



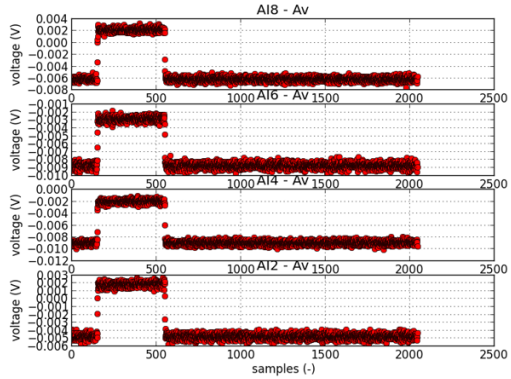
0.9 V gen. sig.



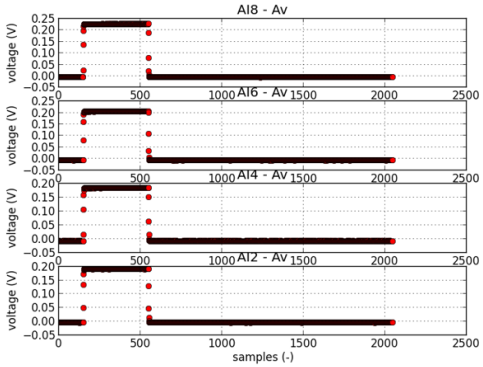
3.4 V gen. sig.



Linearity of full scale



1.0 V gen. sig.



4.6 V gen. sig.

Conclusion

- The test confirm a very stable response
- The signal is clean and sharp
- Very low noise
- Large bandwidth – 1.2MHz
- High sensitivity 1nA/mV
- A very solid and purposely designed case to match detectors specifications
- A modular design for a future upgrades and configurations
- All 9 units are assembled and will be delivered by the end of the year 2019
- A light source (shown in this presentation) will be also delivered with the units

OFE images

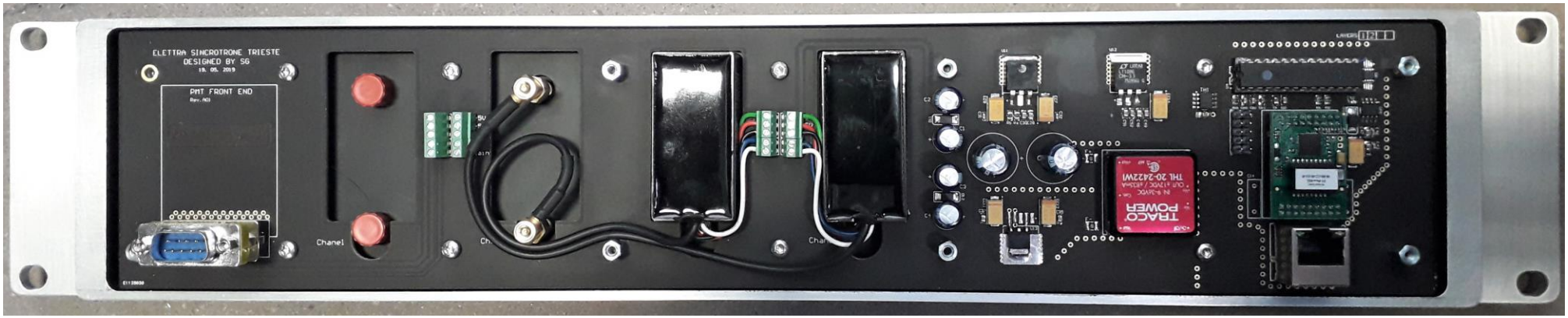

CH4
CH3
CH2
CH1
CH8
CH7
CH6
CH5


PD1
PD2
PD3
PD4
APD1
APD2
APD3
APD4
Optical Front End


NOTICE
DO NOT OPEN.
OFE


Power
PGen In
Light source for OFE VIT TEST
GND

One more thing - SFE



A new standalone Scintillator Front End with PMT tubes

- Gain to 10^7
- Controller on board with Ethernet protocol
- Compatible with existent control system
- All powers on board
- Power over Ethernet is possible
- Low voltage external power source 4W DC max ratings

Thank you !