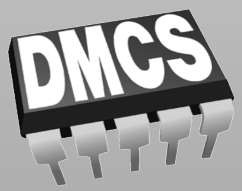
Status of applications on the IOxOS platform

Grzegorz Jabłoński for the TUL DMCS Team

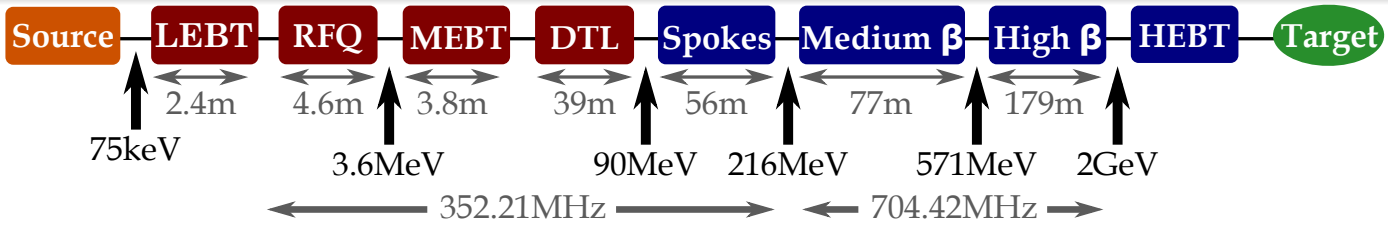
Lodz University of Technology, Poland

22.10.2019



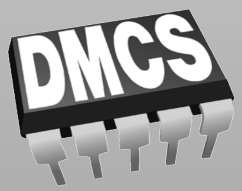
xBLM

- BLM systems are designed to detect showers of secondary particles produced by lost beam particles interacting with the accelerator equipment.
- BLM systems play an important role in machine protection from beam-induced damage by detecting unacceptably high beam losses and promptly inhibiting beam production.
- To be effective, they need to react within a few microseconds
- The ESS BLM consist of two types of systems, differing in detector technology.
- The ICBLM system is based on 266 ionisation chambers as detectors, located almost exclusively throughout the SC parts of the linac. They operate in current mode.
- The nBLM system consists of 82 neutron detectors, specially designed to primarily cover the lower energy part of the ESS linac. They operate in pulse mode.



Work scope

- Polish in-kind contribution
- Contract with ICS with 3 workpackages
- Workpackage 2 done in strict collaboration with BIG
- Firmware for nBLM
- Firmware, IOC and EPICS panels for ICBLM
- In practice, also test software and reference implementation of low-level software components (data transmission, integrity checking, decoding and archiving) for nBLM
- Algorithm for pulse discrimination and its reference implementation provided by BIG
- Firmware framework provided by IOxOS

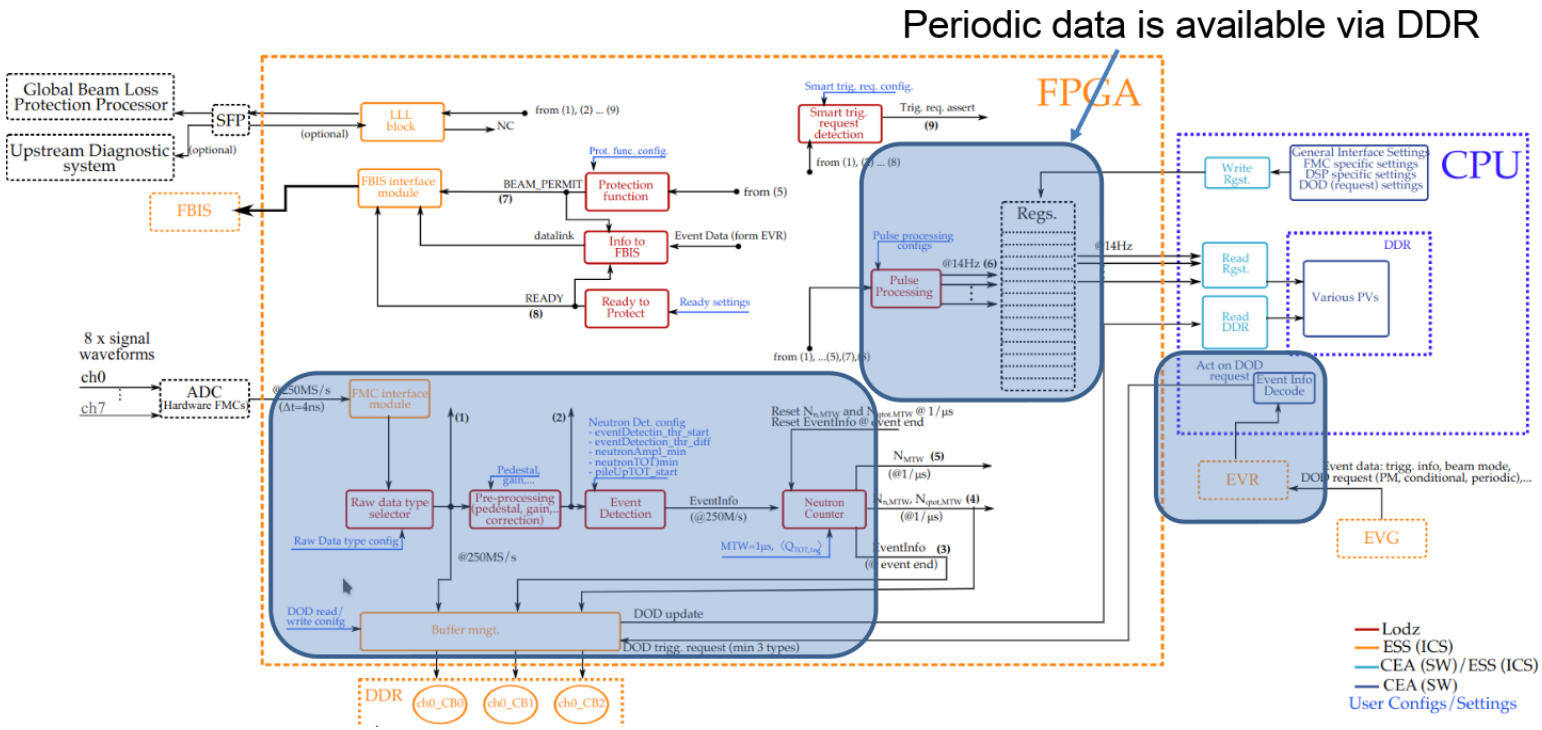


xBLM BEE hardware platform: IOxOS IFC_1410 + ADC FMCs

- 2 banks of 512 MB DDR3 memory
- T2081 POWER processor
- XCKU040 FPGA
- PCIe interface
- 2 FMC Slots for ADCs
  - 2 customized 1 MHz Pico 1M4 for ICBLM (8 channels)
  - single 250 MHz AD3111 for nBLM (8 channels)

nBLM implementation status

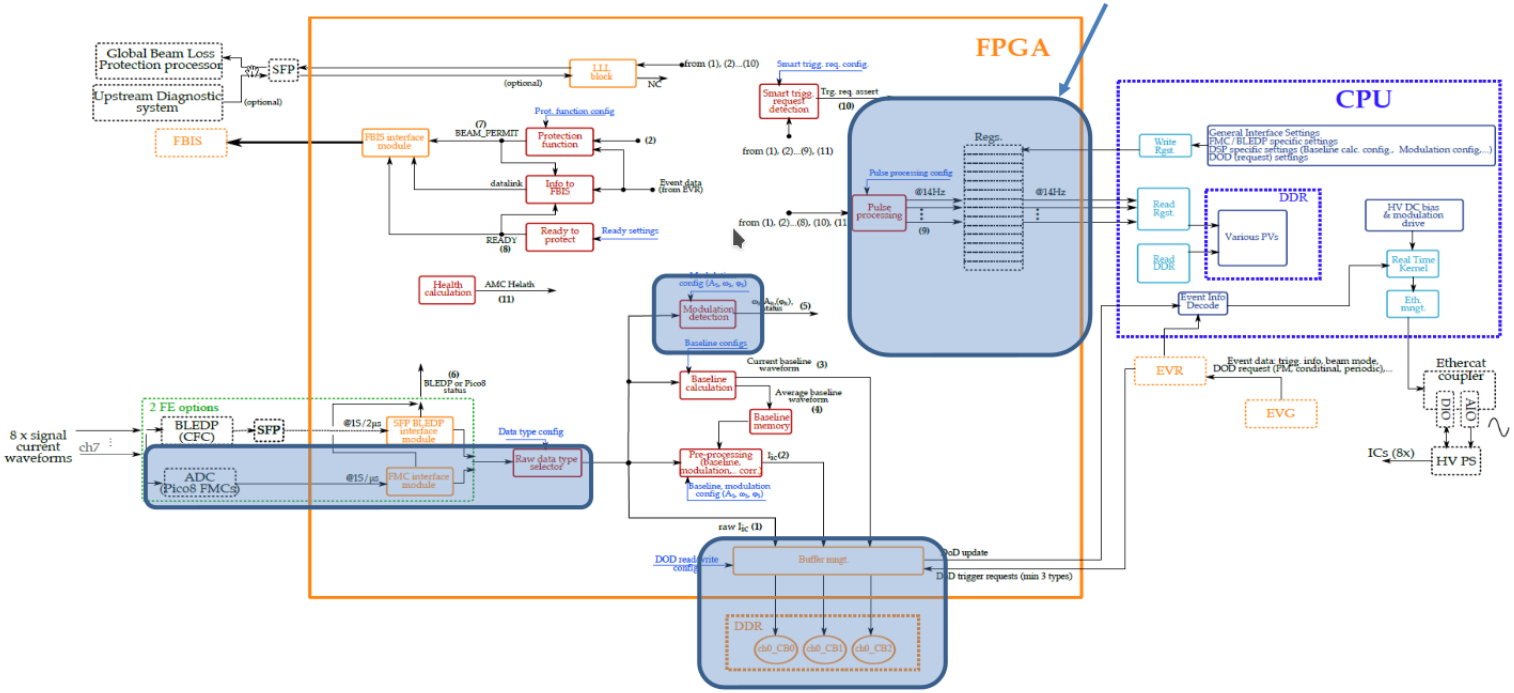
Grzegorz Jabłoński



ICBLM implementation status

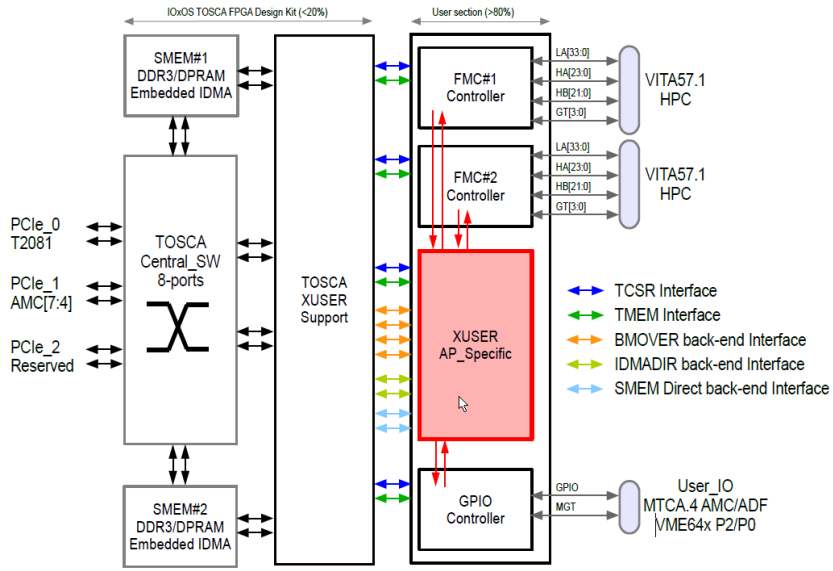
Grzegorz Jabłoński

Periodic data is available via DDR



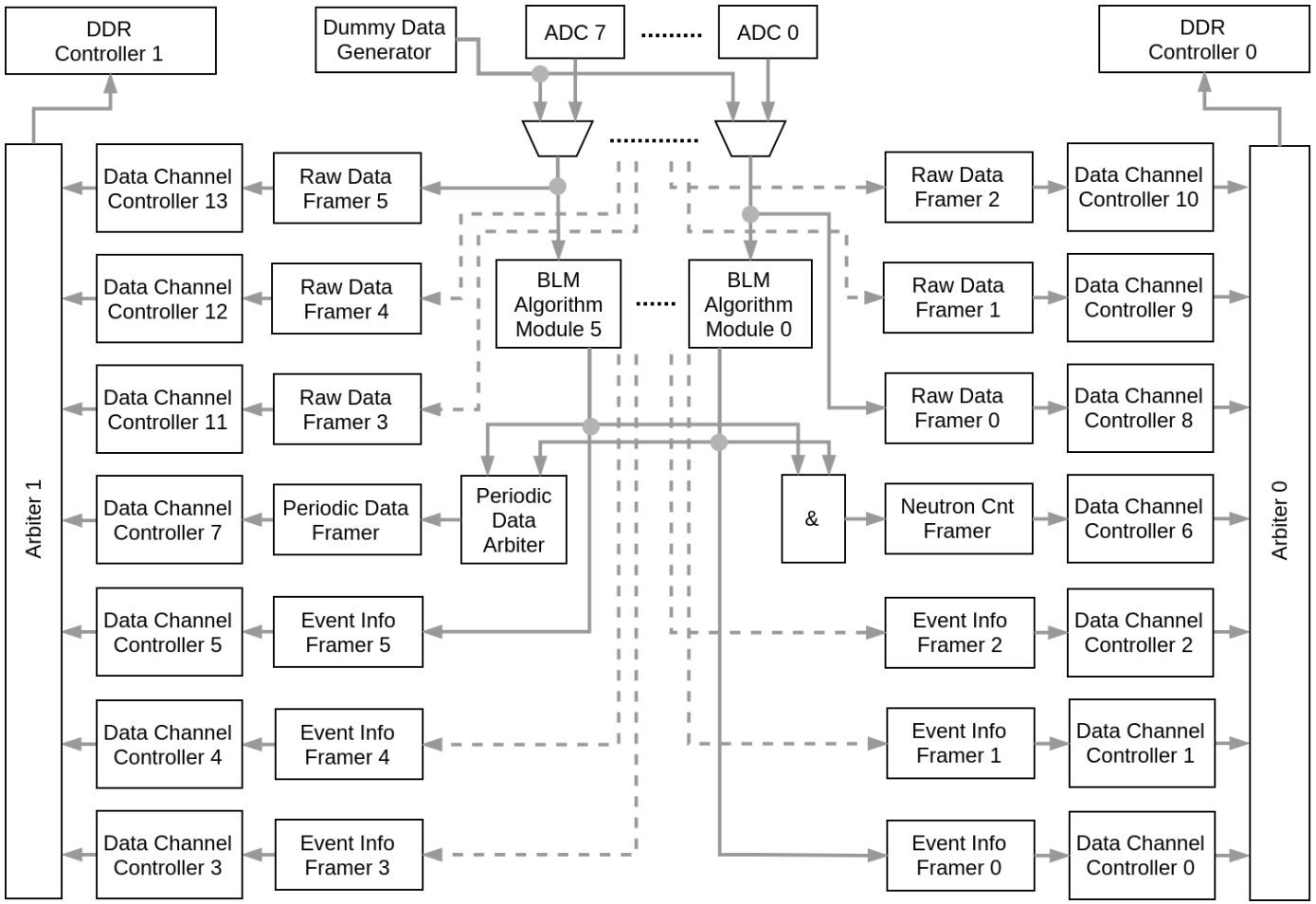
Hardware-software interface

- Using circular buffers in DRAM to stream data to CPU
- Using TSCR interface for control and algorithm parameters
- Two DDR banks @275 MHz via SMEMDIR interface, 2000 MB/s bandwidth each
- DDR-to-CPU DMA bandwidth of 1000 MB/s total



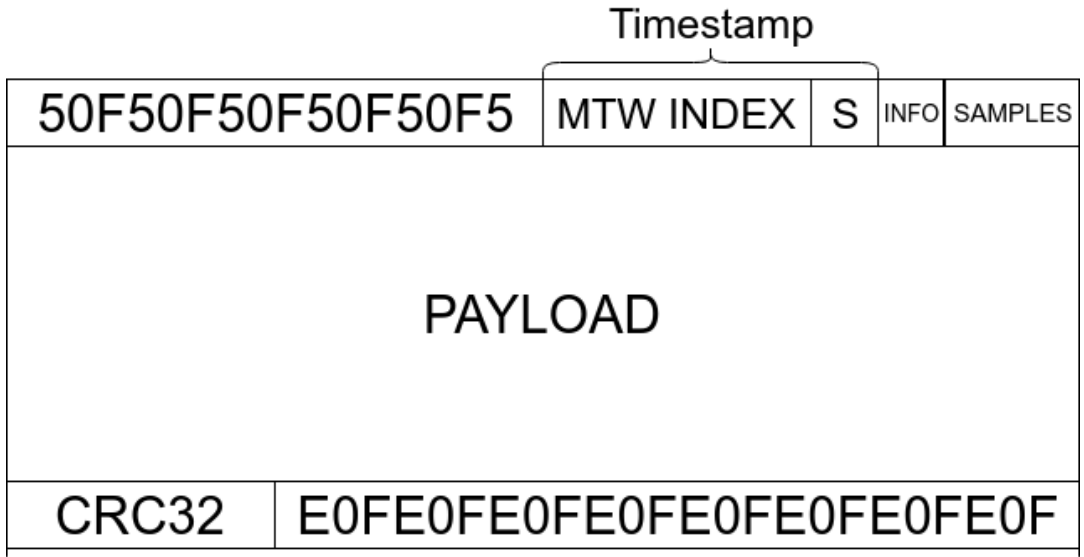
Data transmission protocol layers

- Circular buffers – stream of unstructured data
- Data frames – timestamping and integrity check
- Periodic data – content-specific header



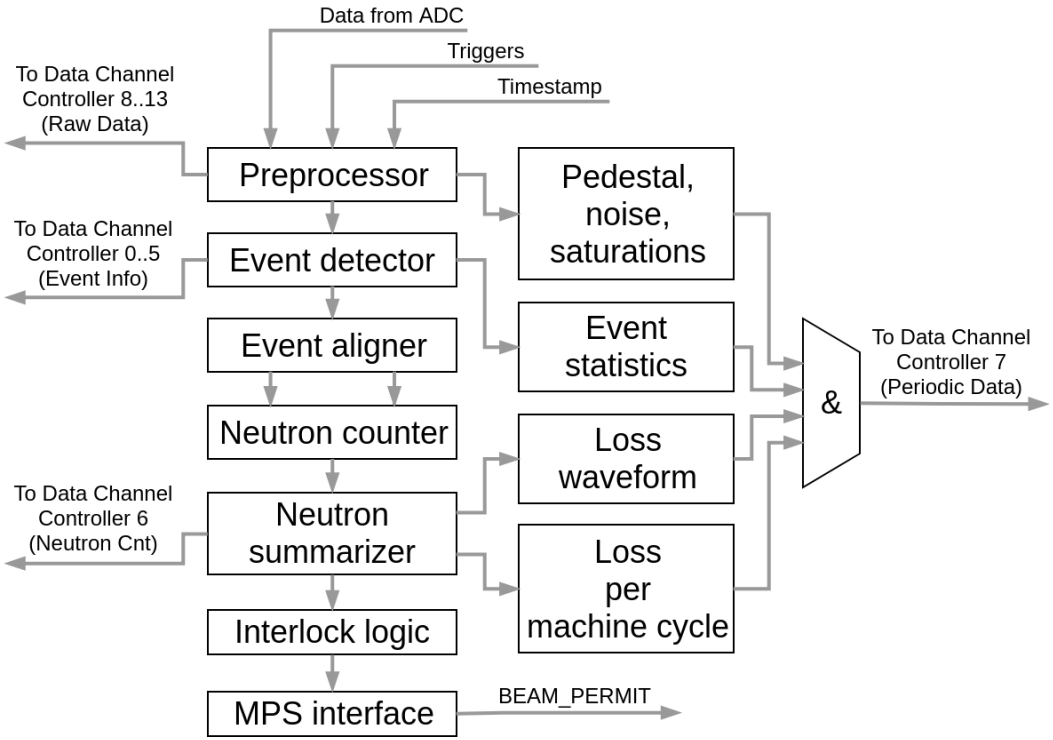
Frame layout

- Start-of-frame pattern
- Timestamp
  - Serial number of the 1-microsecond window
  - Sample index within the window.
- 1 generic information byte
- 16-bit number of samples in the frame
- Payload packed back-to-back on the bit level without any additional padding
- 32-bit CRC of all the previous words in the frame followed by the End-of-frame pattern.



nBLM algorithms block diagram

- Main flow – 5 pipelined processing blocks
- Implemented in C++ with High Level Synthesis
- Data timestamped by MTW number and sample number within MTW (unique within more than 1 hour)
- All components, apart from interlock logic and MPS interface, implemented

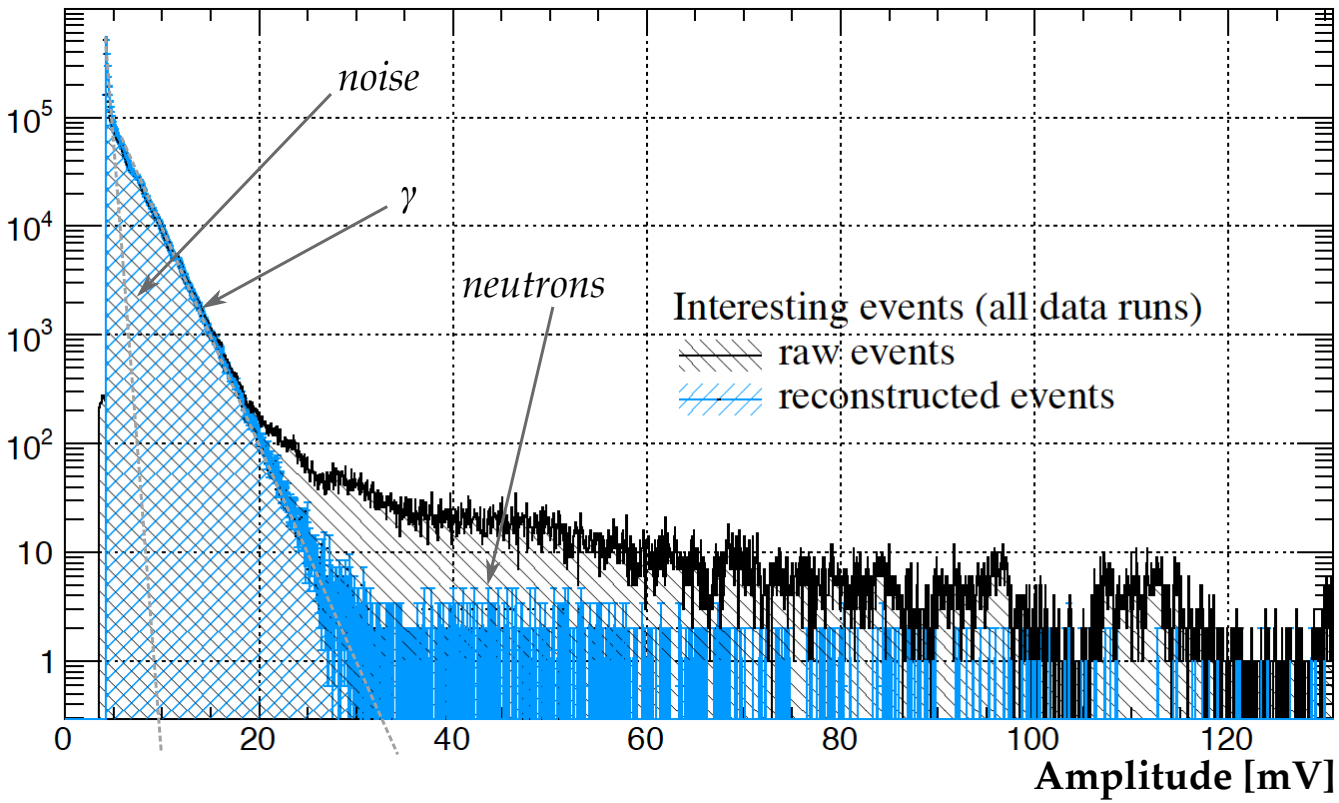


Timestamping

- There are three kinds of timestamps in the system:
  - FPGA Internal - MTW number (32-bit) and sample number within MTW (8-bit)
  - EVR (seconds and nanoseconds since the epoch)
  - CPU (nanoseconds since the epoch)
- All data coming from FPGA is timestamped using the FPGA internal timestamp.
- At every 14 Hz trigger, EVR provides the EVR timestamp and the CPU timestamp of the trigger. The trigger is also timestamped by FPGA and read on CPU using the set of registers and an interrupt. Thus, at every trigger we have:
  - EVR timestamp and CPU timestamp from EVR
  - FPGA timestamp and CPU timestamp from FPGA
- In this way the EVR and FPGA timestamp of the trigger can be matched
- The trigger timestamps and data are interleaved in the output data stream and used to interpolate the EVR timestamps of data.
- The FPGA internal timestamp wraps around in ca. 4000 seconds. To ensure unambigous timestamp mapping, we cannot keep data in IOxOS buffers for longer than half an hour.

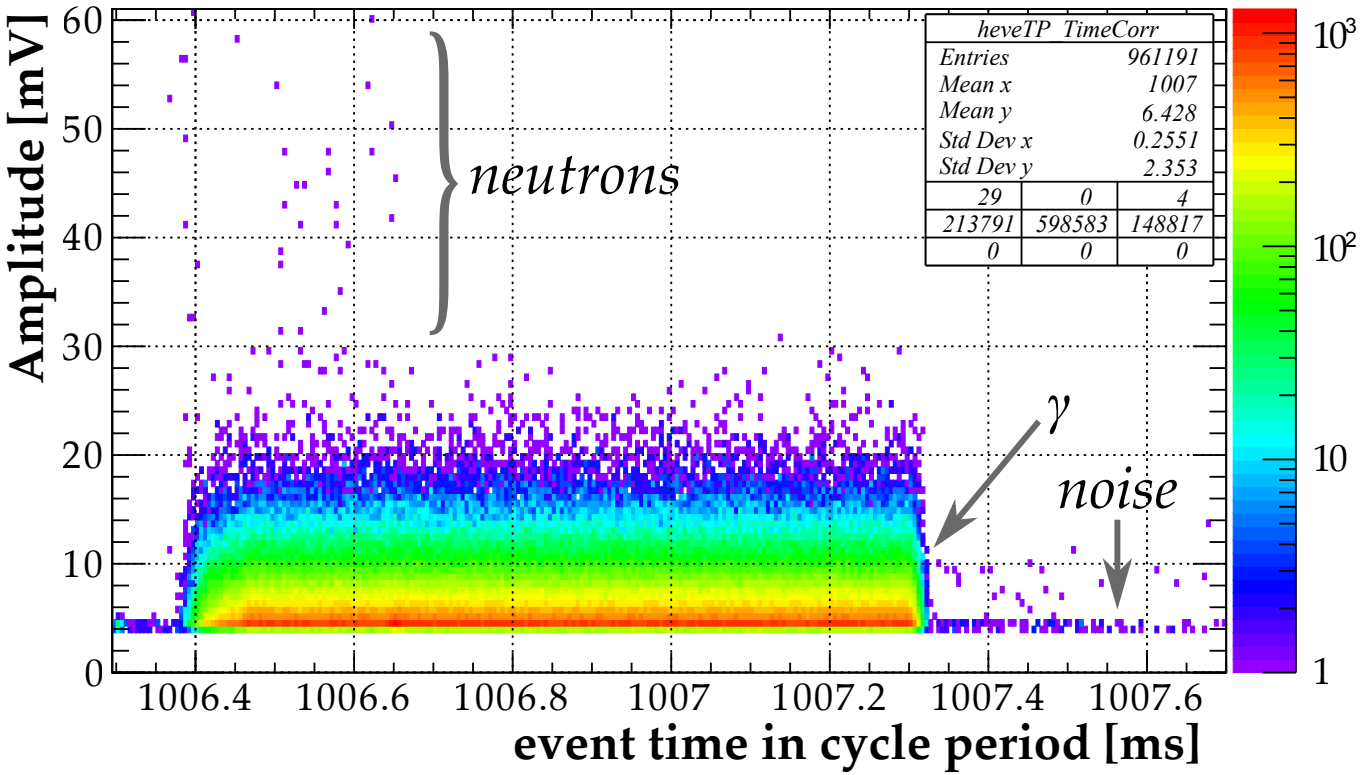
nBLM tests at Linac 4

- In December 2018, a nBLM-F pre-series detector module was installed at LINAC4 at CERN, in the section where conditions close to the ones expected in the ESS DTL can be expected.
- The module was placed close to the beam pipe at the inter-tank region between DTL1 and DTL2 tank, where H^- beam energy reaches ~12 MeV.



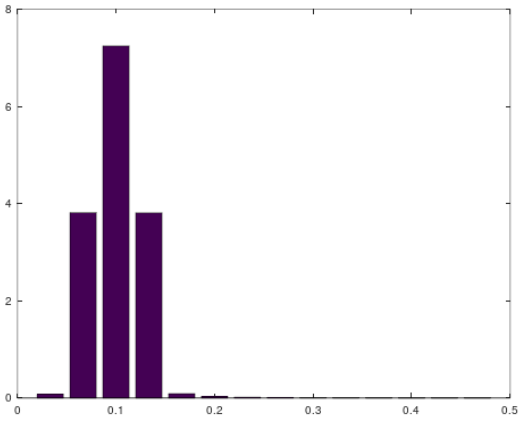
nBLM tests at Linac 4

- There were some problems with interpretation of the data, as the system did not support external timestamp source.
- The exact ADC clock rate has been estimated based on the optimization of the steepnes of the falling edge of the event count distribution.

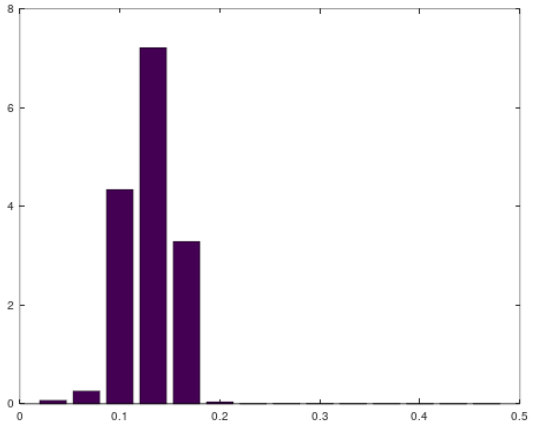


ICBLM implementation status

- ICBLM is much less demanding (in terms of data rates and clock frequencies) than nBLM
- So far, the most complex block is HV 0.1 Hz modulation detection
- Two proposals:
  - Do a Fast Fourier Transform of the input signal and have the magnitude of several frequencies
  - Apply Goertzel algorithm to verify a presence of a specific frequency
- We have decided to implement FFT so the operator sees more information on the panel.



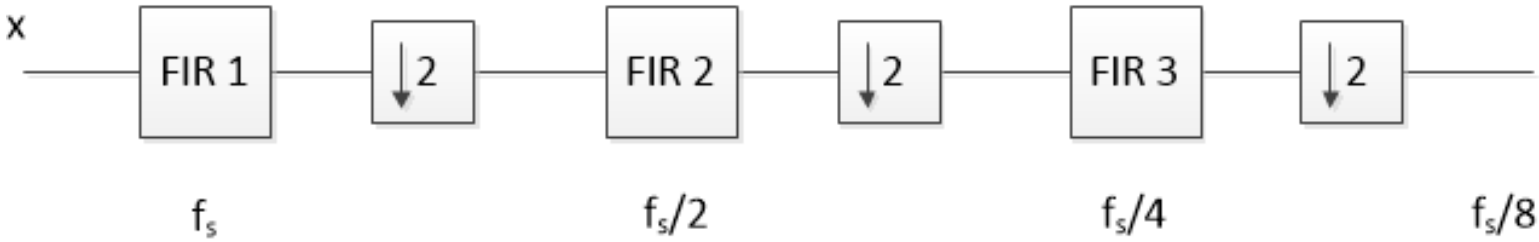
0.1 Hz



0.13 Hz

Decimation

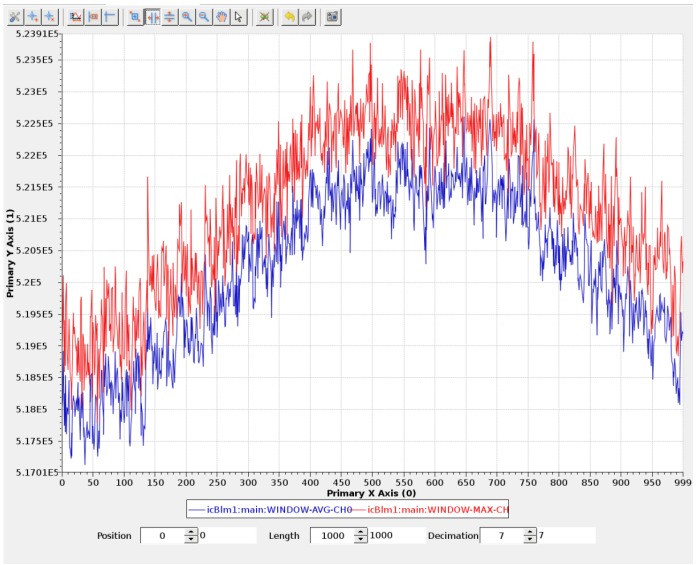
- Reduce the sampling rate to ca. 1 Hz before further processing.
- First filter out higher frequencies
- Then take every n-th sample
- For the bandwidth 0.4 Hz at 1 Ms/s sampling the FIR antialiasing filter would need a few millions coefficients
- At decimation factor $>$ 10 multistage decimation is more efficient.



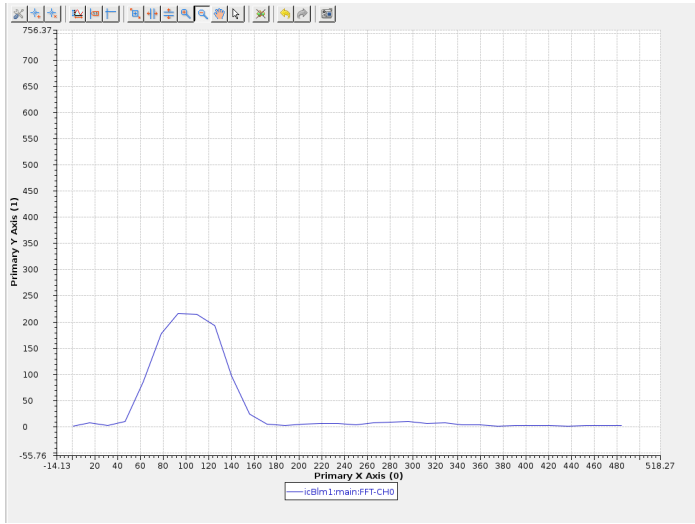
Mutistage decimator

ICBLM EPICS panels

- The results of FFT are transmitted in the periodic data channel.
- One can choose among rectangular, Hamming, Hann, Bartlett, Flattop windows.
- The DC level has been removed by subtracting the average of data in window from each sample.
- Below the results for 1% modulation, with 10 decimation stages, flattop window.



Raw data (100 Hz)



FFT

Problems

- The accelerator timing is not yet defined
  - Background correction specifications in case of ICBLM cannot be finalised - no information about empty pulses
  - Trigger sequence per cycle not precisely defined
  - No examples or guidelines of how to work with beam data, synchronisation, timestamping
- Problems with standalone operation of EVR - timestamps abruptly jumping at every full second
  - Not clear how to set up a test in realistic environment with external cycle trigger (planned test at Linac 4 in November 2019)
- No power supply with HV modulation yet
- No MPS interface board available
- Various problems with IOxOS boards and TOSCA framework
  - Limited memory and DMA bandwidth
  - Numerous problems with kernel driver (Tosca vs Tsc vs ESS Tsc, interrupt support, scatter-gather DMA)
  - TOSCA constantly changing, but without apparent improvement
  - Problems with timing closure
  - Problems with memory calibration at 275 MHz
  - Interrupts coming before the end of the DMA transfer
  - Random CRC errors (might be also caused by software bugs)

Conclusion

- nBLM as advanced, as specification is complete and hardware is ready.
- ICBLM at the early stage of development and not yet blocked by external factors.