



*“Above the
Threshold”*



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Introduction to the Session and Overview of the Front End Integration

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Detector Group Leader

On Behalf of ESS Detector Group and Collaborators

IKON'18

European Spallation Source ERIC

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Welcome to the pre-Dinner session





This IKON Session



Detector Background Sensitivity and Electronics: Overview of Front-End I... *Richard Hall-Wilton*

Update on Status of the Readout *Steven Alcock*

Sten Broman, Grand Hotel 15:35 - 15:50

VMM Integration Update *Dorothea Pfeiffer*

Sten Broman, Grand Hotel 15:50 - 16:05

Downstream of the Readout Master *Morten Jagd Christensen*

Detector Backgrounds: Fast Neutron and Gamma Sensitivity of Helium-3 and B... *Francesco Piscitelli*

Detector Backgrounds and Timing Resolution *Alexander Backis*



TG3 for Detectors Document



Document Type Review Report
Document Number ESS-1546427
Date Sep 27, 2019
Revision 1 (1)
State Preliminary
Confidentiality Level Internal
Page 1 (8)

Chess document: ESS-1546427

Detector Systems Review Process for Instrument Projects at TG3

	Name	Role/Title
Owner	Wen Xiong	Detector Group Administrator
Reviewer	Steven Alcock Richard Hall-Wilton Kalliopi Kanaki Francesco Piscitelli Tobias Richter Oliver Kirstein	Detector Group, FPGA Engineer Detector Group Leader Detector Group, Design Section Leader Detector Group, Detector Scientist Data Management Group Leader Head of Instrument Technologies Division
Approver	Gabor Laszlo	Neutron Instruments Lead Engineer

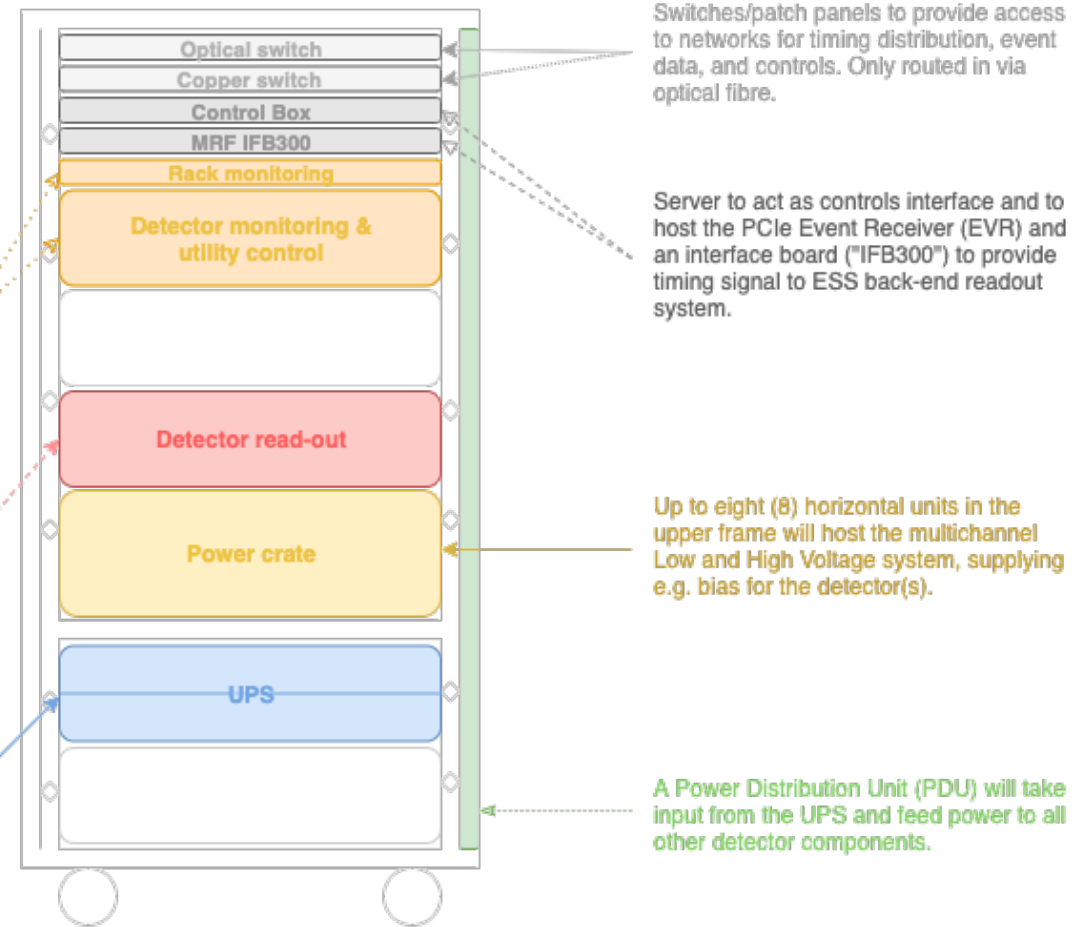
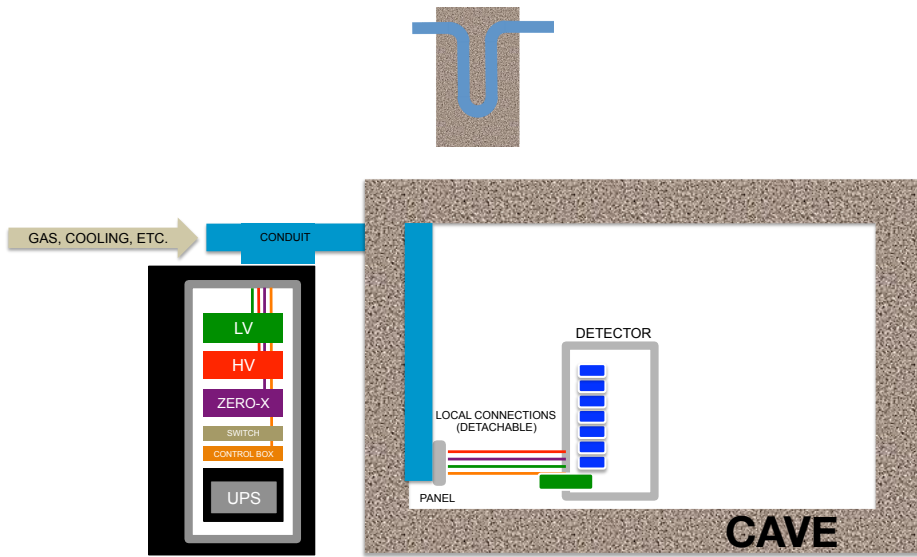
Rack electronics

The standard detector rack is considered part of the readout back-end.

The rack environment will be monitored for e.g. humidity and temperature by use of a commercial-off-the-shelf system. Beckhoff terminals (3U–6U) are used to read and control detector parameters.

The ESS readout back-end provides a common interface for detector front-ends including controls and time distribution.

Six (6) horizontal units of space in the lower frame are reserved for the double-converting Uninterruptable Power Supply (UPS) which will be grounded through the mains input and supply floating ground for all downchain detector electronics.



Power, Grounding and Detector Connection

- Draft layout of detector racks done
- Anders Lindh Olsson left in December
- Work will be completed (document) as soon as replacement identified



Standard Detector Racks

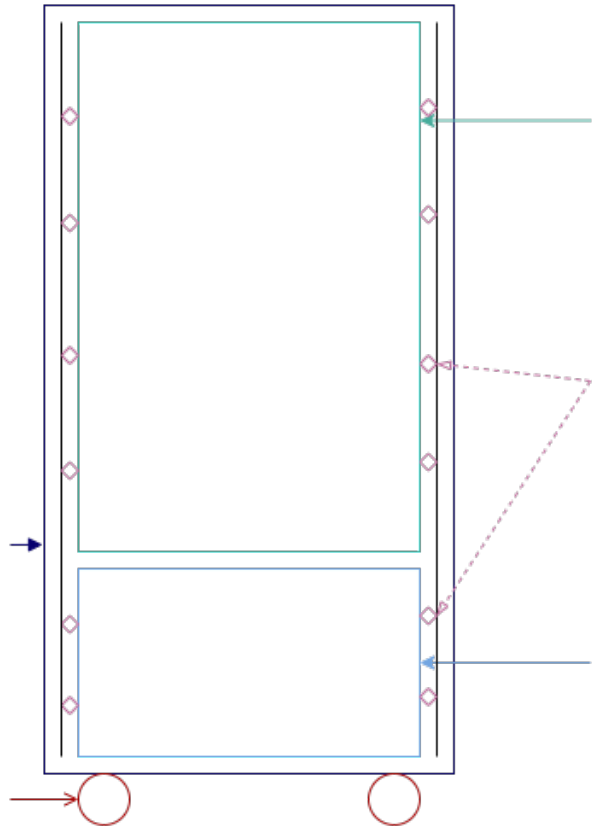
- "Standard detector rack" selected based on STFC In-Kind report

Detector rack

The standard detector rack is an nVent Schroff VARISTAR 'EMC' (i.e. RF-shielded) with separate upper and lower inner frames which are galvanically isolated from the enclosure and thus also each other. The inner frames themselves are conductive.

The enclosure itself is of an EMC enhanced version, has roof-mounted lifting eye-bolts and glazed front and back doors.

The enclosure stands on casters with build-in levelling feet.



The upper frame is an extension of the instrument cave's grounding zone through the Zone Entry Point, ensuring that all detector components are on the same floating ground.

The electrically conductive (AlZn) upright inner frames are separated from the outer frame by ISOBOLTS (isolating mounting bolts).

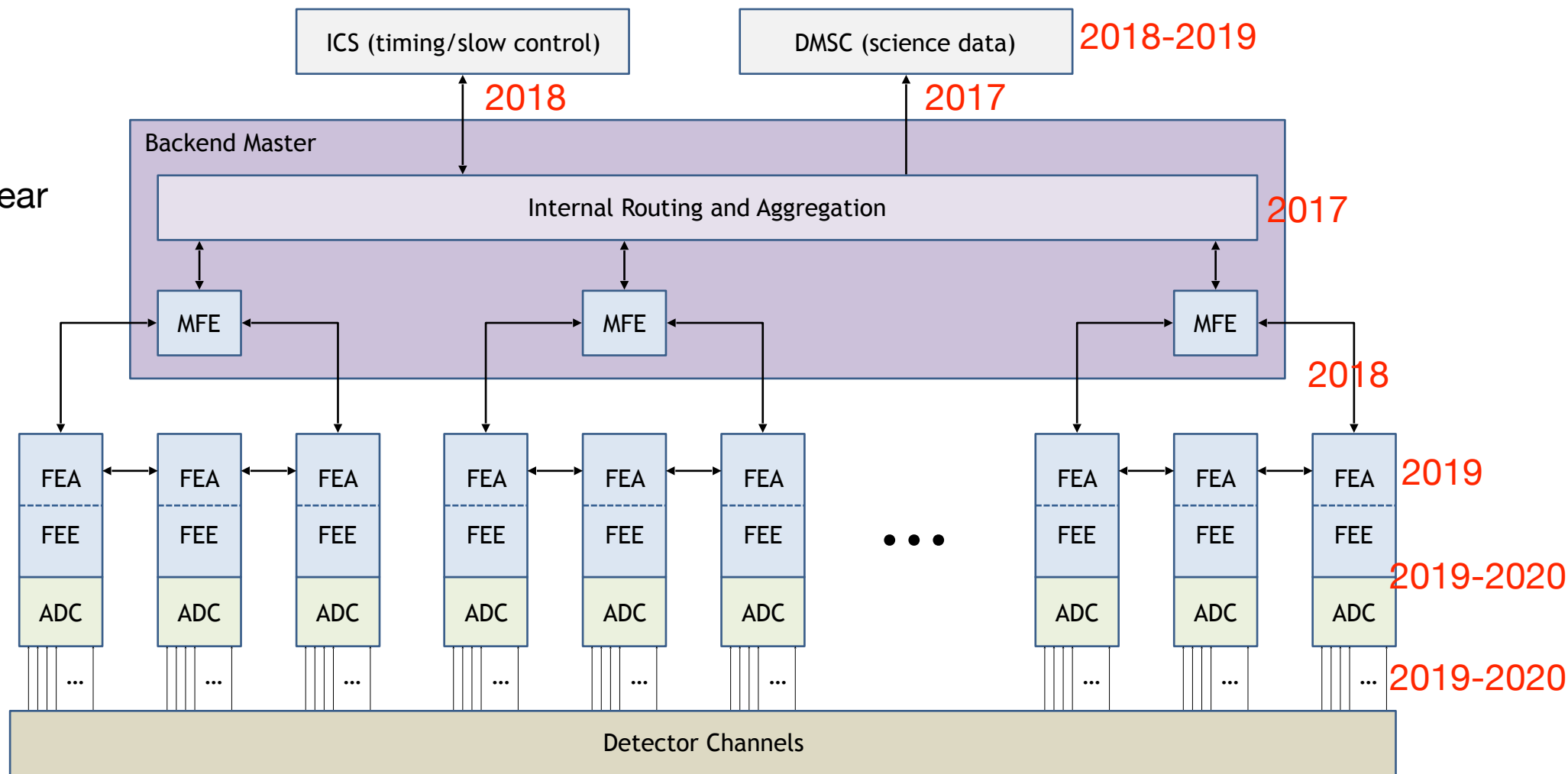
The lower (12U) frame has the same ground as equipment inside of the rack, and is primarily to host the UPS which then provides ground for the rest of the detector electronics (preamplifiers, detector bias, etc.)



Readout Architecture

1st end-end DAQ demonstration this year

2020/2021: moving this into a production system



Detector Electronics Integration Models





Assister Specification Document



Chess document: ESS-2055809



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Document Type	Interface Description
Document Number	ESS-2055809
Date	Feb 14, 2020
Revision	1 (1)
State	Preliminary
Confidentiality Level	Internal
Page	1 (48)

ESS Readout Electronics:

Front End Interface Guidelines Release V1

	Name	Role/Title
Owner	Harry Walton	In-Kind Collaborator, STFC
Reviewer	Scott Kolya	Research Engineer in Detector Electronics
	Steven Alcock	FPGA Firmware Engineer
Approver	Richard Hall-Wilton	Detector Group Leader



FE user interface



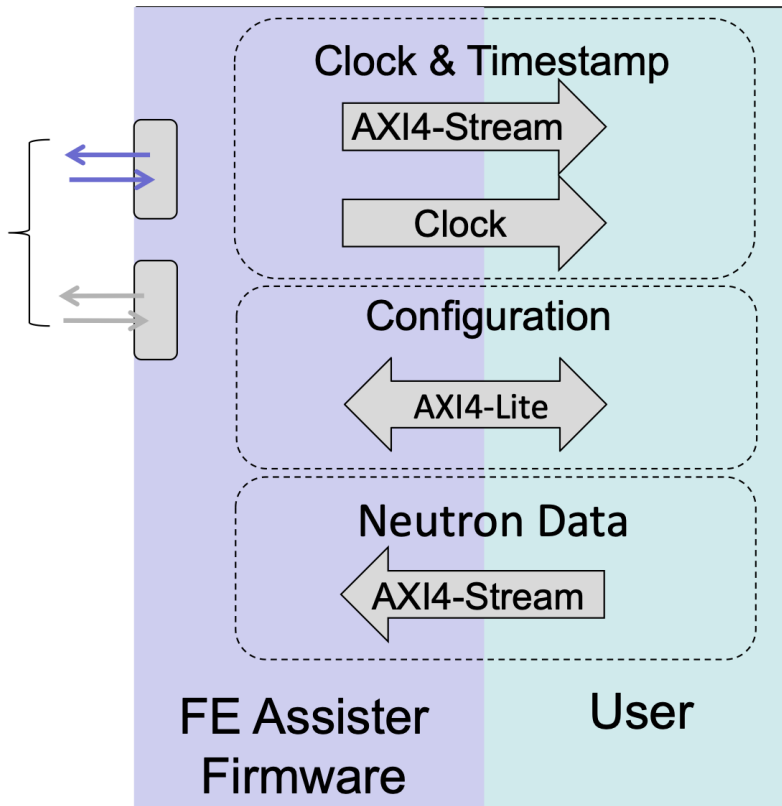
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- FEA (front end assister) firmware communicates with the ring/backend
- FEE (front end user firmware) communicates with frontend ASIC like VMM3a or ADC
- FEA and FEE part of firmware communicate via AXI4 streams



Ring (Backend)

Front End User Interface



For FE integration models see
BrightnESS Deliverable Report: D4.1 – *Integration Plan
for Detector Readout*, Scott Kolva et.al. 2017



Front-End to Back-End Integration Status



Instrument	Front-End	Integration Agreed?	Integration Model	Integration Started?	Estimate for Integration Demonstration
CSPEC	VMM	Yes	A	Yes: Nov19	May 2020
TREX	VMM	Yes	A	Yes: Nov19	May 2020
ESTIA	VMM	Yes	A	Yes: Nov19	May 2020
FREIA	VMM	Yes	A	Yes: Nov19	May 2020
NMX	VMM	Yes	A	Yes: Nov19	May 2020
DREAM	CIPIX	Yes	C	Yes: Oct19	Apr 2020
MAGIC	CIPIX	Yes	C	Yes: Oct19	Apr 2020
HEIMDAL	CIPIX	Yes	C	Yes: Oct19	Apr 2020
LOKI	ISIS PREAMP/CAEN R5560	Yes	C	Yes: Jun19	Mar 2020
BIFROST	ILL PREAMP / CAEN R5560	Yes	C	No: Mar20	Jun 20
VESPA	<i>PREAMP / CAEN R5560 (TBC)</i>	No	C (tbc)	No	tbd
MIRACLES	<i>PREAMP / CAEN R5560 (TBC)</i>	No	C (tbc)	No	tbd
SKADI	IDEAS	Yes	X	Partially: Aug19/Jan20	May 2020
ODIN	Custom Camera+EPICS & TIMEPIX 3	Partially	XX & C (tbc)	No	tbd
BEER	Delay Line + Custom FPGA	No	C (tbc)	No	tbd
Beam Monitors	PREAMP / PINK BOX	Yes	B	Yes	Complete
TestBeam Line	Custom	No	tbd.	No	No



After Integration Demonstration?



- Full DAQ chain needs to be challenged with data to iron out features ...
- ... and to understand data , geometry and how to commission ...
- ESS Detectors systems are complicated compared to most existing neutron detectors

- Full system needs to be documented



Enjoy the Session