LLRF for ESS – Modelling and Control

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What is Control?

Accelerator Controls: Providing computer environment that allows remote access to accelerator hardware // ... [3]



<u>Automatic Control</u>: Modelling and controller design for dynamic systems to obtain desired performance.





What this talk will be about





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<u>Overview</u>

- RF System Modelling
- Analysis from a control perspective
 - Prediction of achievable cavity field stability
 - What factors limit/affect achievable performance



Cavity Model [2]

$$\frac{d}{dt} \begin{bmatrix} V_{\text{Re}} \\ V_{\text{Im}} \end{bmatrix} = \begin{bmatrix} -\omega_{1/2} & -\Delta\omega \\ \Delta\omega & -\omega_{1/2} \end{bmatrix} \begin{bmatrix} V_{\text{Re}} \\ V_{\text{Im}} \end{bmatrix} + \begin{bmatrix} R_L \omega_{1/2} & 0 \\ 0 & R_L \omega_{1/2} \end{bmatrix} \begin{bmatrix} I_{\text{Re}} \\ I_{\text{Im}} \end{bmatrix}$$

- V cavity voltage
- $\bullet~\mathbf{I}=2\mathbf{I_g}+\mathbf{I_b}$ = klystron current + beam current
- $\omega_{1/2}$ cavity bandwidth
- $\Delta \omega$ detuning of the cavity



Klystron & Modulator Model

Klystron dynamics are modelled by 1st order low-pass filter with 1.9 MHz bandwidth.



Each % of modulator voltage variation induces $>10^{\circ}$ phase shift and 1.25% amplitude change in the klystron output [1].





RF Distribution & Cables



Time delays:

40 m / 0.68c = 175 ns 40 m / 0.82c = 145 ns 10 m / 0.82c = 40 ns



Control algorithm execute @ 100 MHz on FPGA

Analog/Digital Converter Noise: 60 dB SNR

Downsampling (improves SNR 10 dB) modelled as 1st order filter with 5 MHz bandwidth

Time-delays	
ADC latency	130 ns
25 FPGA cycles	250 ns
DAC delay	90 ns
Total	490 ns

LLRF





Putting things together





Putting things together





Putting things together







Analysis from a control perspective



Control Methodology

Flat-top operation is considered. Disturbances are either repetitive or random.





Repetitive disturbance -> Iterative Learning Control



Random disturbance -> Feedback



Disturbance Rejection using Feedback





Disturbance Rejection using Feedback



Bode's Integral Theorem,

$$\int_0^\infty \ln \frac{1}{1 + P(i\omega)C(i\omega)} \mathrm{d}\omega = 0$$

puts fundamental limitation on achievable control performance.



Disturbance Rejection using Feedback



Loop delay has large impact on achievable performance!



Frequency Specific Disturbance Rejection



Increased controller gain at a specific frequency gives improved narrow-band disturbance rejection. Small degradation for other frequencies.



Feed-Forward of Beam Current Ripple (1/2)





Accessing the measurement signal from the Beam Current Monitors seems feasible.



Feed-Forward of Beam Current Ripple (2/2)



Potential performance gain from using feed-forward from beam current monitor.

 $Assumptions: BCM \ BW = 1 \ MHz, \ good \ SNR \ for \ the \ BCM. \ Ion \ Source \ BW = 0.65 \ MHz, \ Cavity \ BW = 12 \ kHz, \ Loop-delay \ 1us \ NHz \ Loop-delay \ Sumptions \ Summatrix \ Summatr$



- There are limitations to what can be achieved by control.
- Time delays, beam current ripple and klystron ripple are the main performance limitations.
- Good disturbance rejection for
 - Low frequencies (< 1 kHz)
 - High frequencies (> 1 MHz)
 - Narrow-band disturbances (with modified controller)
- Two methods for improved disturbance suppression were presented.



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[2] Thomas Schilcher.

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[3] Elke Zimoch.

Accelerator controls.

Joint Universities Accelerator School, 2015.

