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Master Module CDR

10th February 2023
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- Overview of the Detector Readout Master Module (DRMM) Functionality and Purpose.
- FPGA Architecture, Resource usage and I/O.
- Product development.
- Readout Master Module Requirements Document.
- Summary of Local Soak and Thermal Stress Testing.

Before we start...

Term	Definition
ADC	Analog-to-Digital Converter
ASIC	Application Specific Integrated Circuit
DMSC	Data Management and Software Centre
EFU	Event Formation Unit
EPICS	Experimental Physics and Industrial Control System
EVR	Event Receiver
FEBEAC	Front End Back End Assister Card
FEN	Front End Node
FEE	Front End Electronics
FPGA	Field Programmable Gate Array
MFE	Master Front End

The Role of Detector Group Readout

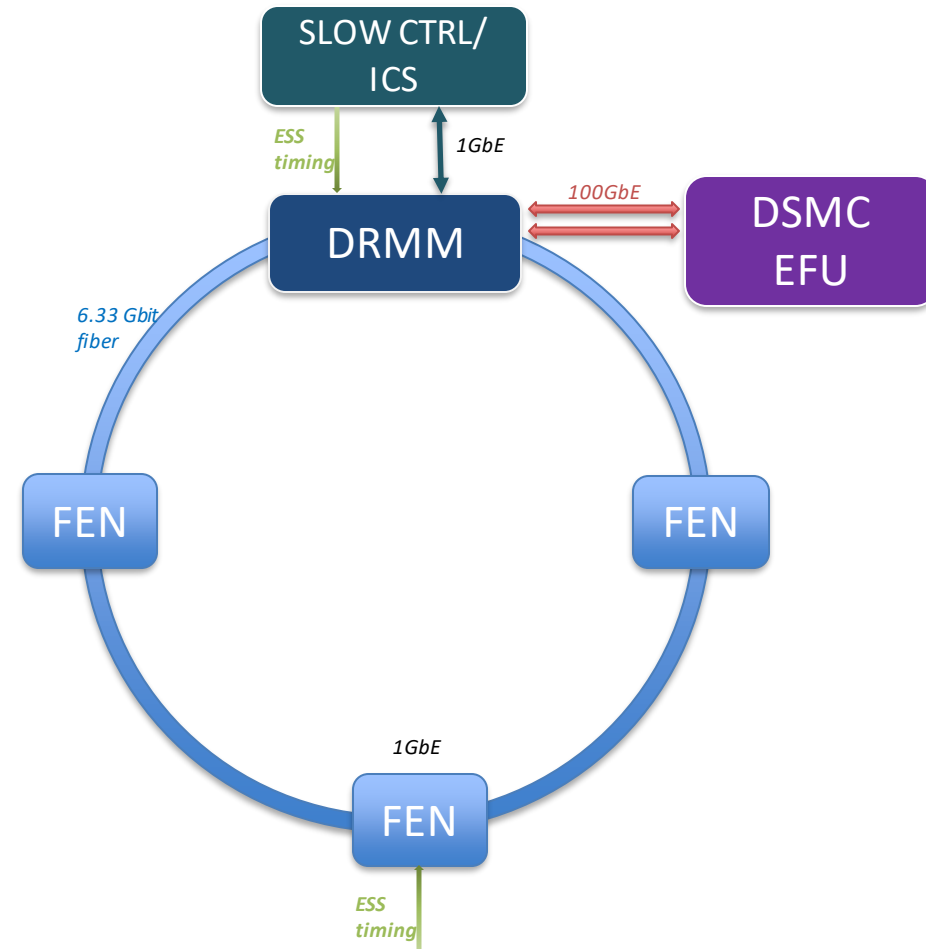
- Ensure that the DAQ chain is commissionable, operable and maintainable with minimal resource requirements for the lifetime of the instrument.
- How?
 - Support instruments in the choice and development of readout front ends (digitisers and associated logic).
 - Provision a generic framework for science data, slow control and timing for these front ends.
 - Manage and facilitate the integration of these front ends into this generic readout framework.



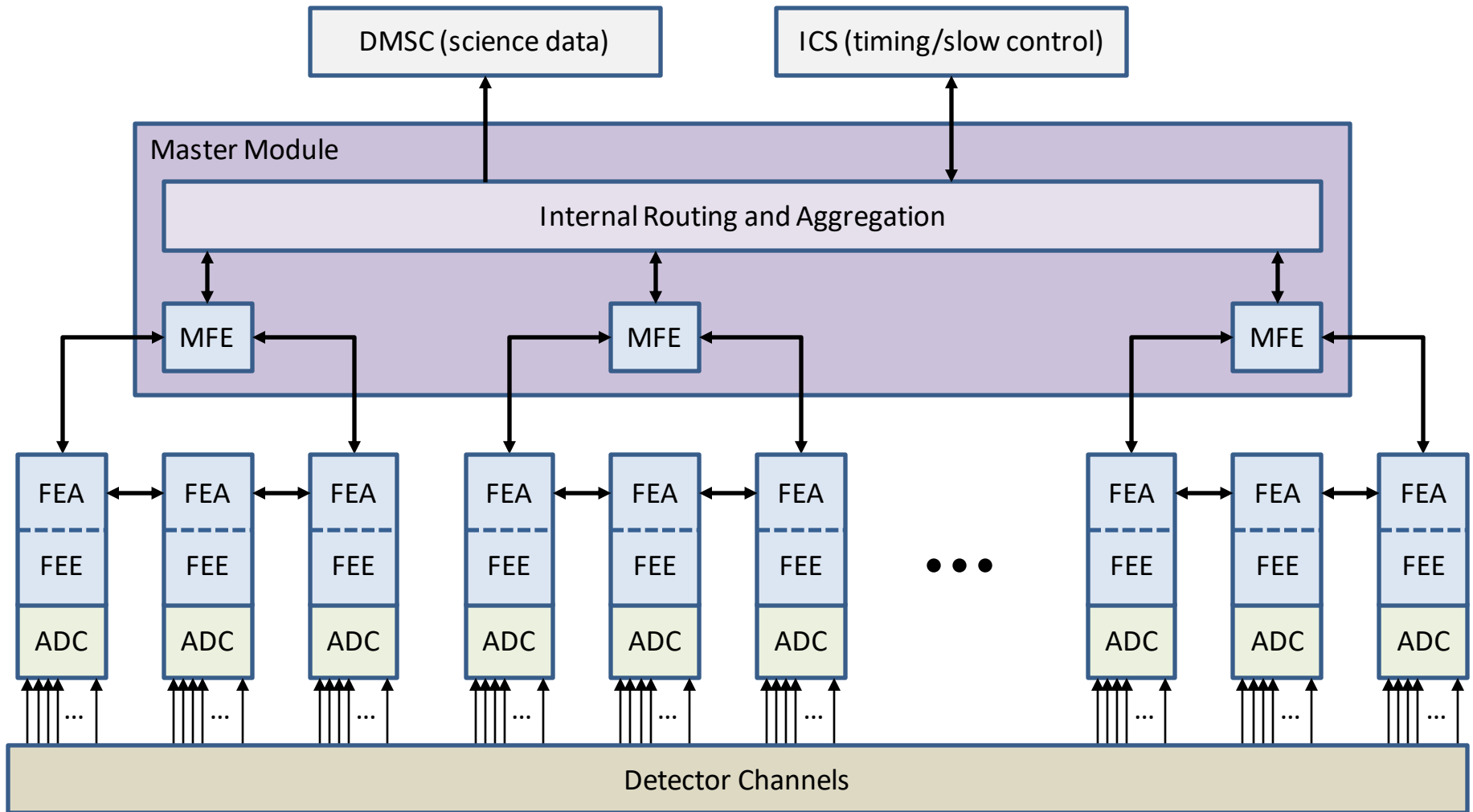
Detector Readout Master Module (DRMM) – Requirements - ESS-4184238

APPLICABILITY:

- Acquire data from the "Front End Nodes" (FENs) which interface to the front-end FPGA/ADC/detector chain.
- The connectivity between the Readout Master and the FENs is achieved through 8B/10B encoded MGT-driven (Multi-Gigabit Transceiver) optical fibres links arranged in a ring topology.
- For the slow control interface, the Readout Master instantiates a lightweight UDP stack which communicates with the EPICS IOC (Input Output Controller) using a standard Gigabit Ethernet link.
- The master module shall support an output bandwidth of 200Gb/s utilizing 2 100Gb/s Ethernet links to the EFU.



ESS Readout Architecture



Detector Readout Master Module (DRMM) – Requirements - ESS-4184238



Main requirements:

Logical:

- Data acquisition system common across all ESS instruments.
- Integrate ICS timing, ICS EPICS slow control and Data Egress downstream to DMSC.
- Output bandwidth 2x100Gb/s.
- Data rings to front-end: 12 bidirectional rings (24 fibers).
- Ring connection done through daughter boards interfacing with fibre via SFP connectors.

Form factor:

- Based around VCU118 FPGA (UltraScale+ Architecture) hardware from Xilinx.
- Fits in standard 19" rack.
- Standard Shuko power socket.
- Body of master module forms a self-contained crate, with good EMC protection.

Common Detector Readout



- The readout data is sent over Ethernet as UDP payload which can be as long as 8972 bytes long.
- Maximum transmission unit (MTU) for Ethernet of 9000 bytes.
- The connectivity between the Readout Master and the FENs is achieved through 8B/10B encoded MGT-driven (Multi-Gigabit Transceiver) optical fibres links arranged in a ring topology.
- For the slow control interface, the Readout Master instantiates a lightweight UDP stack which communicates with the EPICS IOC (Input Output Controller) using a standard Gigabit Ethernet link.
- The master module shall support an output bandwidth of 200Gb/s utilizing 2x100Gb/s Ethernet links to the EFU.

FPGA Architecture

- Virtex™ UltraScale+™ is a high performance FPGA, using TSMC's 16nm FinFET+ process (16FF+).
- >600 MHz operation.
- Several I/O and transceivers.
- "As the industry's most capable FPGA family, the devices are ideal for compute-intensive applications ranging from 1+Tb/s networking and machine learning."
- XCVU9P

Device Name	VU9P
System Logic Cells (K)	2,586
CLB Flip-Flops (K)	2,364
CLB LUTs (K)	1,182
Max. Dist. RAM (Mb)	36.1
Total Block RAM (Mb)	75.9
UltraRAM (Mb)	270.0
DSP Slices	6,840
Peak INT8 DSP (TOP/s)	21.3
PCIe® Gen3 x16	6
PCIe Gen3 x16/Gen4 x8 / CCIX ⁽¹⁾	–
150G Interlaken	9
100G Ethernet w/ KR4 RS-FEC	9
Max. Single-Ended HP I/Os	832
Max. Single-Ended HD I/Os	0
GTY 32.75Gb/s Transceivers	120
GTM 58Gb/s PAM4 Transceivers	–
100G / 50G KP4 FEC	–
Extended ⁽²⁾	-1 -2 -2L -3
Industrial	-1 -2

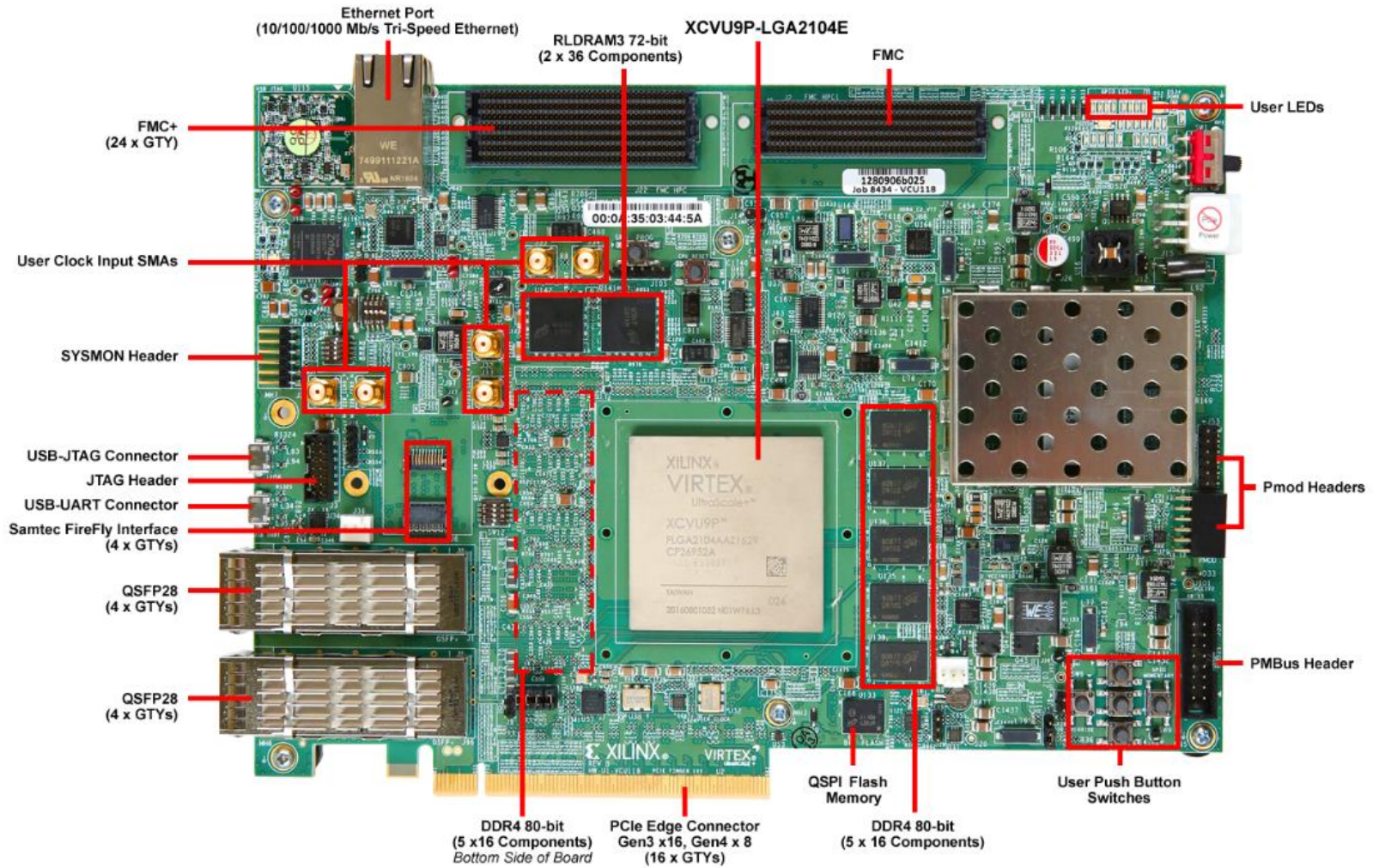


FPGA Resource Usage

Resource	Utilisation	Maximum	%
LUT	79230	1182240	6.70
LUTRAM	5167	591840	0.87
FF	190018	2364480	8.04
BRAM	221	2160	10.23
DSP	6	6840	0.09
IO	59	832	7.09
GT	29	52	55.77
BUFG	88	1800	4.89
MMCM	3	30	10.00
PLL	2	60	3.33

Resource utilisation of Backend Master commit 9b15d30a9e944badb7118e8e1d9754fbb6127068 [6]

VCU118 Master IO



Product Development: 100 G Detector Readout Demonstrator.



100 G Data Generator

Second Joint BrightnESS WP4 and WP5

Jamboree

15th September 2017

Steven Alcock (DG)

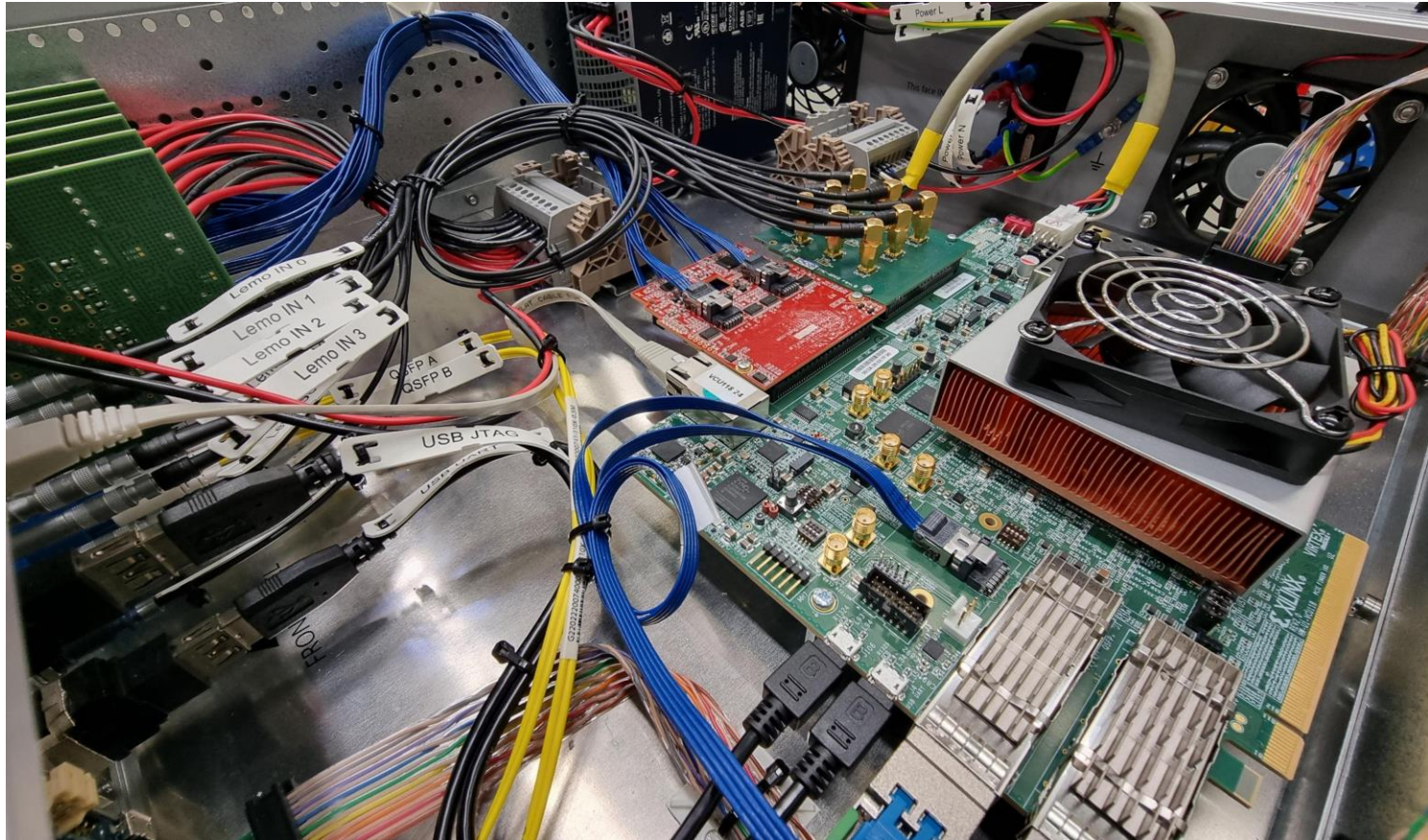
First Design



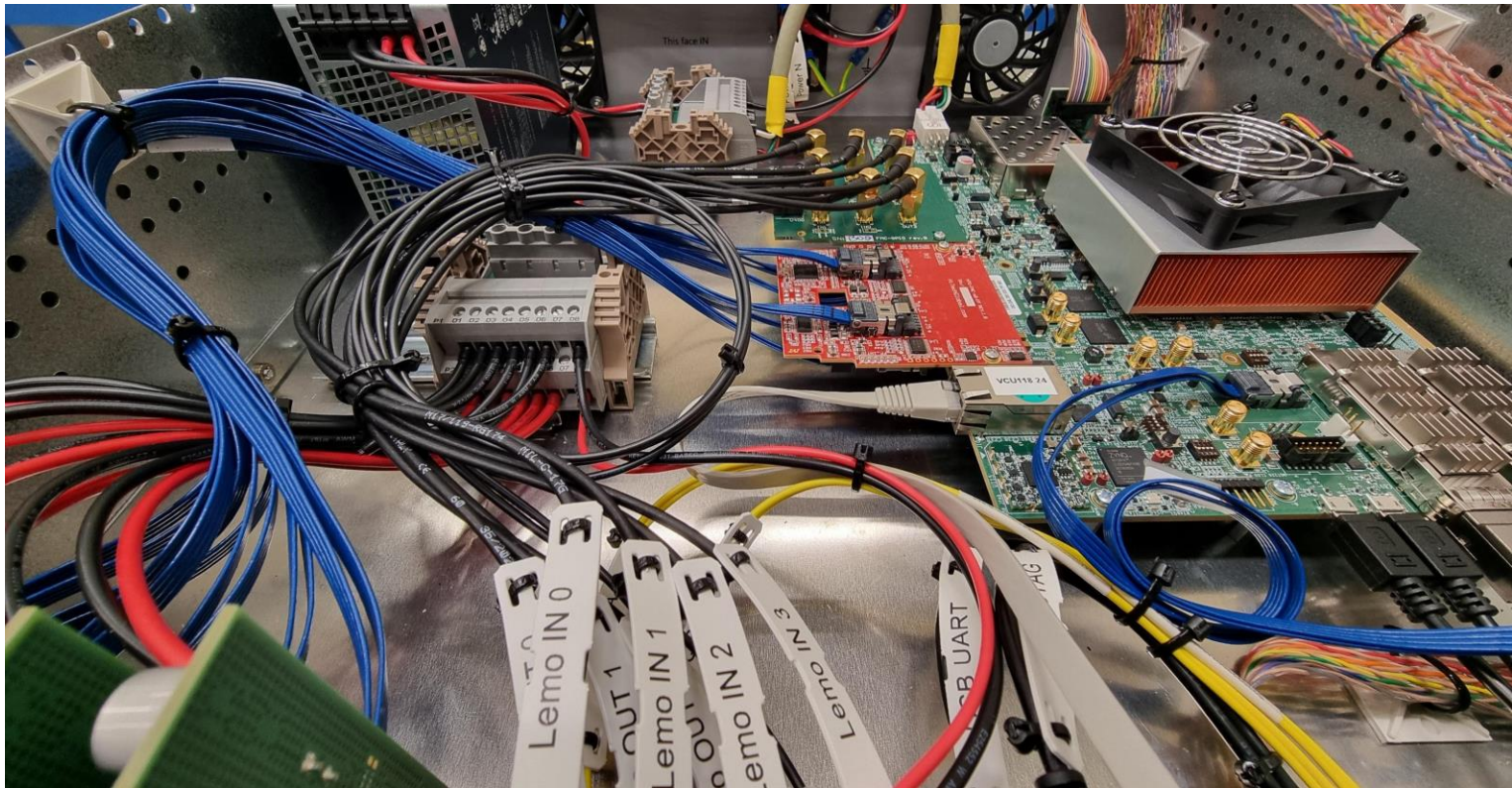
Final Design



Inside the DRMM crate – Front right corner view

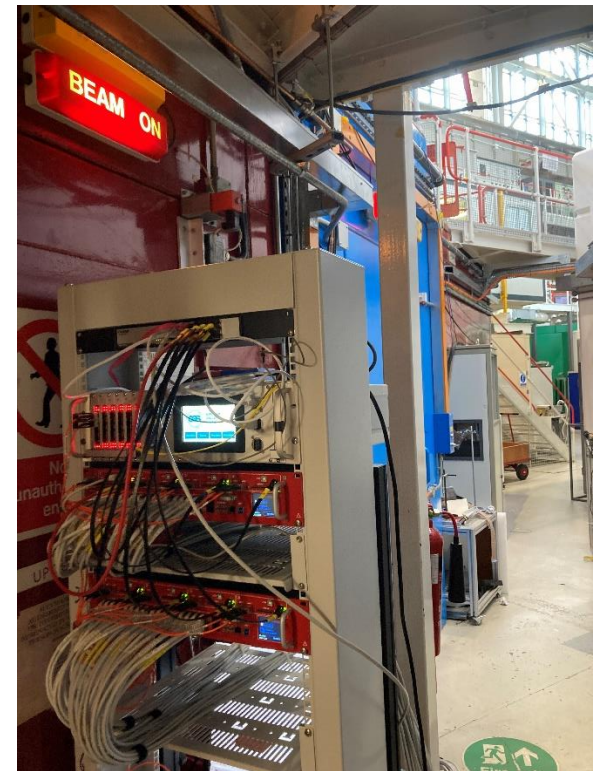
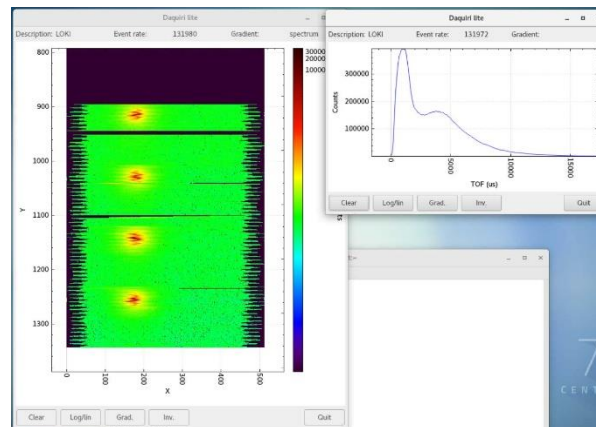


Inside the DRMM crate –Back view



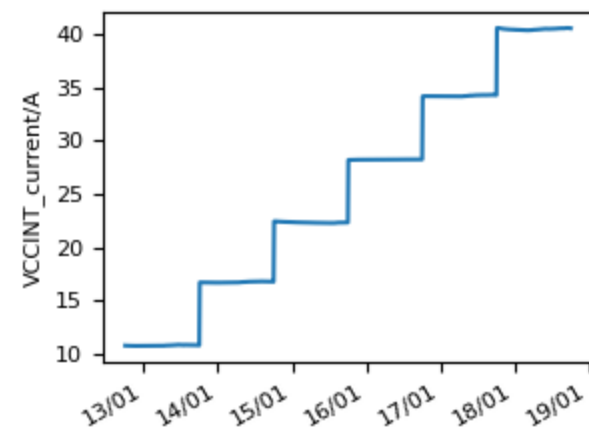
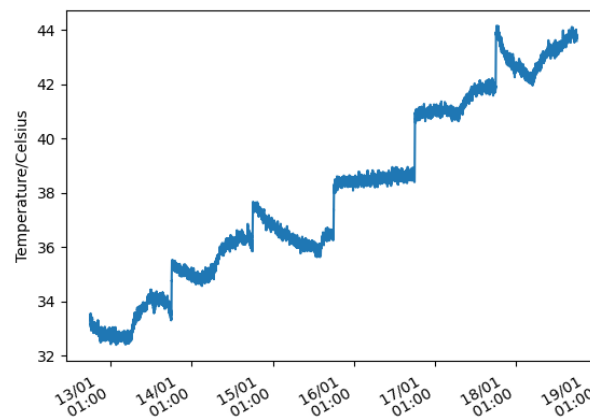
Deployments: LOKI Beamtime (April 2021)

- Successful beamtime at ISIS was the first true end-to-end test of the full DAQ chain (detector through to **DMSC**).
- Provides confidence that the ESS Readout System can be used for configuration, time distribution, and data readout of a real Instrument.



Local Soak Tests (January 2022)

- Custom test firmware deployed to ensure the Master Module could sustain high electrical loads over long periods of time.
- Configured the FPGA to draw increasingly large currents (far in excess of what is voltage, current and temperature measurements from the relevant on-board power regulators at 5 second intervals.
- Results showed system can operate comfortably at expected loads: full report is available.



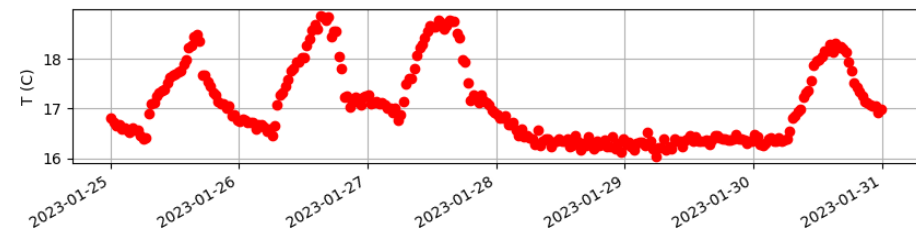
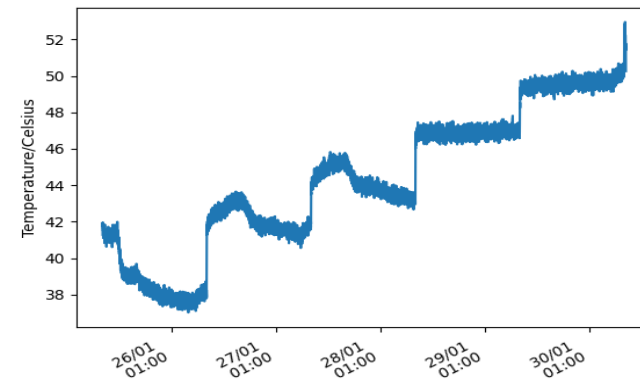
Local Soak Tests – Updated chassis (February 2023)



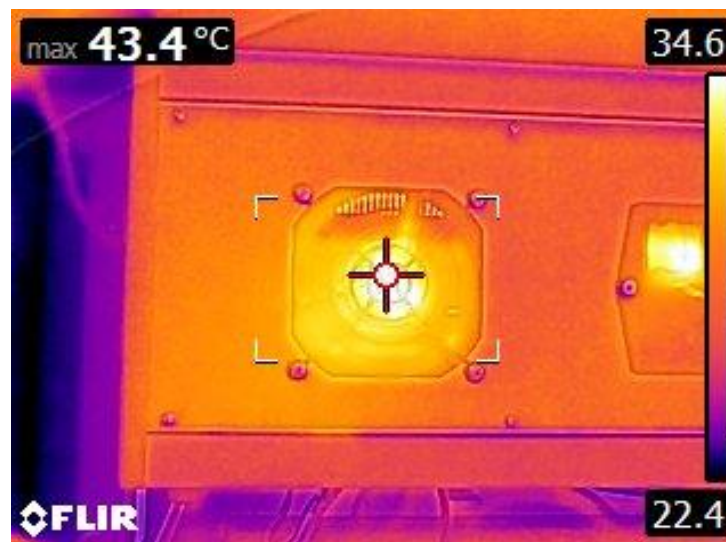
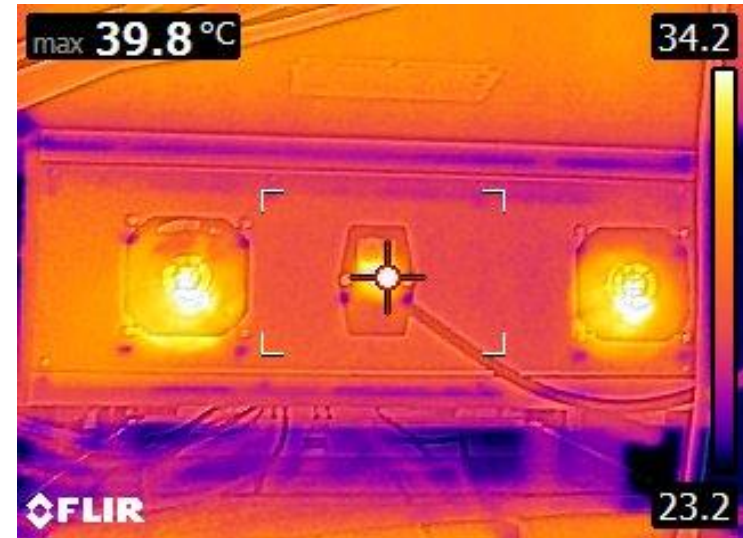
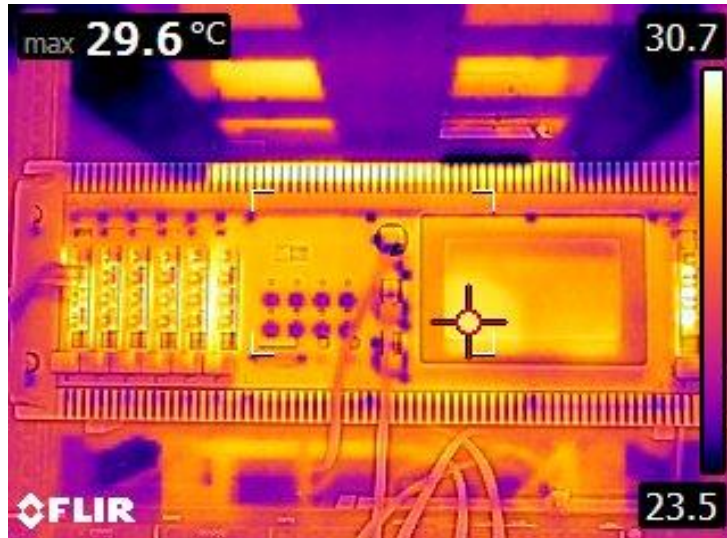
New tests were made with updated 3U/4U Verotech Caseframe chassis featuring airflow vents integrated into the top and bottom covers.

Local Soak Tests – Updated chassis (February 2023)

- A five-day soak test similar to the prototype Master Module testing was conducted, using a closed rack with no fans installed.
- Of the 8 fans slots in the top of the rack, one was open for cables, and the other 7 were closed off. To provide additional thermal load in the rack, there was also a server and an R5560 ADC crate installed in the rack.

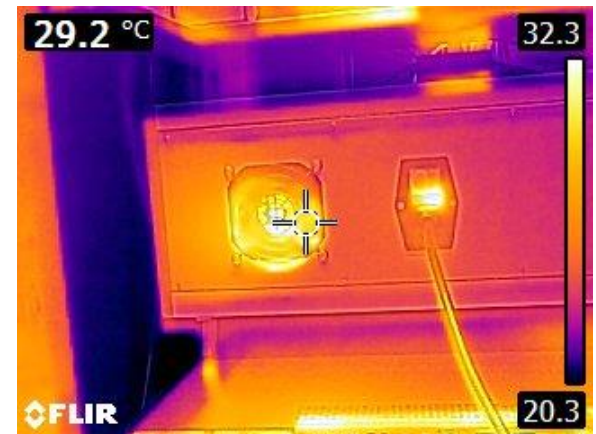
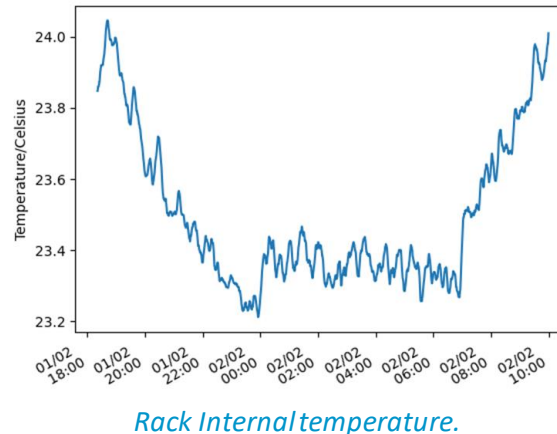
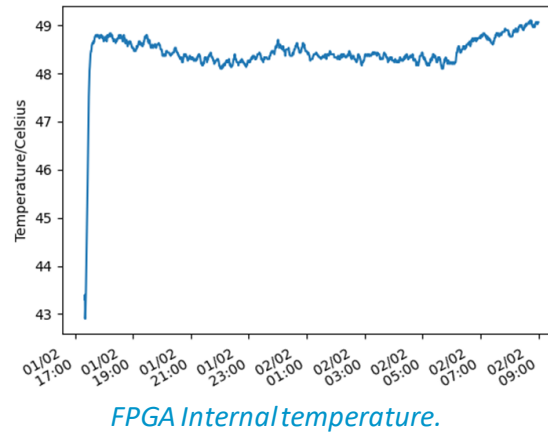


Soak test - Thermal Camera photos



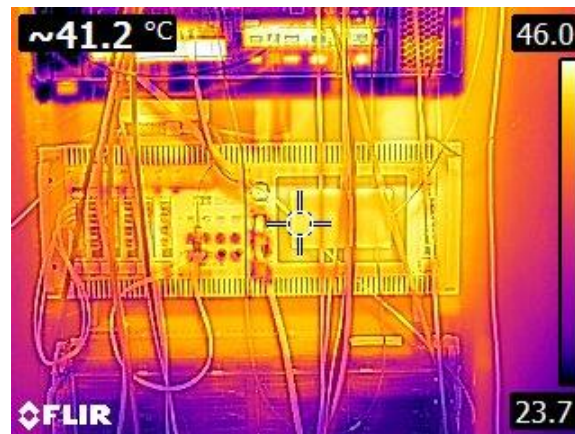
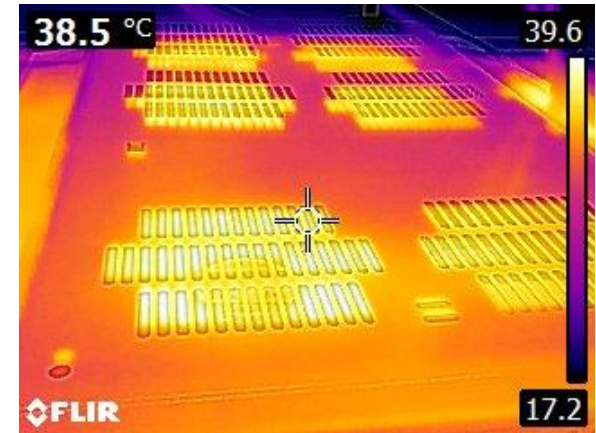
Thermal stress – Ventilated Rack

RMM under test in a ventilated rack (stress test in a normal usage environment).



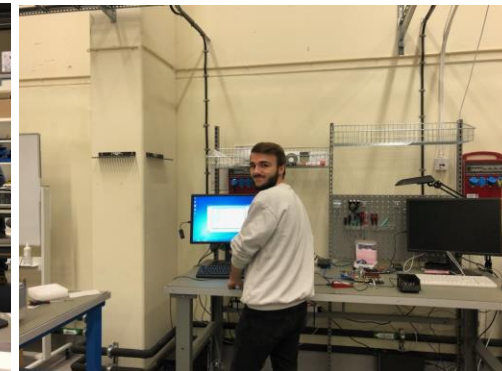
Thermal stress – Hot Rack

The ambient temperature was set to 40°C to simulate a rack fan ventilation failure.



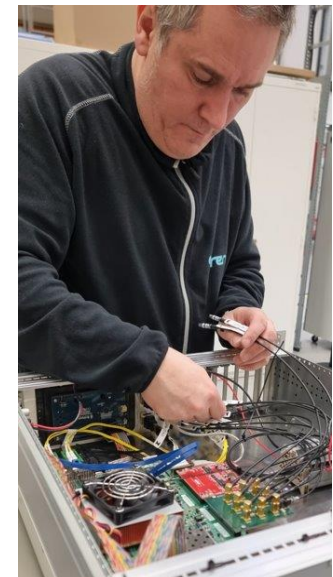
Readout Master Module Functionality Testing

- VCU118 test
 - Check that the VCU118 is functional before RMM assembly
- RMM functional test
 - Check that assembly has been performed correctly



project_1 - [/home/sgroup/project_vj/project_1/npj] - Vivado Lab Edition

Name	Tx	Rx	Status	Bits	Err.	BER	BERT Reset	TX Pattern
▼ % FEBEAC 1 (4)								
Lnk 4	Quads_126MGT_X0Y26TX Incutp_01	Quads_126MGT_X0Y26RX Incutp_01	6.340 Gbps	1.139E12	0E0	8.809E-33	Reset	PRBS 7-tbit
Lnk 5	Quads_126MGT_X0Y30TX Incutp_01	Quads_126MGT_X0Y30RX Incutp_01	6.340 Gbps	1.141E12	0E0	8.764E-33	Reset	PRBS 7-tbit
Lnk 6	Quads_126MGT_X0Y34TX Incutp_01	Quads_126MGT_X0Y34RX Incutp_01	6.340 Gbps	1.141E12	0E0	8.764E-33	Reset	PRBS 7-tbit
Lnk 7	Quads_126MGT_X0Y38TX Incutp_01	Quads_126MGT_X0Y38RX Incutp_01	6.340 Gbps	1.141E12	0E0	8.764E-33	Reset	PRBS 7-tbit
▼ % FEBEAC 2 (7)								
Lnk 8	Quads_122MGT_X0Y12TX Incutp_01	Quads_122MGT_X0Y12RX Incutp_01	6.339 Gbps	1.139E12	0E0	8.827E-33	Reset	PRBS 7-tbit
Lnk 9	Quads_122MGT_X0Y16TX Incutp_01	Quads_122MGT_X0Y16RX Incutp_01	6.340 Gbps	1.139E12	0E0	8.827E-33	Reset	PRBS 7-tbit
Lnk 10	Quads_122MGT_X0Y20TX Incutp_01	Quads_122MGT_X0Y20RX Incutp_01	6.340 Gbps	1.139E12	0E0	8.827E-33	Reset	PRBS 7-tbit
Lnk 11	Quads_122MGT_X0Y24TX Incutp_01	Quads_122MGT_X0Y24RX Incutp_01	6.340 Gbps	1.139E12	0E0	8.827E-33	Reset	PRBS 7-tbit
▼ % FEBEAC 3 (4)								
Lnk 12	Quads_125MGT_X0Y26TX Incutp_01	Quads_125MGT_X0Y26RX Incutp_01	6.335 Gbps	1.127E12	0E0	8.871E-33	Reset	PRBS 7-tbit
Lnk 13	Quads_125MGT_X0Y30TX Incutp_01	Quads_125MGT_X0Y30RX Incutp_01	6.340 Gbps	1.127E12	0E0	8.871E-33	Reset	PRBS 7-tbit
Lnk 14	Quads_125MGT_X0Y34TX Incutp_01	Quads_125MGT_X0Y34RX Incutp_01	6.340 Gbps	1.127E12	0E0	8.871E-33	Reset	PRBS 7-tbit
Lnk 15	Quads_125MGT_X0Y38TX Incutp_01	Quads_125MGT_X0Y38RX Incutp_01	6.340 Gbps	1.127E12	0E0	8.871E-33	Reset	PRBS 7-tbit
▼ % FEBEAC 5 (4)								
Lnk 20	Quads_120MGT_X0Y4TX Incutp_01	Quads_120MGT_X0Y4RX Incutp_01	6.340 Gbps	1.126E12	0E0	8.936E-33	Reset	PRBS 7-tbit
Lnk 21	Quads_120MGT_X0Y8TX Incutp_01	Quads_120MGT_X0Y8RX Incutp_01	6.340 Gbps	1.126E12	0E0	8.929E-33	Reset	PRBS 7-tbit
Lnk 22	Quads_120MGT_X0Y12TX Incutp_01	Quads_120MGT_X0Y12RX Incutp_01	6.340 Gbps	1.126E12	0E0	8.929E-33	Reset	PRBS 7-tbit
Lnk 23	Quads_120MGT_X0Y16TX Incutp_01	Quads_120MGT_X0Y16RX Incutp_01	6.340 Gbps	1.126E12	0E0	8.929E-33	Reset	PRBS 7-tbit
▼ % FEBEAC 6 (4)								
Lnk 24	Quads_233MGT_X1Y58TX Incutp_01	Quads_233MGT_X1Y58RX Incutp_01	1.761 Gbps	3.092E11	0E0	3.234E-32	Reset	PRBS 7-tbit
Lnk 25	Quads_233MGT_X1Y57TX Incutp_01	Quads_233MGT_X1Y57RX Incutp_01	1.761 Gbps	3.092E11	0E0	3.234E-32	Reset	PRBS 7-tbit
Lnk 26	Quads_233MGT_X1Y56TX Incutp_01	Quads_233MGT_X1Y56RX Incutp_01	1.761 Gbps	3.092E11	0E0	3.234E-32	Reset	PRBS 7-tbit
Lnk 27	Quads_233MGT_X1Y55TX Incutp_01	Quads_233MGT_X1Y55RX Incutp_01	1.761 Gbps	3.092E11	0E0	3.234E-32	Reset	PRBS 7-tbit
▼ % QSER 6 (4)								
Lnk 28	Quads_232MGT_X1Y52TX Incutp_01	Quads_232MGT_X1Y52RX Incutp_01	28.126 Gbps	4.904E12	0E0	2.039E-33	Reset	PRBS 7-tbit
Lnk 29	Quads_232MGT_X1Y53TX Incutp_01	Quads_232MGT_X1Y53RX Incutp_01	28.126 Gbps	4.904E12	0E0	2.039E-33	Reset	PRBS 7-tbit



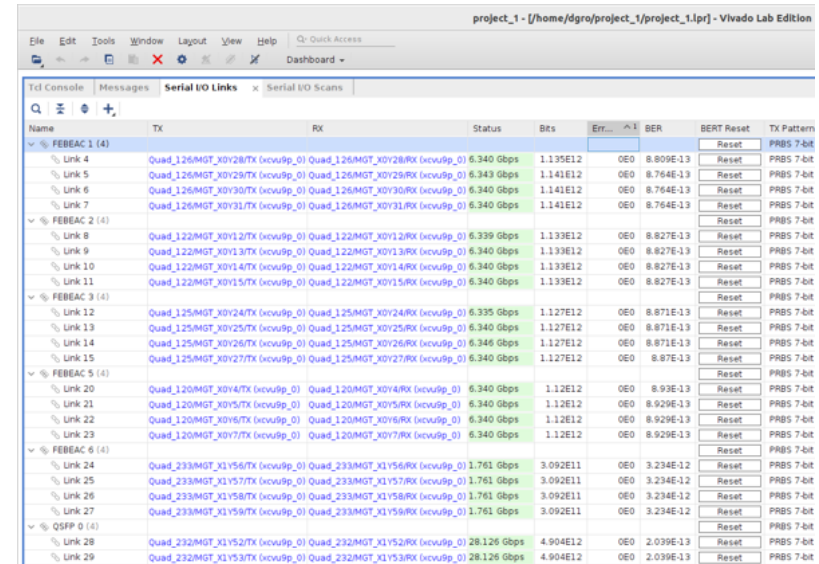
Readout Master Module Functionality Testing

- **IBERT**

- Integrated Bit Error Rate Test
- Xilinx IP core
- Test Multi-Gigabit Transceivers

- **Used to test**

- Ring transceivers (24x6.34Gbps)
- 100GbE transceivers (8x25.78Gbps)
- Timing system (Embedded EVR) transceiver (1x1.76Gbps)
- Also tests clock chip programming



project_1 - [/home/dgro/project_1/project_1.lpr] - Vivado Lab Edition

Name	TX	RX	Status	Bits	Err...	BER	BERT Reset	TX Pattern
FEBCAC 1 (4)							Reset	PRBS 7-bit
Link 4	Quad_126MGT_XD028/TX (xcvu9p_0)	Quad_126MGT_XD028/RX (xcvu9p_0)	6.340 Gbps	1.135E12	0E0	8.809E-13	Reset	PRBS 7-bit
Link 5	Quad_126MGT_XD029/TX (xcvu9p_0)	Quad_126MGT_XD029/RX (xcvu9p_0)	6.343 Gbps	1.141E12	0E0	8.764E-13	Reset	PRBS 7-bit
Link 6	Quad_126MGT_XD030/TX (xcvu9p_0)	Quad_126MGT_XD030/RX (xcvu9p_0)	6.340 Gbps	1.141E12	0E0	8.764E-13	Reset	PRBS 7-bit
Link 7	Quad_126MGT_XD031/TX (xcvu9p_0)	Quad_126MGT_XD031/RX (xcvu9p_0)	6.340 Gbps	1.141E12	0E0	8.764E-13	Reset	PRBS 7-bit
FEBCAC 2 (4)							Reset	PRBS 7-bit
Link 8	Quad_122MGT_XD012/TX (xcvu9p_0)	Quad_122MGT_XD012/RX (xcvu9p_0)	6.339 Gbps	1.133E12	0E0	8.827E-13	Reset	PRBS 7-bit
Link 9	Quad_122MGT_XD013/TX (xcvu9p_0)	Quad_122MGT_XD013/RX (xcvu9p_0)	6.340 Gbps	1.133E12	0E0	8.827E-13	Reset	PRBS 7-bit
Link 10	Quad_122MGT_XD014/TX (xcvu9p_0)	Quad_122MGT_XD014/RX (xcvu9p_0)	6.340 Gbps	1.133E12	0E0	8.827E-13	Reset	PRBS 7-bit
Link 11	Quad_122MGT_XD015/TX (xcvu9p_0)	Quad_122MGT_XD015/RX (xcvu9p_0)	6.340 Gbps	1.133E12	0E0	8.827E-13	Reset	PRBS 7-bit
FEBCAC 3 (4)							Reset	PRBS 7-bit
Link 12	Quad_125MGT_XD024/TX (xcvu9p_0)	Quad_125MGT_XD024/RX (xcvu9p_0)	6.335 Gbps	1.127E12	0E0	8.871E-13	Reset	PRBS 7-bit
Link 13	Quad_125MGT_XD025/TX (xcvu9p_0)	Quad_125MGT_XD025/RX (xcvu9p_0)	6.340 Gbps	1.127E12	0E0	8.871E-13	Reset	PRBS 7-bit
Link 14	Quad_125MGT_XD026/TX (xcvu9p_0)	Quad_125MGT_XD026/RX (xcvu9p_0)	6.346 Gbps	1.127E12	0E0	8.871E-13	Reset	PRBS 7-bit
Link 15	Quad_125MGT_XD027/TX (xcvu9p_0)	Quad_125MGT_XD027/RX (xcvu9p_0)	6.340 Gbps	1.127E12	0E0	8.87E-13	Reset	PRBS 7-bit
FEBCAC 5 (4)							Reset	PRBS 7-bit
Link 20	Quad_120MGT_XD04/TX (xcvu9p_0)	Quad_120MGT_XD04/RX (xcvu9p_0)	6.340 Gbps	1.12E12	0E0	8.93E-13	Reset	PRBS 7-bit
Link 21	Quad_120MGT_XD05/TX (xcvu9p_0)	Quad_120MGT_XD05/RX (xcvu9p_0)	6.340 Gbps	1.12E12	0E0	8.929E-13	Reset	PRBS 7-bit
Link 22	Quad_120MGT_XD06/TX (xcvu9p_0)	Quad_120MGT_XD06/RX (xcvu9p_0)	6.340 Gbps	1.12E12	0E0	8.929E-13	Reset	PRBS 7-bit
Link 23	Quad_120MGT_XD07/TX (xcvu9p_0)	Quad_120MGT_XD07/RX (xcvu9p_0)	6.340 Gbps	1.12E12	0E0	8.929E-13	Reset	PRBS 7-bit
FEBCAC 6 (4)							Reset	PRBS 7-bit
Link 24	Quad_233MGT_X1Y56/TX (xcvu9p_0)	Quad_233MGT_X1Y56/RX (xcvu9p_0)	1.761 Gbps	3.092E11	0E0	3.234E-12	Reset	PRBS 7-bit
Link 25	Quad_233MGT_X1Y57/TX (xcvu9p_0)	Quad_233MGT_X1Y57/RX (xcvu9p_0)	1.761 Gbps	3.092E11	0E0	3.234E-12	Reset	PRBS 7-bit
Link 26	Quad_233MGT_X1Y58/TX (xcvu9p_0)	Quad_233MGT_X1Y58/RX (xcvu9p_0)	1.761 Gbps	3.092E11	0E0	3.234E-12	Reset	PRBS 7-bit
Link 27	Quad_233MGT_X1Y59/TX (xcvu9p_0)	Quad_233MGT_X1Y59/RX (xcvu9p_0)	1.761 Gbps	3.092E11	0E0	3.234E-12	Reset	PRBS 7-bit
QSFP 0 (4)							Reset	PRBS 7-bit
Link 28	Quad_232MGT_X1Y52/TX (xcvu9p_0)	Quad_232MGT_X1Y52/RX (xcvu9p_0)	28.126 Gbps	4.904E12	0E0	2.039E-13	Reset	PRBS 7-bit
Link 29	Quad_232MGT_X1Y53/TX (xcvu9p_0)	Quad_232MGT_X1Y53/RX (xcvu9p_0)	28.126 Gbps	4.904E12	0E0	2.039E-13	Reset	PRBS 7-bit

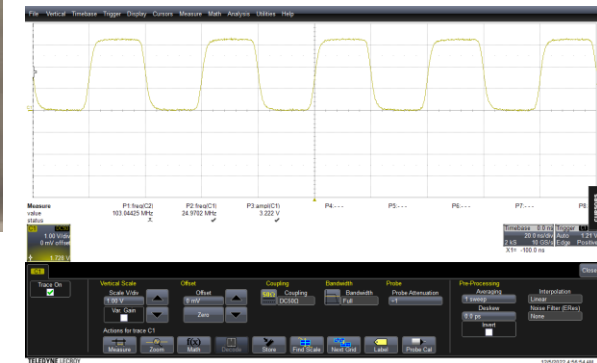
Readout Master Module Functionality Testing

- Other interface tests

- JTAG
- UART
- 1G Ethernet
- Touchscreen
- LEMO
- HFBR



```
Device DNA: VCCINT:
0x40020000 3.750 W
0x01178A25 VCC1V8:
0x3C710245 1.875 W
Git Hash: VADJ:
0xAAAAAAAA 0.075 W
0xBBBBBBBB VCC1V2:
0xC0000000 0.375 W
Bitstream Generation Time: MGTAVCC:
00-00-00 00-00-00 1.975 W
Up Time: MGTAVTT:
00 00 00.28 14.10 W
Current FPGA Temperature: VINTBRAM:
23.6 degrees C 0.200 W
Highest FPGA Temperature:
32.0 degrees C
```





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Questions

Product Longevity

*A product lifecycle is typically defined by four main phases: introduction, growth, maturity, and decline. Xilinx designs products and creates the supporting supply chain with the clear intent to support a minimum **15+ year lifecycle***, starting from first production release. Xilinx parts are used extensively in numerous applications that require a long operational lifetime, and therefore, Xilinx makes a strong commitment to product longevity. With this commitment, although the minimum lifecycle is 15 years, customers will see that the majority of families will be supported much longer. The longevity of Xilinx products is longer than ASSPs, ASICs, and other major FPGA suppliers. In the case of a last time buy, Xilinx does follow the JEDEC standard.*

<https://www.xilinx.com/support/quality/support.html#productLongevity>