
# Detector Readout for ESS Instruments

## (Focusing on Front End Readout)

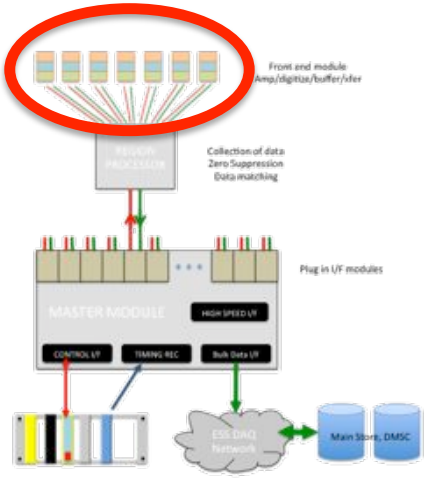
IKON-10
18th Feb 2016

# ESS Instruments.... all about collaboration

The growth in IKON meetings reflects a change in pace; our objectives are set, the clock is ticking, we have to pull together and deliver.

Detector Group exists to support the instrument teams and we are already talking to most of you Please make the most of us!!!

Readout breaks down into a back end interface (connections to the standard ESS data and control networks, which should be the same for most instruments), and front end digitization where the specific requirements of the instrument detector system are paramount..




This talk focuses on the front end. We are promoting enabling work for new technologies with generic developments funded with In-Kind (STFC) and BrightnESS support (EU funding).

Science & Technology Facilities Council

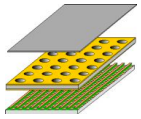
BrightnESS

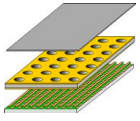
# Detector Baseline for Early Instruments

EUROPEAN SPALLATION SOURCE

| Instrument | Instalation Start (est.) | Lead Institute | Main Detector Technology | Main Detector Developer | Front End Readout | FE Readout Developer | Integration Model |
|---|---|---|---|---|---|---|---|
| LOKI | Q1 2019 | ISIS | BandGEM | Milan | Gemma/Gemini | Milan/INFN | B |
| NMX | Q1 2019 | ESS | Gd-GEM | CERN/ESS (BrightnESS) | VMM | CERN/ESS (BrightnESS) | A |
| ODIN | Q3 2019 | TUM/PSI | MCP, Silicon, etc | Lots | Lots | Lots | XX |
| BEER | Q4 2019 | HZG/NPI | A1CLD, AmCLD | HZG/DENEX | Delay Line | HZG/DENEX | Probably C |
| SKADI | Q4 2019 | FZJ | SoNDE Pix Scinit | SoNDE | IDEAS ASIC | SoNDE | Probably B |
| DREAMS | Q4 2019 | FZJ | Jalouise | Julich/CDT | CIPix | Julich/CDT | C/X |
| ESTIA | Q1 2020 | PSI | Multi-Blade | Wigner/ESS (BrightnESS) | VMM | ESS Led (IK + BrightnESS) | A |
| C-SPEC | Q2 2020 | TUM | Multi-Grid | ILL/CERN (BrightnESS) | VMM | ESS Led (IK + BrightnESS) | A |
| CAMEA/BIFROST | Q1 2021 | DTU | He3 Tubes | Commercial | Commercial? | Commercial? | Probably X |
| HEIMDAL | Q1 2021 | AU(DK) | WLS-Scinti | Unknown | ??ASIC? | Unknown | Probably B |
| FREIA | Q3 2021 | ISIS | Multi-Blade | Wigner/ESS (BrightnESS) | VMM (MB) | ESS Led (IK+ BrightnESS) | A |
| T-REX | Q4 2021 | Julich | Multi-Grid | ILL/CERN (BrightnESS) | VMM | ESS Led (IK+ BrightnESS) | A |
| MAGIC | Q4 2021 | LLB | Jalouise | Julich/CDT | CIPix | Julich/CDT | C/X |
| MIRACLES | Q1 2022 | ESS-B | He3 Tubes | Commercial | Commercial? | Commercial? | Probably X |
| VESPA | Q3 2022 | CNR | He3 Tubes | Commercial | Commercial? | Commercial? | Probably X |
| VOR?? | | WIGNER | Multi-Grid | ILL/CERN (BrightnESS) | VMM | ESS Led (IK+ BrightnESS) | A |

# Detector Integration Models





Pre AMP

A(A)

FE BOARD

FPGA ADAPT

Data Collection Signal Processing

Generic Back End

B

FE BOARD

FPGA ADAPT

Data Collection Signal Processing

Generic Back End

C

FE BOARD

Data Collection Signal Processing

Generic Back End

X

FE BOARD

Data Collection Signal Processing

Generic Back End

XX

FE BOARD

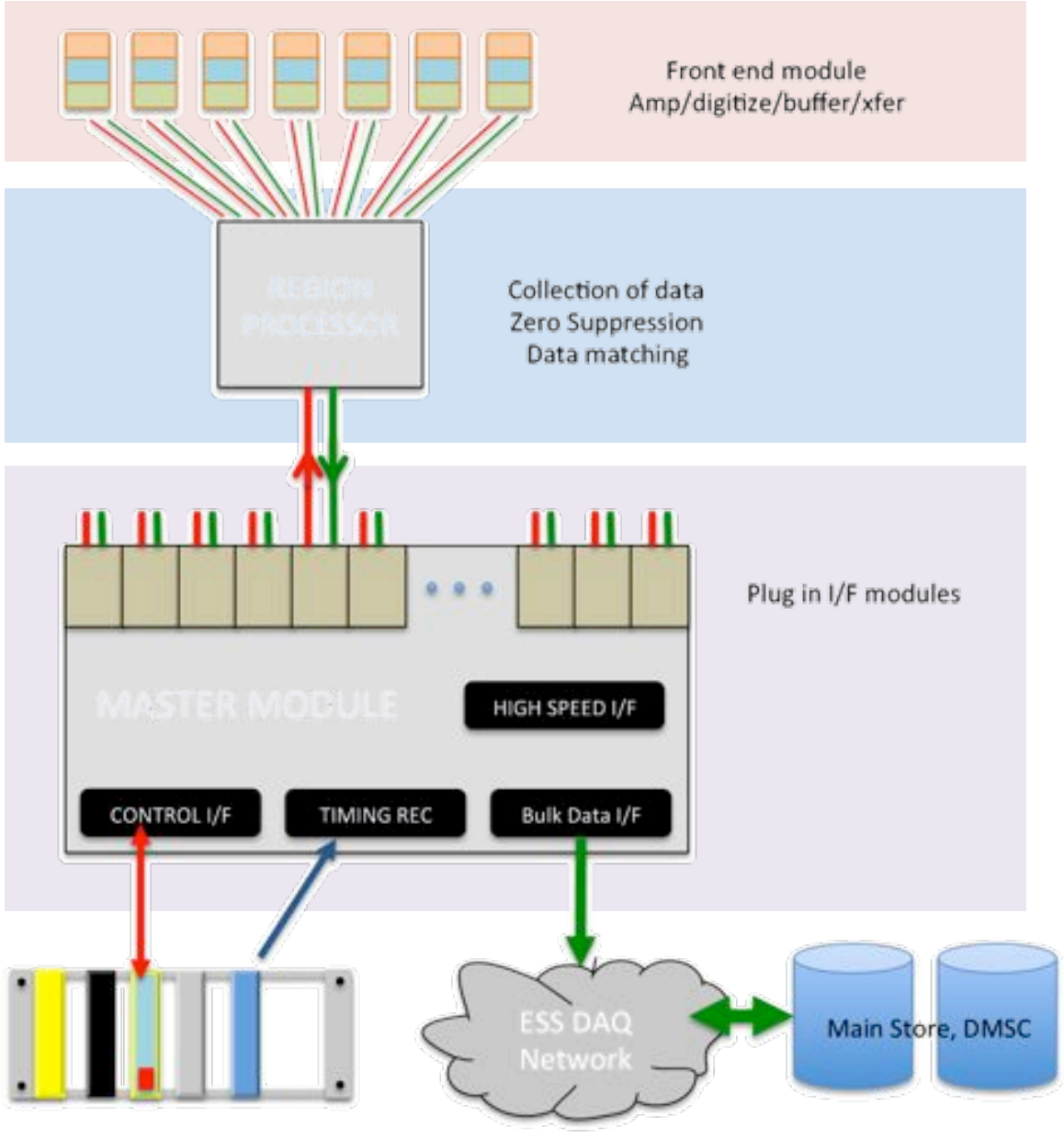
Data Collection Signal Processing

Specific Back End

DMSC

COMPUTE

# Standard Readout Model




There are three logical layers in the generic readout layout. Not all layers are required in all instruments.

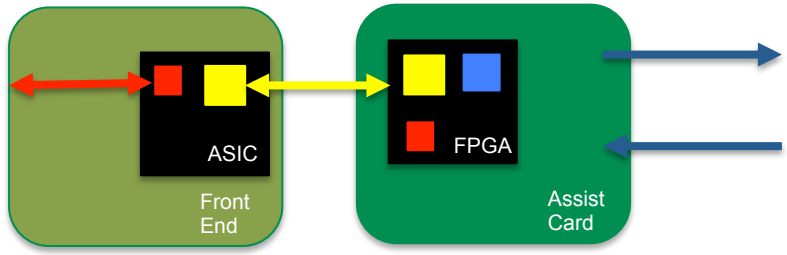
Front end digitizes signals and timestamps. In some cases we might also want to do some first level signal processing there, eg combine clusters.

Region processor collects data to perform full zero suppression, matching of signals from different parts of the detector, etc.

Back end interfaces to ESS systems, and sends data to computing infrastructure, online processing, data store, etc,
Can be multiple output streams.

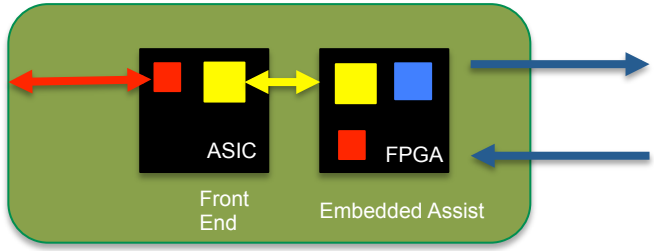
# Assister Module/Core

The ‘Assister’ is a hardware card (or equivalent firmware core that can be used in existing FPGA hardware) that interfaces to the ESS detector data collection system in a standard way.

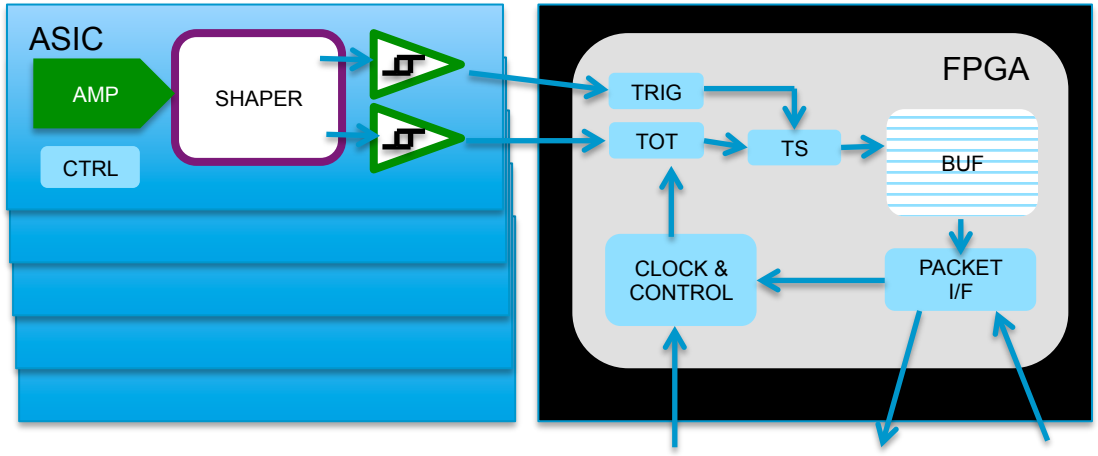



Can be used to adapt an ASIC on a front end card  Can provide:

- Timestamp
- ToT counting
- Comms to next layer (ring or star).




For example, pure analogue ASICs could be adapted to ESS requirements




In-Kind project planed for 2016 (STFC–RAL)

# ESS ASIC Review

As part of their contribution, RAL Microelectronics (STFC) made a 'market survey' of ASICs suitable for gas based detectors (MWPC/GEM)

Will be available on Confluence/wiki soon...

We have chosen the ATLAS VMMx chips developed by Brookhaven as being suitable for a wide range of applications at ESS, and testing will be undertaken confirm usefulness.

2nd generation chips available in some numbers soon (~April)and. 3rd generation part will be available later this year.

ESS review of ASICs – Initial list of charge/current readout front end chips.

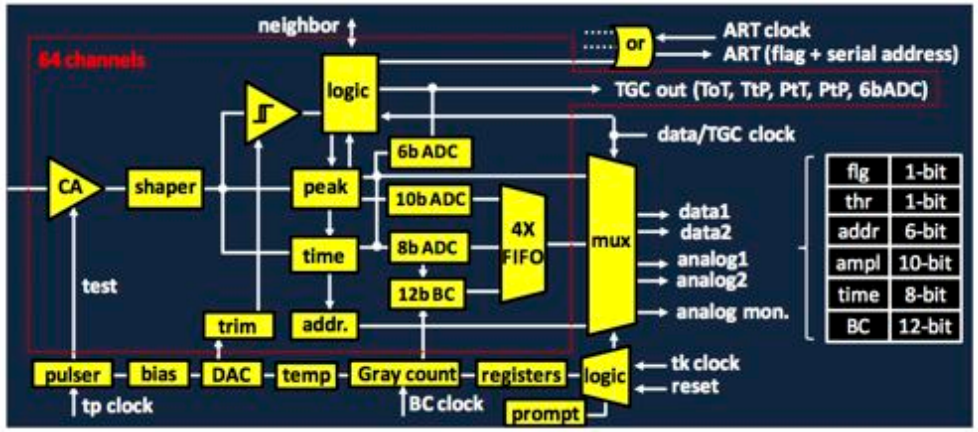
Contents

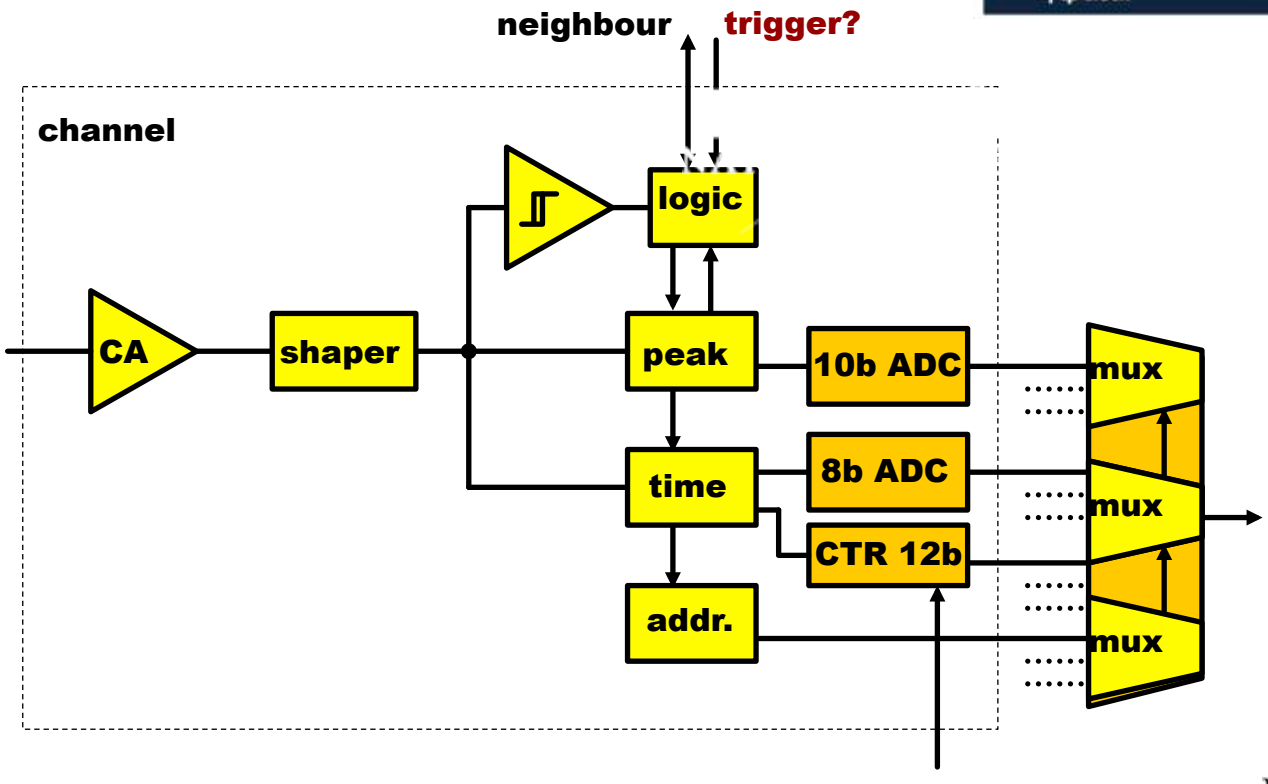


1

# VMM2 Readout ASIC

VMM2 Many modes of operation
We would use it in a 'buffered' mode
Hit rate theoretical readout limit ~ 5Mhz for VMM2
Real rate limit dependent on many factors
VMM3 will support VMM2 mode for non LHC use.




Sub nsec timing resolution

Wide dynamic range

Can cope with large detector capacitance

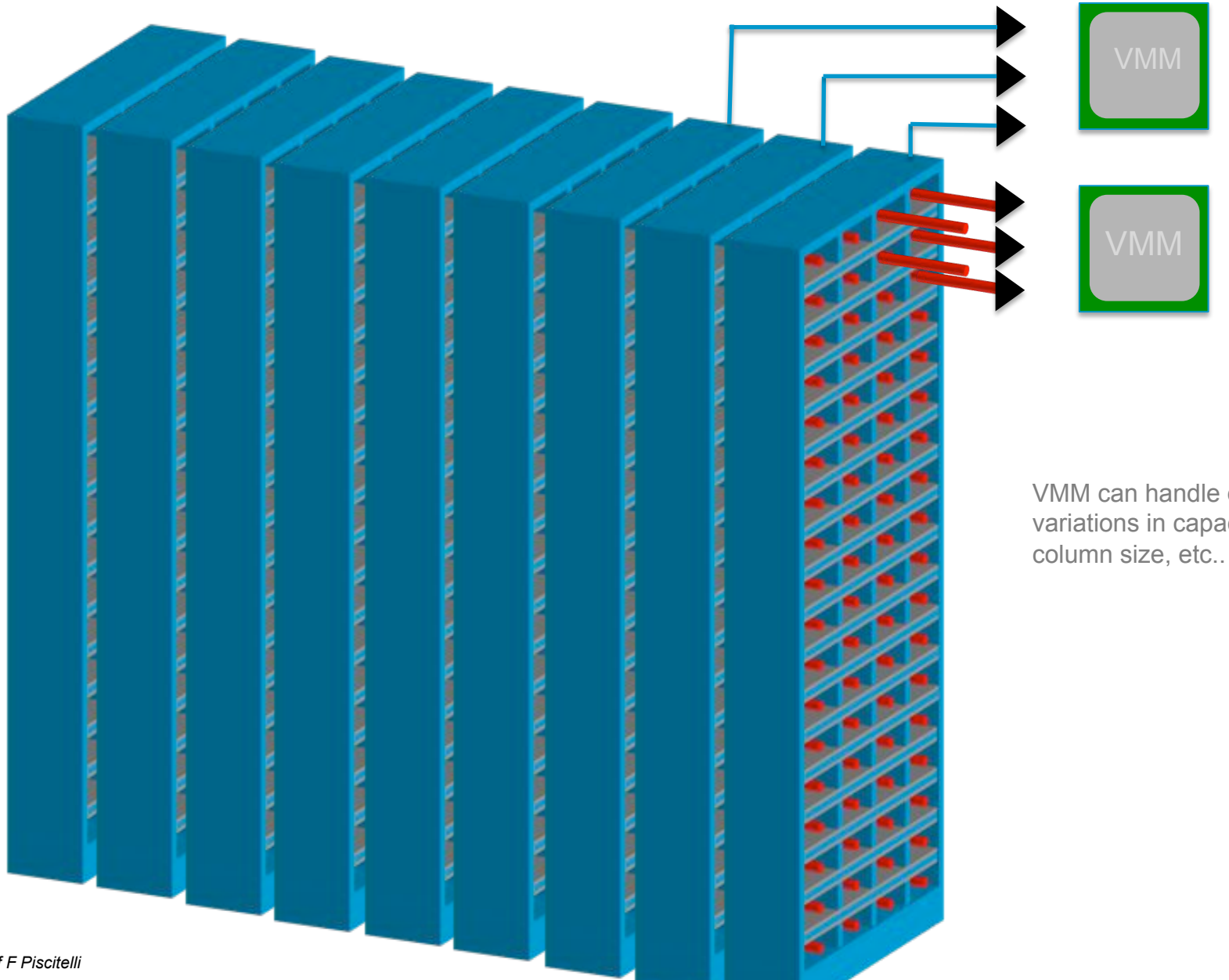
VMM chips design to service multiple detectors in ATLAS upgrade

*Diagrams courtesy of G De Geronimo*


EUROPEAN
SPALLATION
SOURCE

# Detectors/Instruments where we think VMM ASICs might be useful

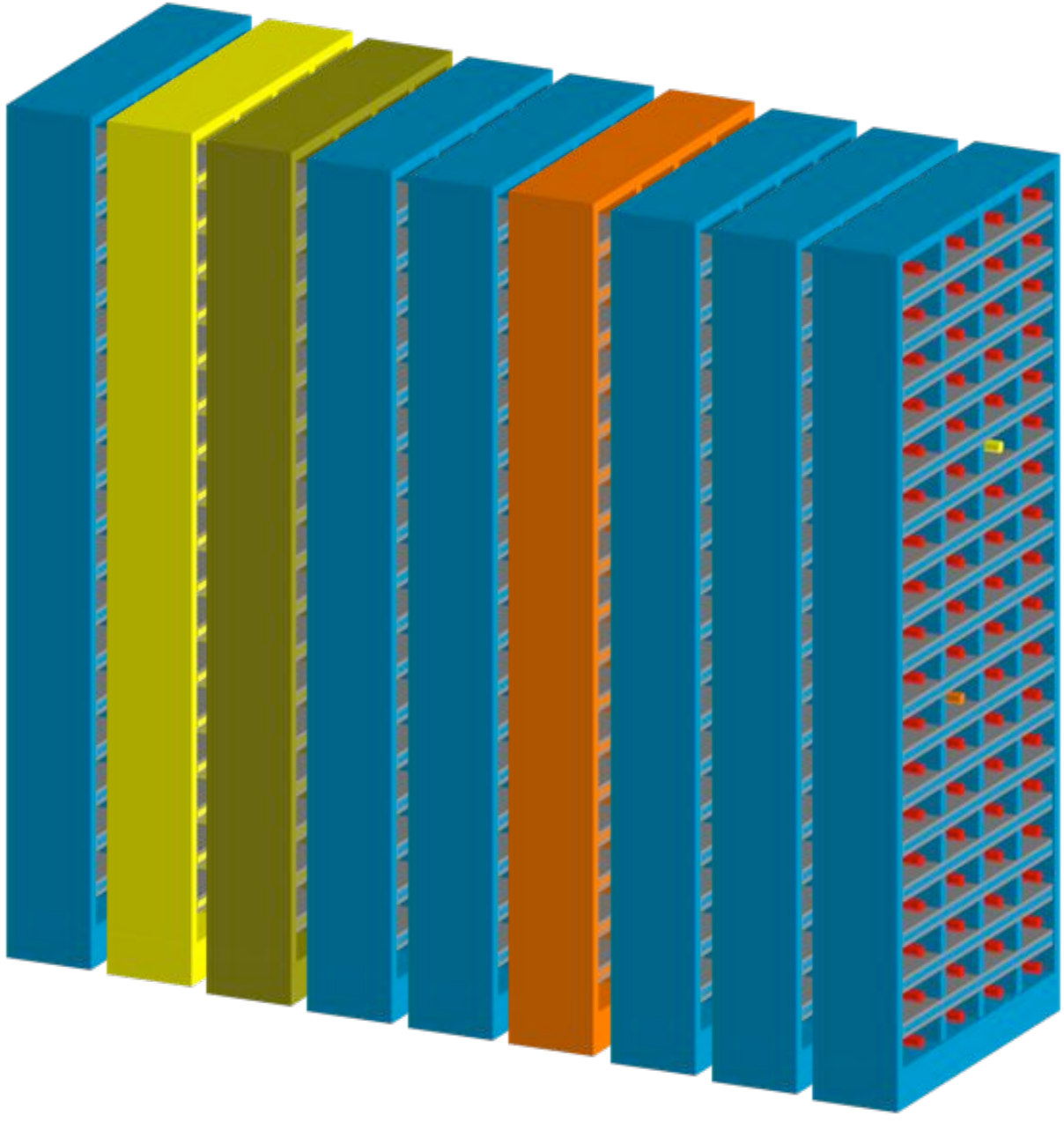
# Multi-Grid B10 Detector (C-SPEC/TREX/VOR)




VMM can handle dual polarity, variations in capacitance due to column size, etc..

*Diagrams courtesy of F Piscitelli*

# Combinatorial Issues



Need to match hits on wires with hits on grids.

There can be many grids in a column, eg 160 grids for C-SPEC baseline design.

Can use timing and size of pulse to associate hits.

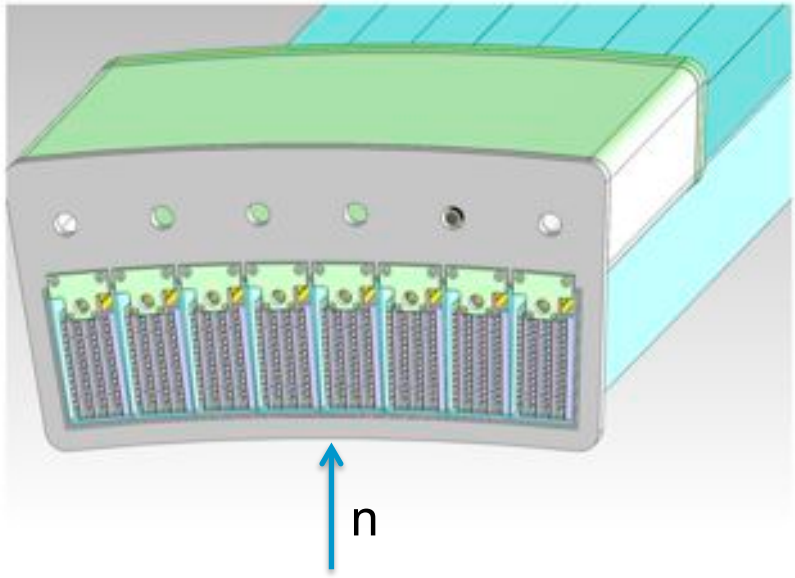
Timing accuracy limited by pulse shape and method used to extract time from pulse (eg leading edge of pulse maximum).
Different pulse shapes will have different offsets from true pulse time.

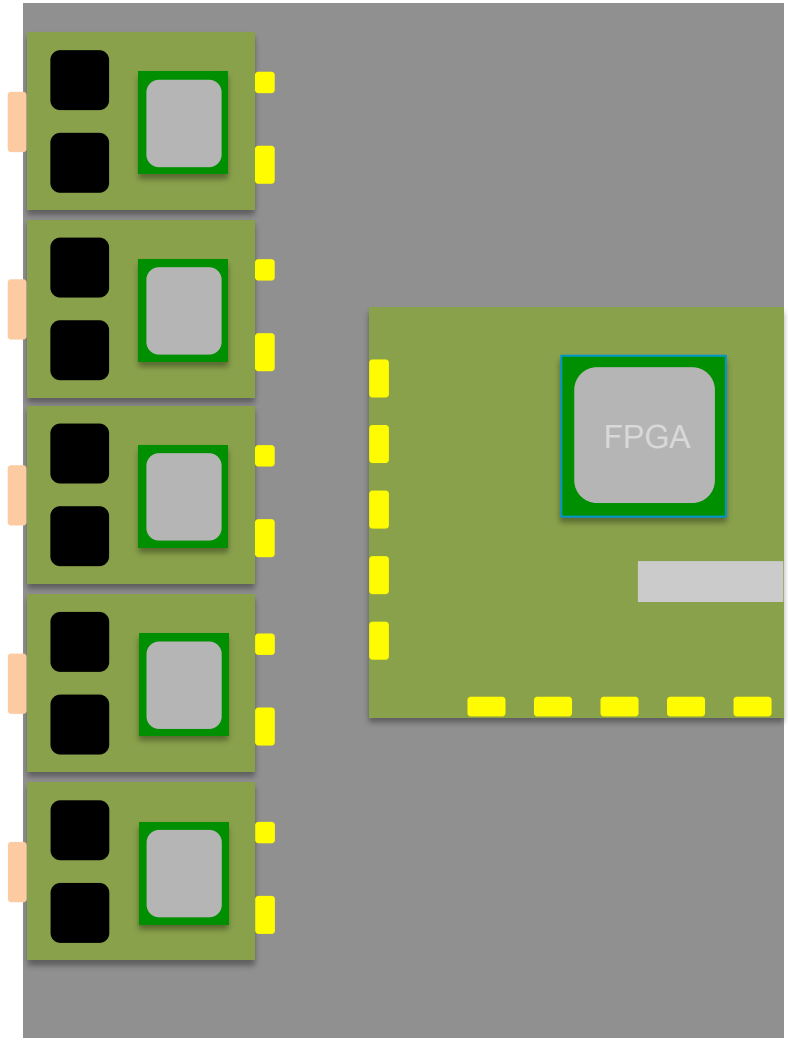
Charge may be shared between grids. Sometimes charge may be lost because a neighbour grid did not fire (below threshold).
VMM neighbour function helps.

Interpolation between grids on the basis of charge sharing is possible.

*Diagrams courtesy of F Piscitelli*

# Readout for Multi-Grid




Electronics usually located at one end. Putting grid readout behind the column is also possible.

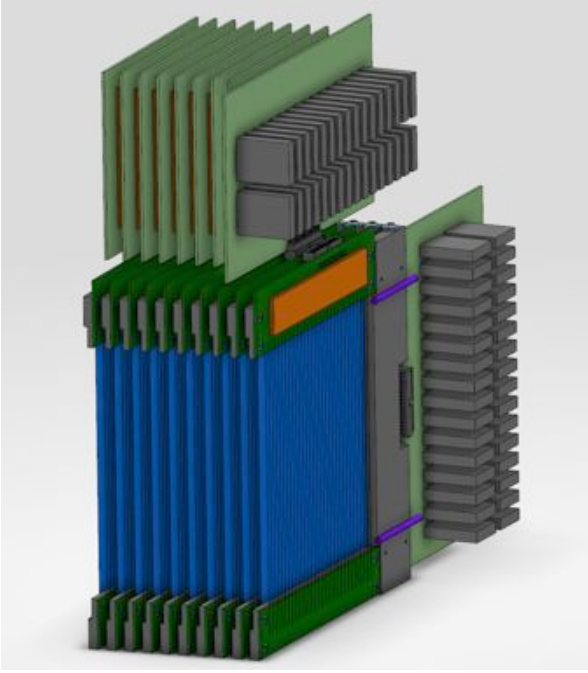
Modular readout with front end cards with ASICs and supporting FPGAs. These communicate with module cards with high speed data links to the back end readout.

We are investigating the use of Atlas VMM ASICs (64 channel).

Power budget is ~30mW per channel plus ~10W overhead.

Eg C-SPEC quad column generates ~30W
(~1KW for full 12m wide 120 column detector)

# *Multi-Blade: Inclined B10 MWPC (ESTIA/FREIA)*

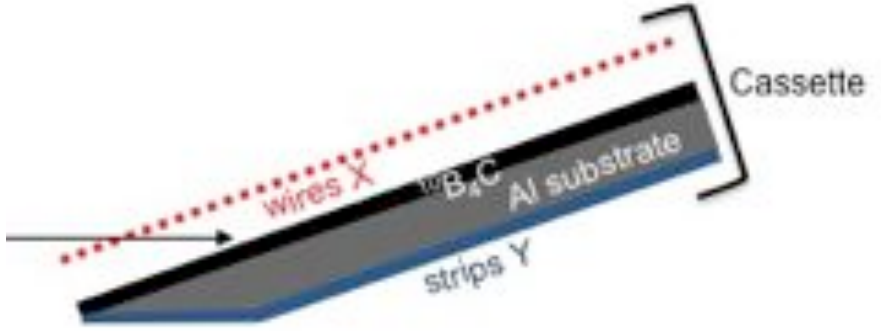


Inclined converter to improve efficiency.

Projection effect improves position resolution in X, ie as you sweep across the wire plane.

Similar concept to Jalouise, A1CLD.

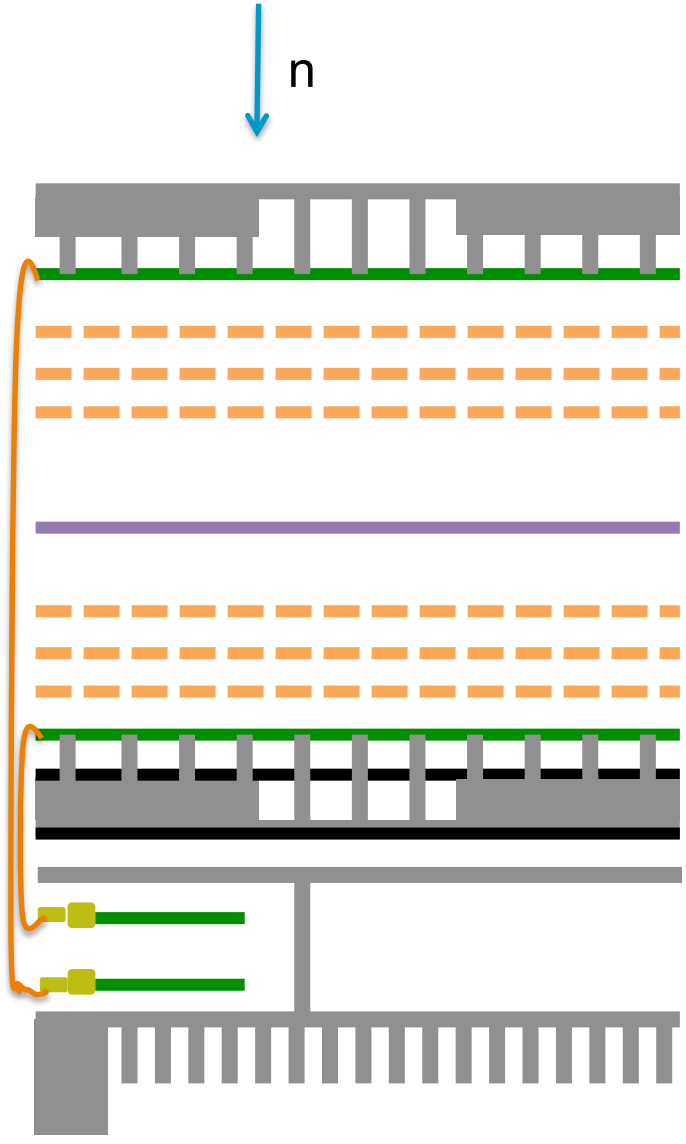
VMM chips can handle the high rates expected in reflectometry.






*Diagrams courtesy of F Piscitelli*

# NMX: Gd-GEM

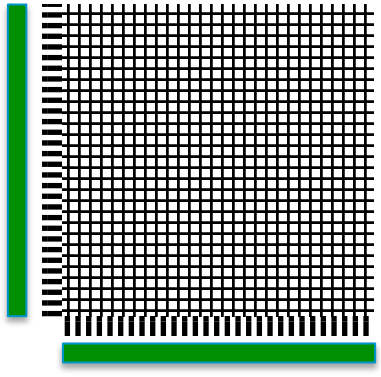


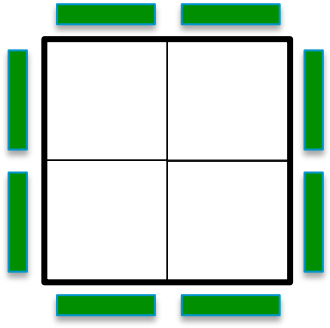

Convertor layer with triple gem behind.

Possibly gem detector in front and behind.

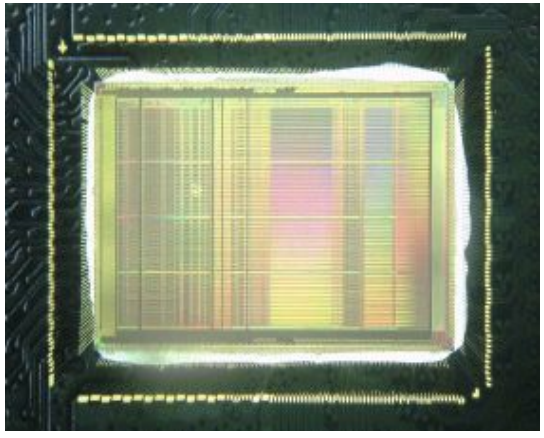
Broken into 4 segments with strips readout at free edges. Higher segmentation would require more complicated connections segments

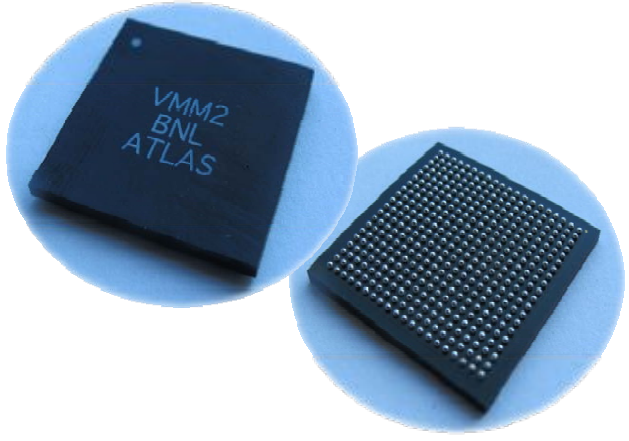
Demonstrators being tested with APV chips but VMM integration well underway (SRS system).





# VMM2 In reality







Big chip, ~115 sq mm
Bare die or custom packaged BGA
SRS front end cards exist, to be used for RD51 testing
Not enough available for others to have for testing.
Chips available from current production run. Due April.

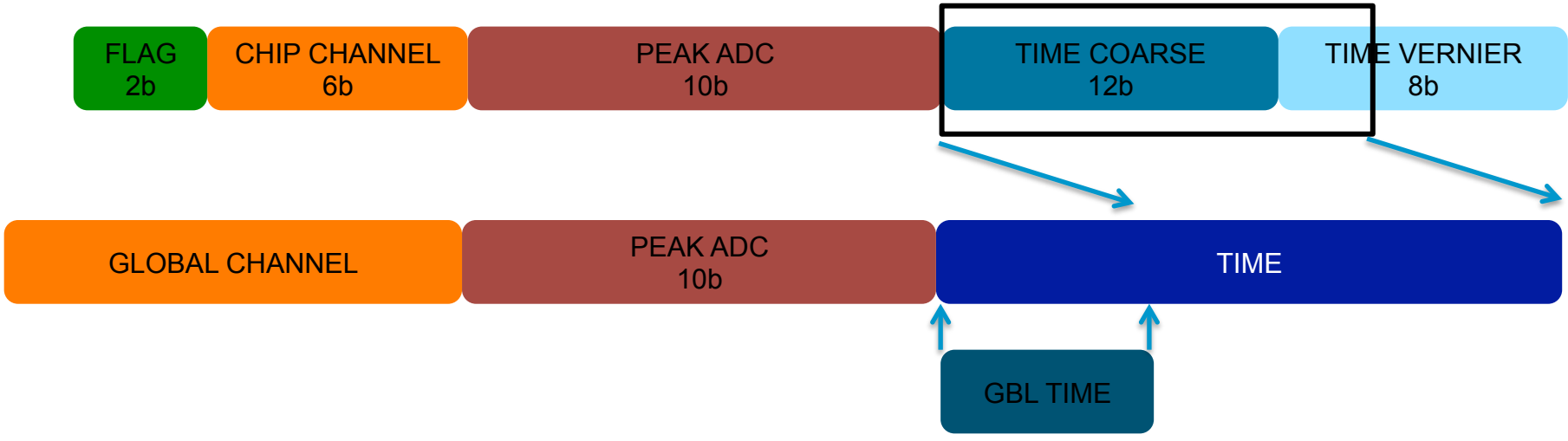
BrightnESS

# Pulse readout


Data produced by ASIC (VMM2) is 38 bits for each ‘hit’, of pulse over threshold.
Time is measured at shaped peak.
Shaper has peaking time of 25,50,100,200nsec
Eight gain ranges.
Dual polarity
Timing designed to run at 40Mhz counter (100usec wrap), 256 bit vernier, but*

Actual sequencing and operation of chip not certain (to us), will be verified with first parts. VMM2 parts available soon.

Front-end or back-end FPGAs can slice/combine/format data as required



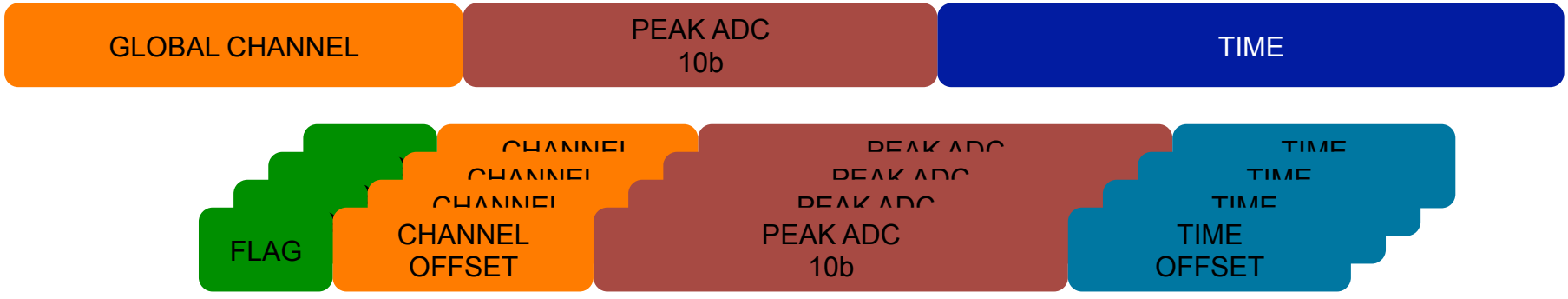
# Data Merging (Pre-clustering)


Charge sharing between grids means several channels may be hit by a single pulse (or deliberatly triggered using the ‘neighbour’ feature).

Can consider using a ‘delta’ format to reduce the overall data volume from a chip. Clustering to be studied on the basis of simulated data.

Index a group of adjacent hits against the first hit, no need to repeat full time or channel info.

Whatever we do, it will always be possible to expand back to individual channel, pulse height, and time info offline. Ie lossless compression.




# Other Front End Readout

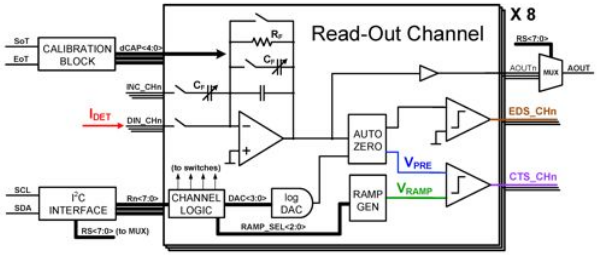
# LoKI: Band-GEM

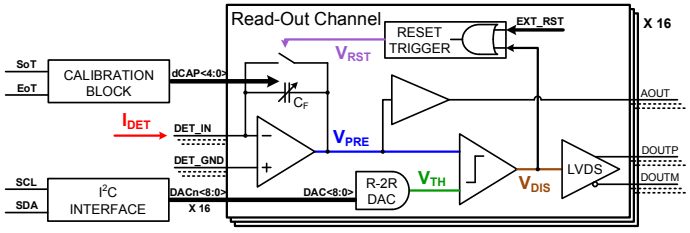
Inclined B10, followed by triple GEM.

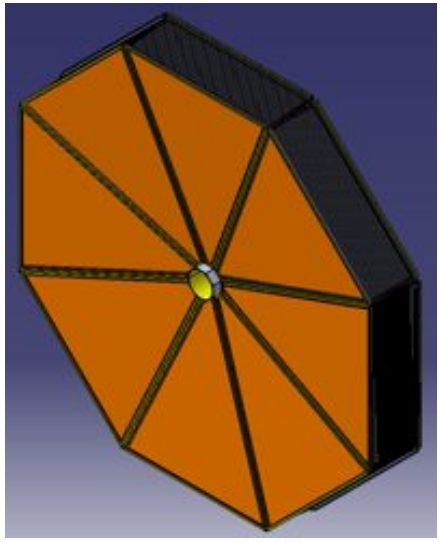
Readout pads, not strips. Readout electronics placed behind the pads.

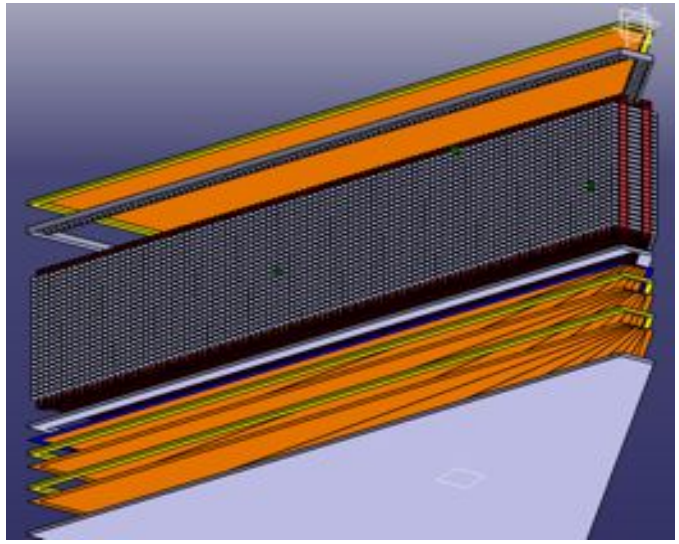
Dedicated ASIC being developed: GEMMA/GEMINI.
Discriminator type

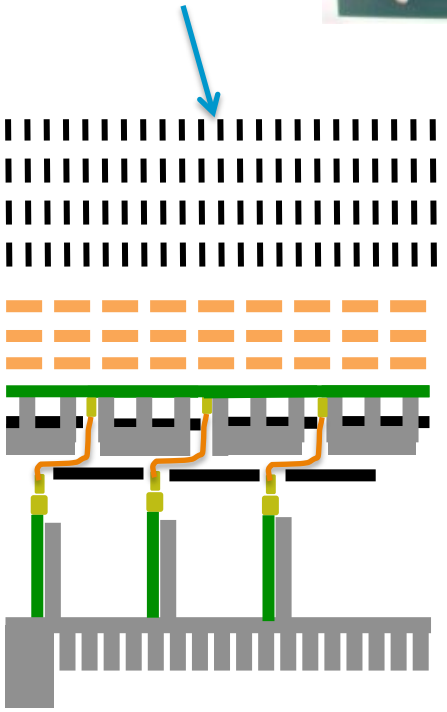
ASIC support logic likely to be merged with ESS assister firmware for full front end

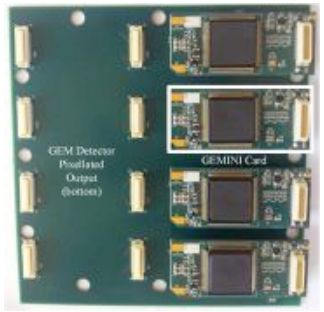










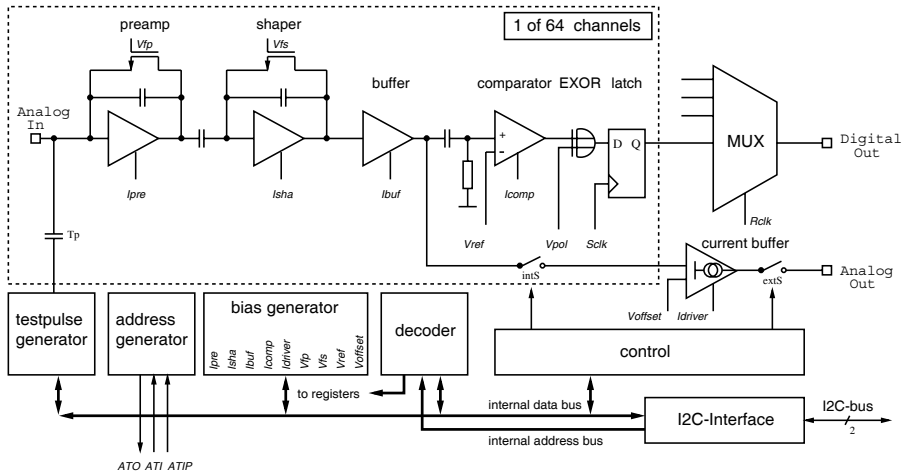

*Diagrams & Phtographs courtesy of IFP-CNR and Collaborators*

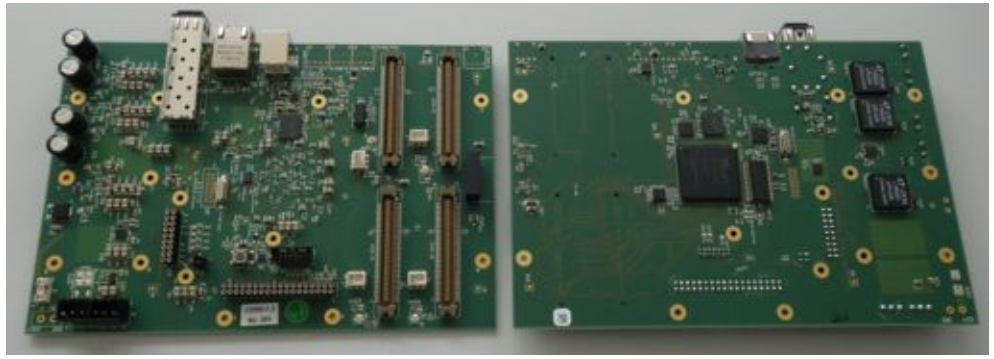
# DREAMS/MAGIC: Jalouise

Inclined B10, similar concept to Multi-Blade, A1-CLD. In production for Powtex.

Frond end readout cards based on CIPix ASIC derived from Particle Physics MWPC.
Modular readout. Module cards carry ASICs boards and provide supporting FPGAs.
High speed data links to the back end readout.

Concept of operation compatible with ESS generic back end readout.





*Diagrams &n Photographs courtesy of CDT*

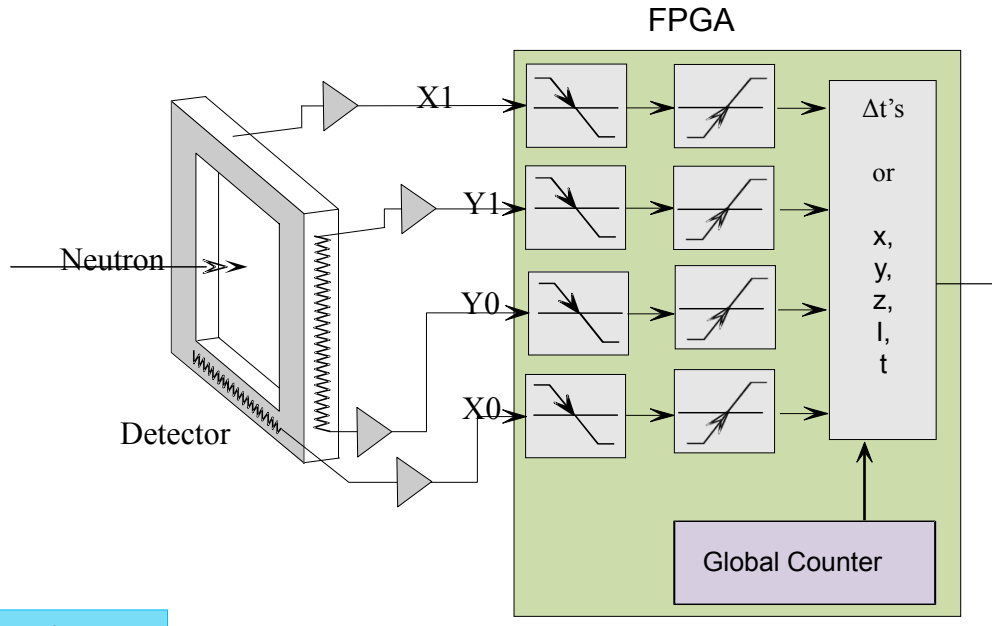
# BEER: A1-CLD  Am-CLD

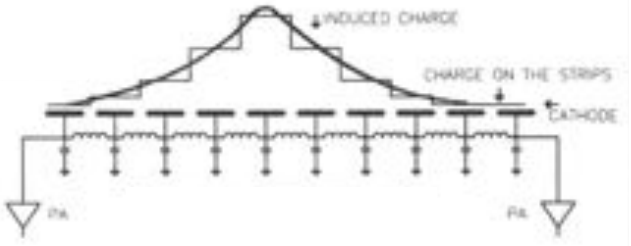
A1-CLD Inclined B10 MWPC  (similar concept to Multi-Blade, Jalousie).

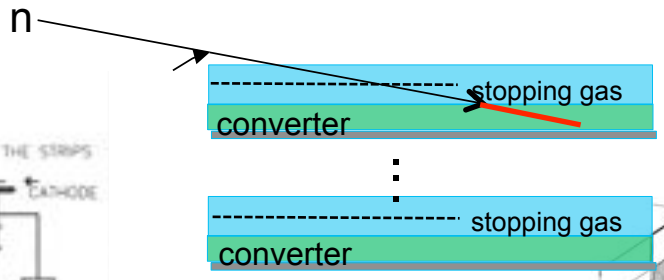
Am-CLD stacked B10 MWPC (corresponds to Multi-Grid)

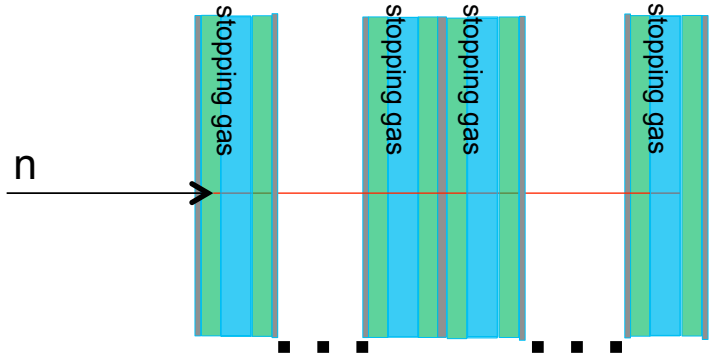
Delay line readout to TDC/FPGA

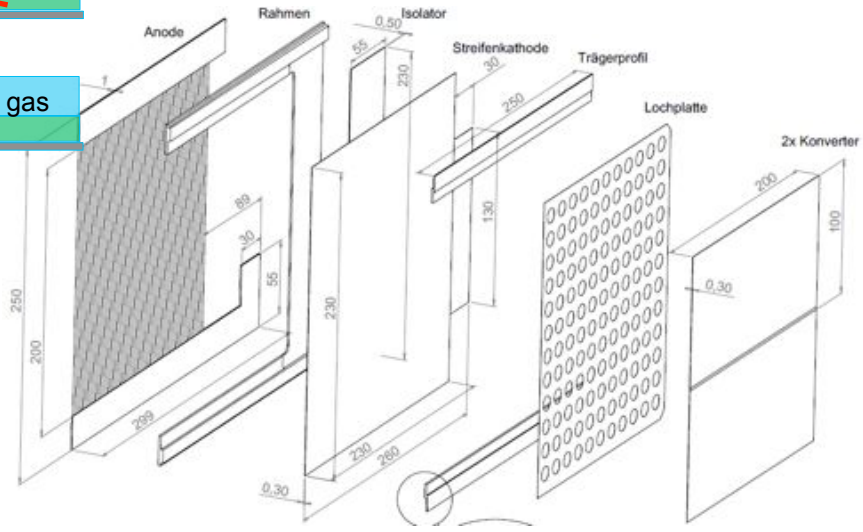
Concept of operation compatible with ESS back end readout.




*Diagrams courtesy of HZG/DENEX*

# He3 Tubes (BIFROST/MIRACLES/VESPA)

EUROPEAN SPALLATION SOURCE

Mature technology, well understood

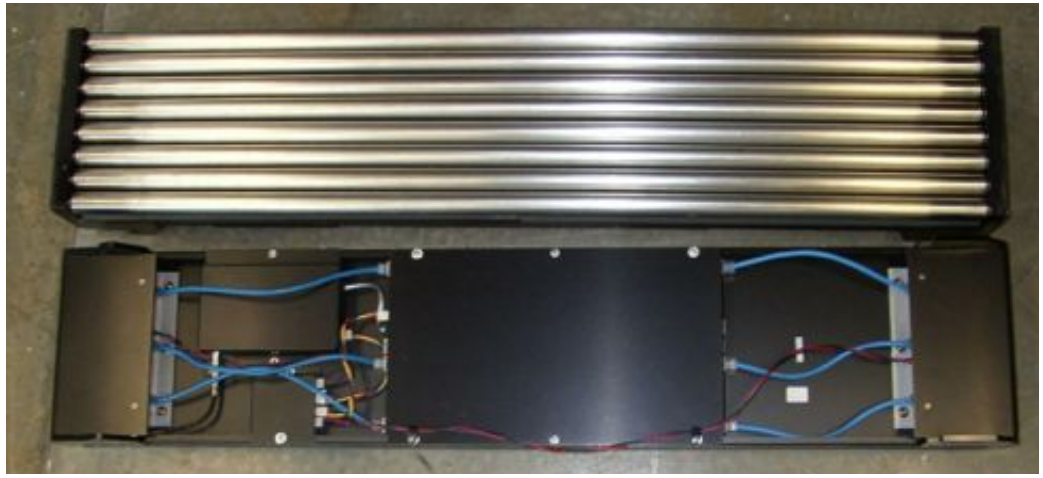
Resistive wire readout requires high precision ADC. High cost of discrete ADC not an issue here. Limited multi-pulse capability

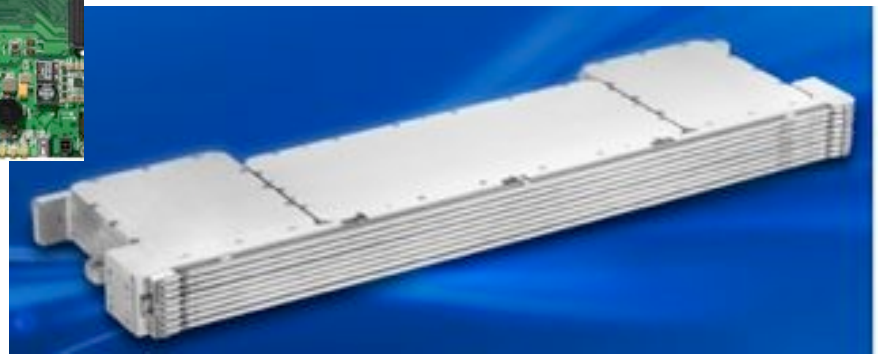
ISIS get good results with 10 bit ADCs. ADCs commercially available, eg Mesytec etc.

14/16 bit low power ADCs available at high sample rates (>100Msps).

Can go to a ‘one stop shop’, eg GERS will configure and sell you a complete detector package including readout to module level.

Anticipate most FPGA based solutions can be interfaced to standard ESS back end readout. Integration model X or XX



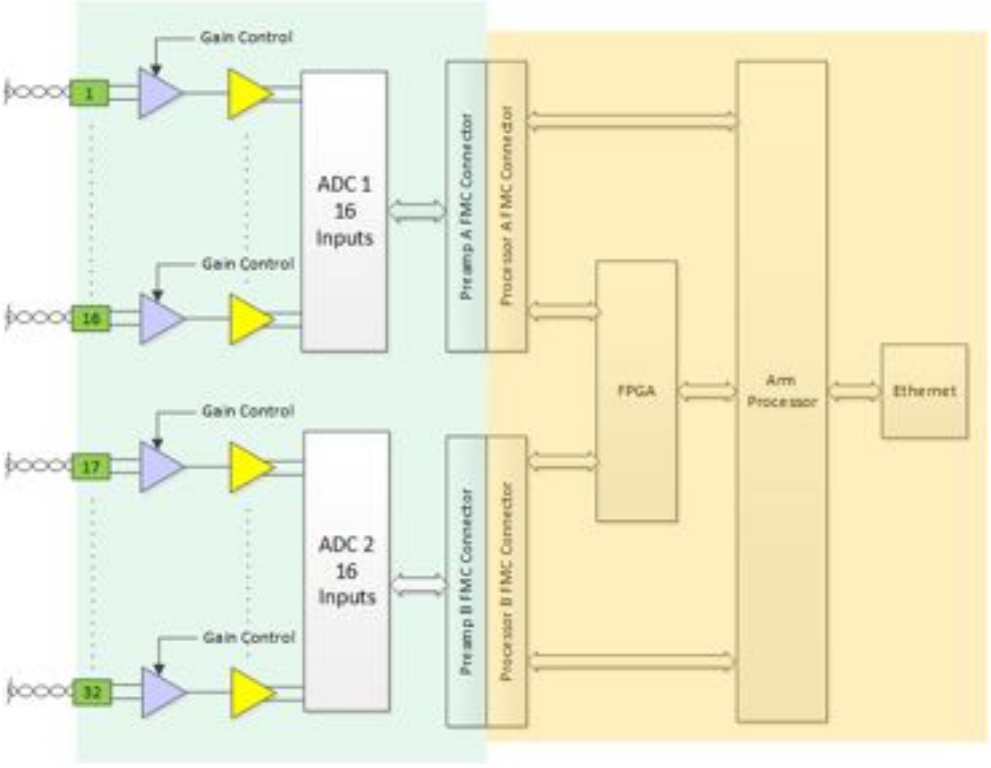


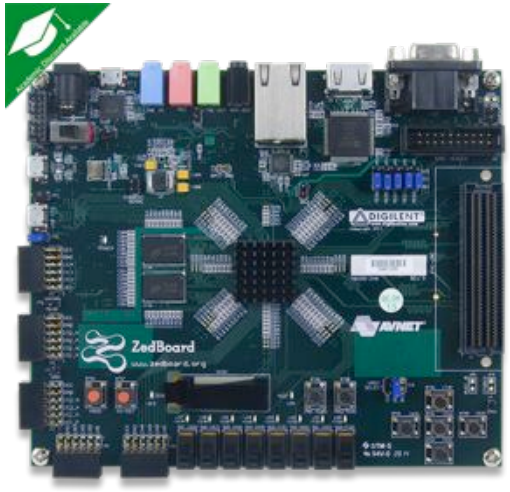


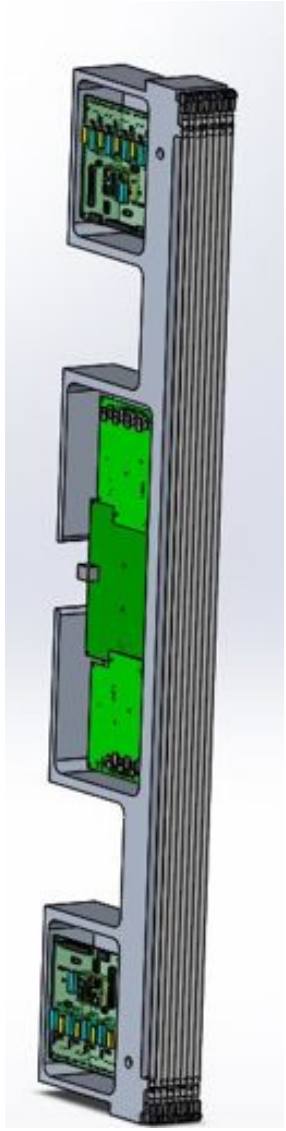
*Material from BES workshop and GERS*

# GE Reuter Stokes NeuAcq

Integrated system, tubes, preamp, ADC boards, FPGA SOC motherboard.
FPGA board is similar to boards used at ESS for prototyping work.
Commercial network protocols with embedded timing.
Simplest integration is to re-work FPGA code, but external conversion to GERS protocols also possible.





*Material from GERS & Diligent.*

# Concluding comments

Detector technologies and associated readout for the first 16 instruments all well under control. We depend on our In-Kind partners and EU funding for readout provision.

We must standardize where technically necessary, and where the cost benefits cannot be ignored.

At the same time, the availability of multiple technical approaches to the solution of any specific problem greatly reduces risk.

Detector group has been using Confluence for some time, and there is a large volume of material already there. *If you can't find what you need, please ask!!!!!*

*https://ess-ics.atlassian.net/wiki/display/DG/Detector+Group*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