Polish IKC for BCM and BPM systems

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WUT-ISE / PEG

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Polish Electronic Group

1. National Centre for Nuclear Research (NCBJ Świerk)
2. Łódź University of Technology
   - Department of Microelectronics and Computer Science
3. Warsaw University of Technology
   - Institute of Electronic Systems

WARSAW UNIVERSITY OF TECHNOLOGY

Experience

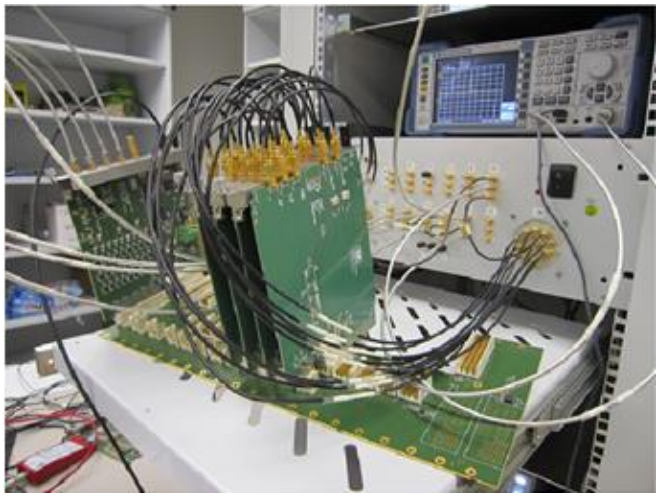
- Development of complex electronic circuits and systems
- Analog and microware circuits
- Digital circuits and VHDL
- Software
- Long (~15 years) collaboration with DESY: mainly LLRF, Synchronization and Special Diagnostics for FLASH and European XFEL

Selected Projects for MTCA Based LLRF Control System for XFEL and Other Accelerators

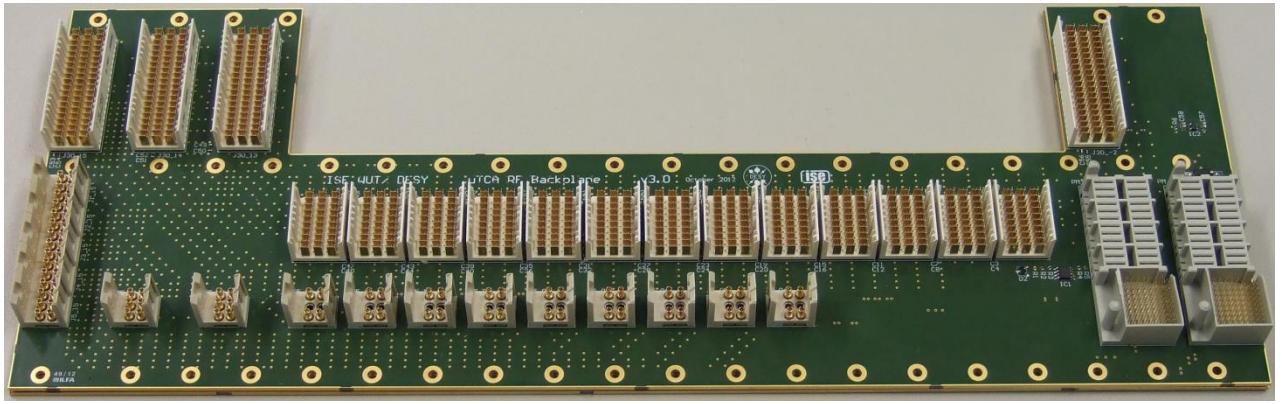
10-channel Downconverter
uRTM form factor
1.3GHz -> 54 MHz
ISE, DESY

2-channel Vector Modulator
uRTM form factor
100 MHz - 6GHz
ISE, DMCS

Automated teststand for MTCA components
ISE



RF Backplane for MTCA crates. Simplifies cable management. ISE, DESY



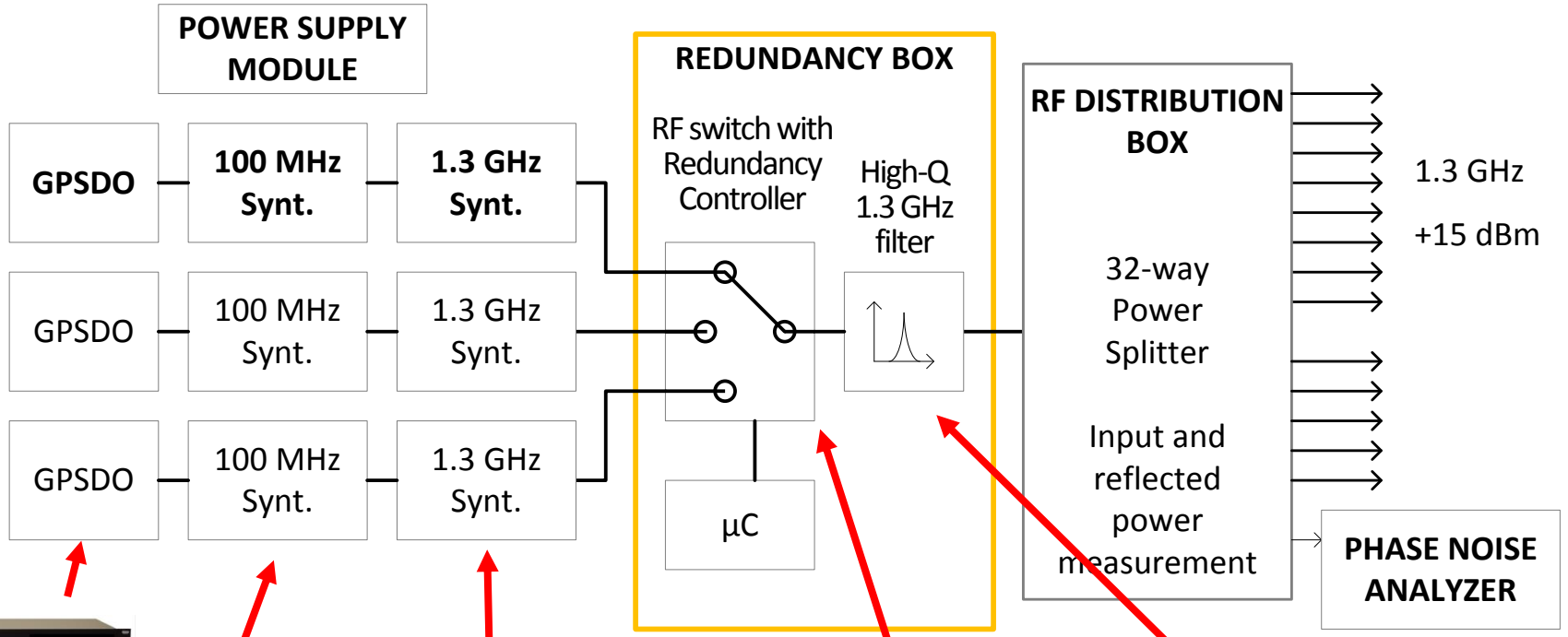
Master Oscillator System for FLASH

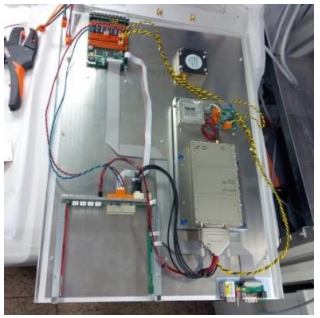
Injector Area

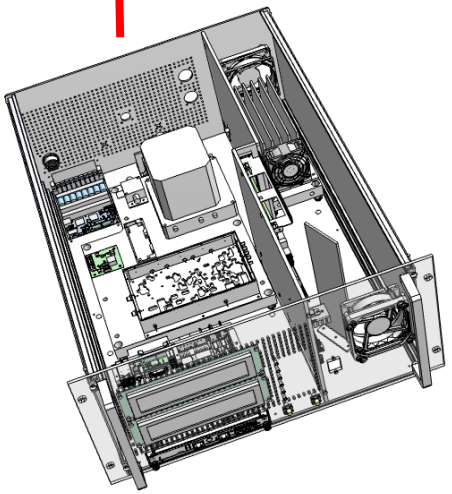
H3 Extension Subdistribution

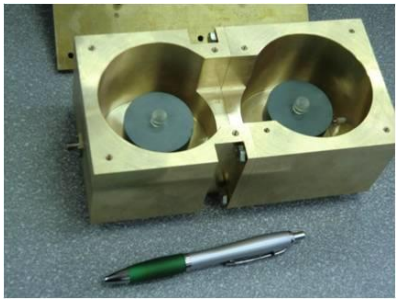
Team work of DESY and ISE engineers. Many subcomponents of the system were developed in Warsaw

XFEL Master Oscillator

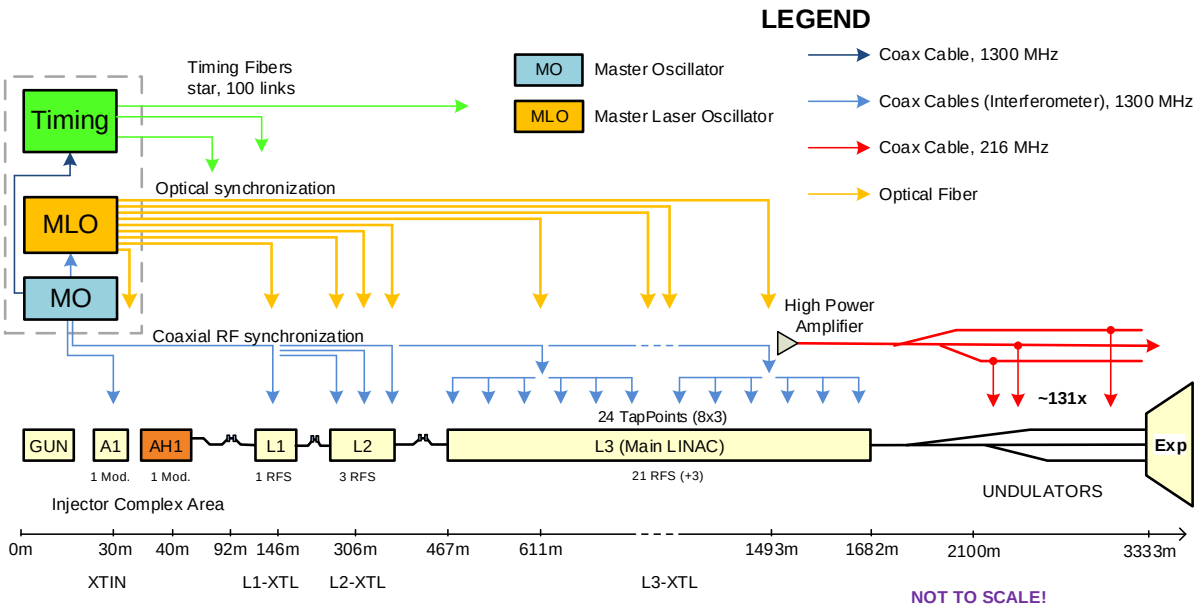


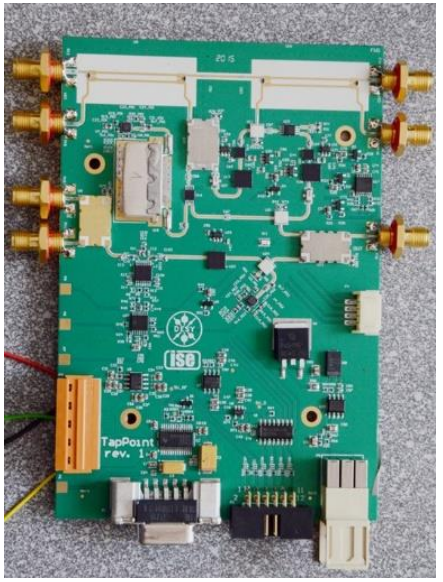




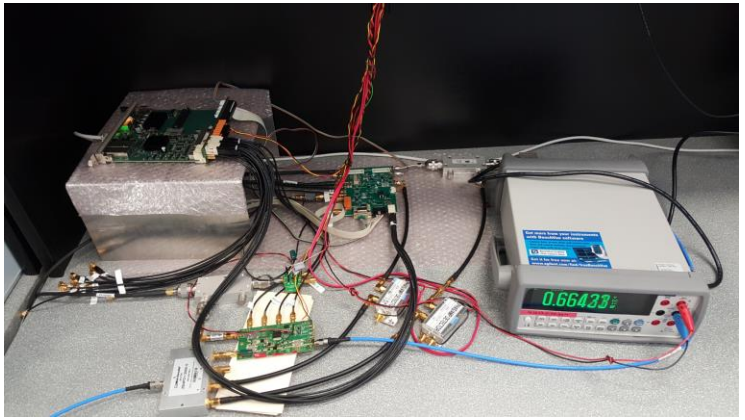


XFEL RF Phase Reference System





- **Three complementary systems (compromise between performance and cost):**
  - Optical synchronization: sub-10fs (jitter, drift) performance, 12 links
  - RF Coaxial distribution: sub-100fs (jitter) and sub-1ps (drift) performance, interferometers, local distribution (44 links, ~260 reference outputs)
  - Timing system



Polish Contributions to ESS

Delivery of LLRF System for 704 MHz

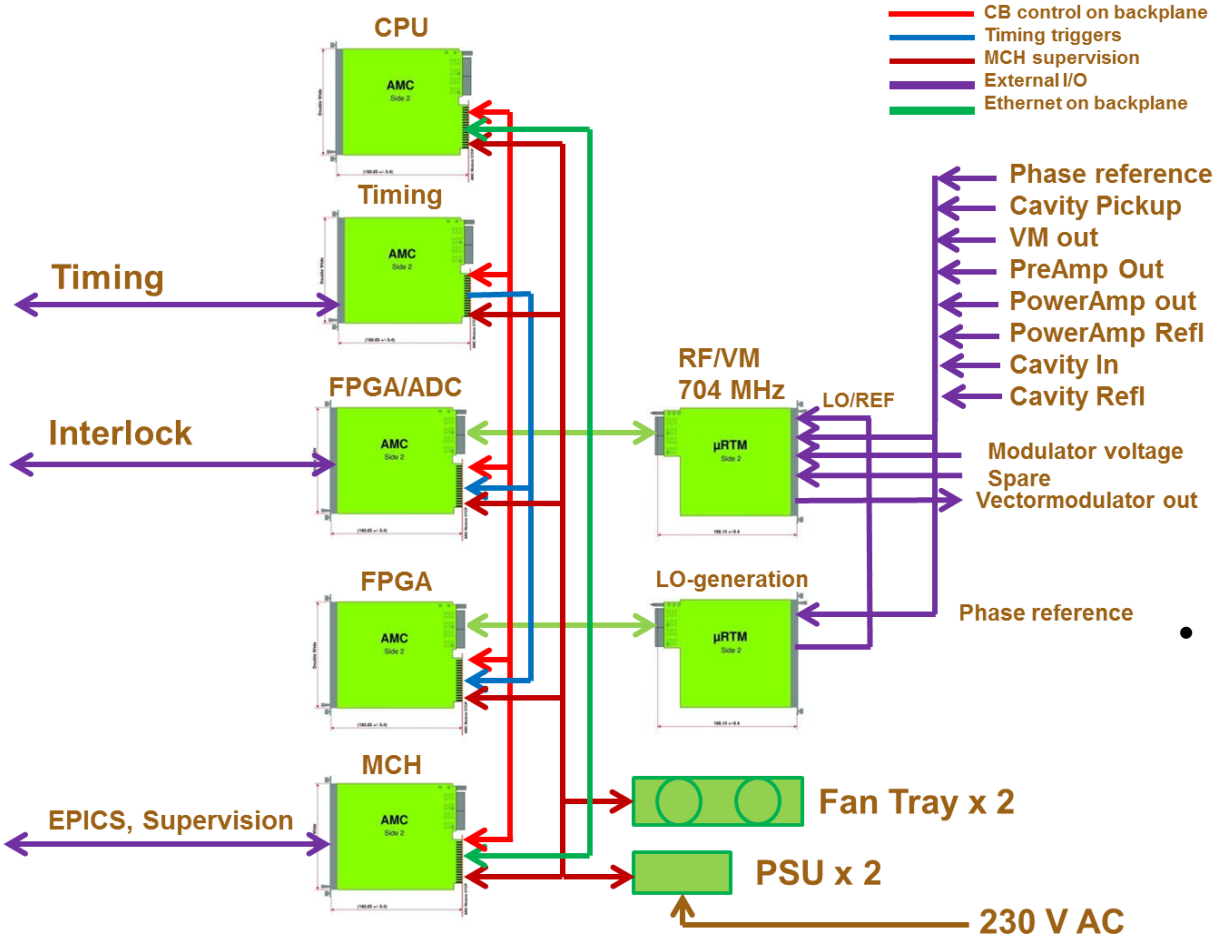
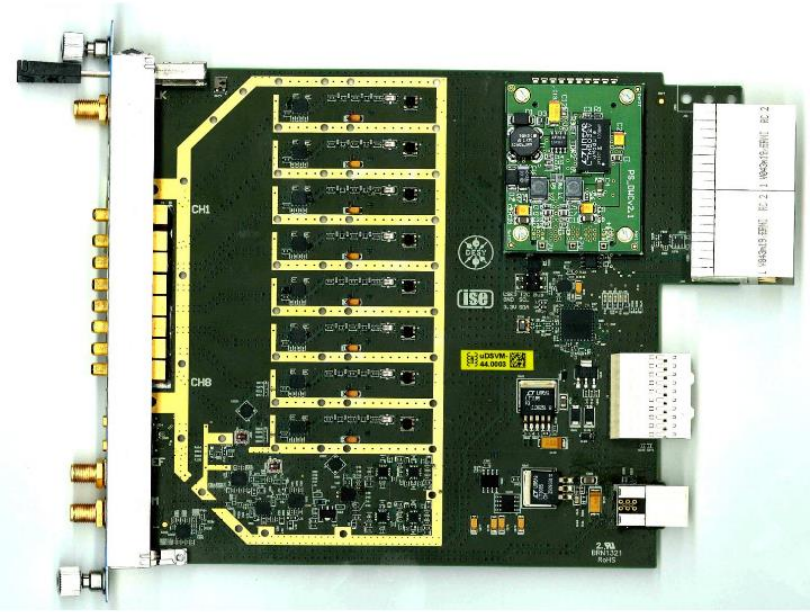


Figure: courtesy A. J. Johansson

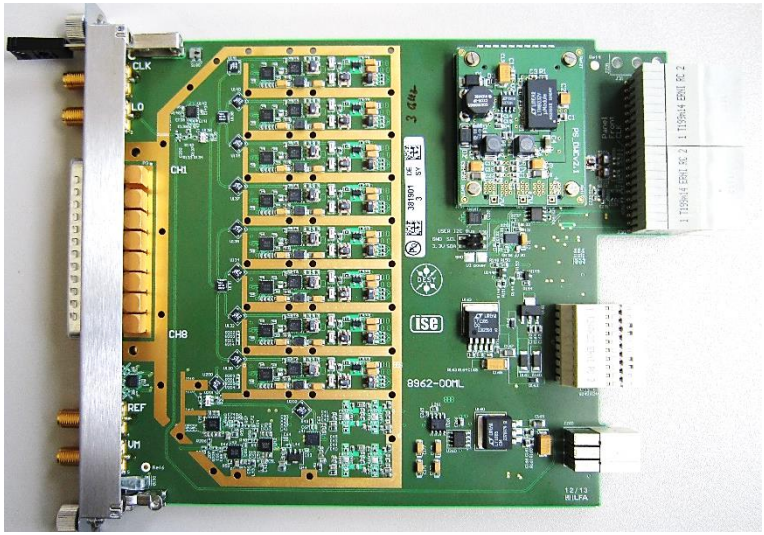
- PEG will develop:
  - Piezo Tuner hardware (RTM)
  - Low cost AMC FPGA board: carrier for LO and Piezo
  - LO-generation RTM
- PEG will assembly, deliver and test 704 MHz LLRF systems
- **The same LO RTM is planned for BPM**

Boards for ESS LLRF

- DS8VM1 card (5 -~700MHz)
- 8 channel analog front end for SIS83xx board
- 1 Vector Modulator output
- MTCA.4 RTM
- Designed with DESY
- Was considered by ESS LLRF



- DWC8VM1 card (700MHz – 4GHz)
- 8 channel downconverter for SIS83xx board
- 1 Vector Modulator output
- MTCA.4 RTM
- Designed with DESY
- Will be used for ESS LLRF

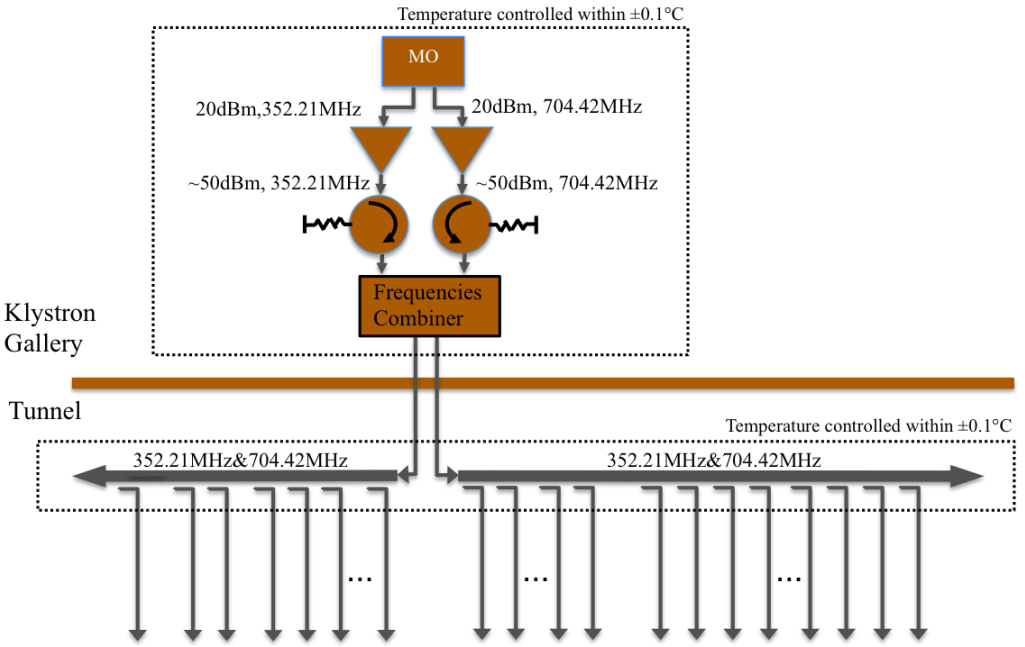


Phase Reference Distribution System

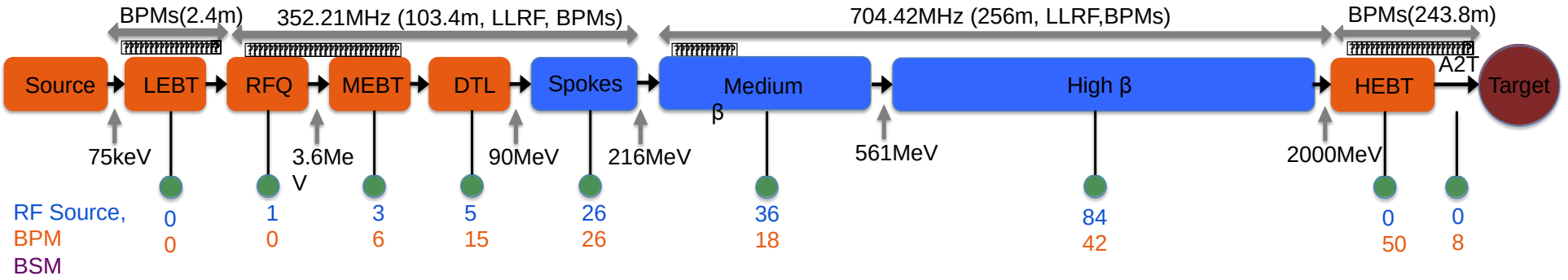
WUT will prototype and build the ESS RF Phase Reference System

ESS Requirements (by Rihua Zeng):

- For LLRF, BPMs, along the tunel, 352 MHz and 704 MHz
- Stability requirement 0.1° for short term(during pulse), 1° for long term (hours to days)
- There shall be 40 along 352.21MHz section and 21 taps along 704.42MHz section.



Figures: one of considered scenarios, courtesy R. Zeng

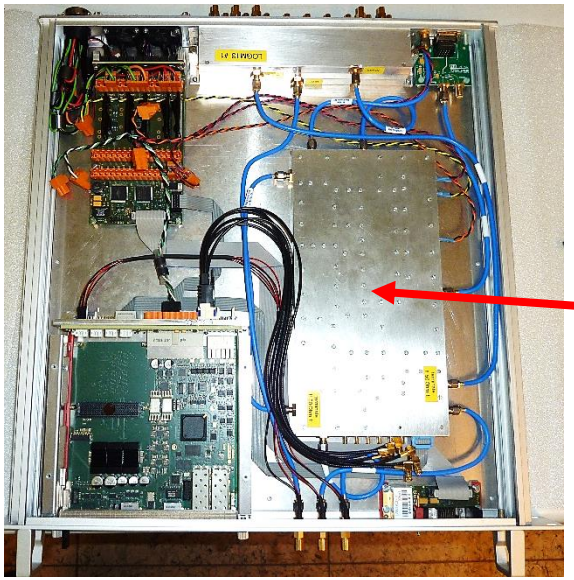


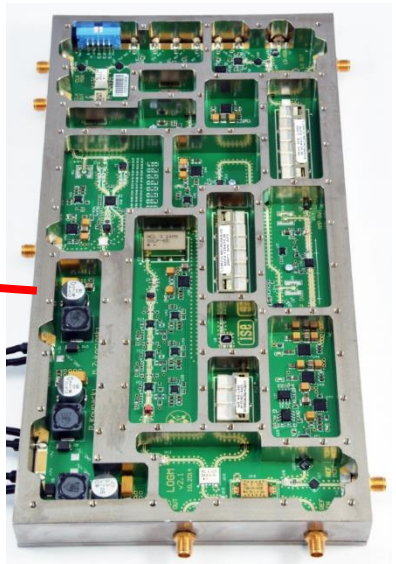
LO Generation

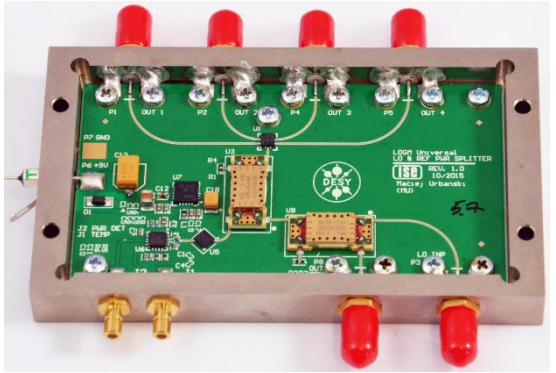
Specification (still not fixed):

- The module should be compliant with MTCA.4 RTM card specification
- 8 LO outputs, +14 dBm
- LO freq. configurable ~20 to 40 MHz above the REF frequency
- 8 CLK outputs, ~100 MHz
- Reference input: 352.21 MHz or 704.42 MHz
- Max jitter 100 fs rms
- Remote configuration and health monitoring

High-performance LO modules developed with DESY







Other Possible Contributions

- Prototyping, test, verification and series-fabrication of BCM differential driver modules and differential receiver RTMs based on ESS requirements
- Series-fabrication of the ESS-SLAC down-mixer RTM for ESS BPMs
- …

Thank you for your attention!