DEVELOPMENT OF A LONG PULSE HIGH POWER KLYSTRON MODULATOR FOR THE ESS LINAC BASED ON THE STACK MULTI-LEVEL TOPOLOGY

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Abstract

A novel Stacked Multi-Level (SML) modulator topology optimized for long pulse and high average power applications has been developed at ESS. It utilizes six identical modules connected in series at the HV output side and fed in parallel from the low voltage side. Each one is formed by one HF inverter, one step-up transformer, one HV rectifier bridge and one HV passive filter. They are supplied, in groups of two, from three capacitor banks which in turn will be charged from the low voltage electrical grid by using three groups of active AC/DC and DC/DC converters. Industrial standard power electronic components are used at the primary stage, which are placed in conventional electrical cabinets. Only few special components (transformers, rectifiers, filters) are required to be placed in an oil tank. A technology demonstrator rated for 115kV/20A and 3.5ms/14Hz is at the final phase of construction. The main power conversion circuit and regulation principles will be described and details on the design and construction of the main subsystems will be given. Simulation and experimental results will be given showing the achieved performance in terms of HV pulse quality and AC grid power quality.

INTRODUCTION

The European Spallation Source (Lund, Sweden) is an under-construction multi-disciplinary research facility to be based around a Linear Particle Accelerator which is to provide 2.86 ms long proton pulses at 2 GeV at pulse repetition rate 14 Hz, representing an average beam power of 5 MW, Fig. 1, below [1].

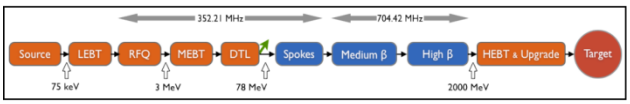

Figure 1: ESS linear accelerator.

The Linac will require, amongst others, the following High Power RF amplifiers:

- 1 Klystron for the RFQ;
- 5 Klystrons for the DTL tanks;
- 36 Klystrons for the Medium Beta;
- 84 Klystrons or IOT's for the High Beta

Since the Linac is a pulsed machine with 2.86ms beam pulse length and a pulse repetition rate of 14Hz, all the klystron modulators will also be pulsed.
The RFQ klystron and the DTL tank #1 klystrons will be both powered in parallel by one dedicated modulator. A second and third modulator will power, respectively, klystrons of DTL tank #2 and of tank #3 (in parallel) and klystrons of DTL tank #3 and tank #4 also in parallel.
The modulators for the Medium Beta will power 4 klystrons in parallel, Fig. 2. Therefore, a total number of 9 modulators will be required for this section of the machine. All modulators are expected to be identical in ratings, topology and interfaces.

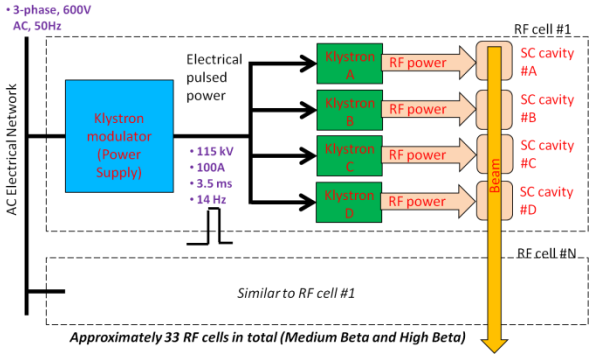

Figure 2: Power configuration of klystrons by their modulators in the High Beta section

For the High Beta section both klystrons and IOT's are considered and a decision is expected to be taken later in 2017. In case klystrons would be adopted, the modulators and powering scheme would be exactly as in the Medium Beta and therefore 21 additional modulators would be required. In the case of IOT's choice, new modulators compatible with IOT requirements will have to be developed and produced. Still, each IOT modulator will power 4 IOT's in parallel.

CONCEPTS & KEY POINTS

Conventional long pulse modulators are pulse transformer based and commonly exhibit poor efficiency, low power density, large footprint and cost [2]. In addition, these topologies due to their nature in combination with the above cited high peak power requirement for short periods of time commonly produce prohibitive levels of flicker and harmonic content while operating at suboptimal power factor, problems usually corrected by both costly and spacious external grid compensators.
A novel stacked multi-level modulator topology optimized for long pulse and high average power applications has been developed at ESS, Fig. 3 [3]. To evaluate the potential of this new topology, a reduced scale prototype rated for 115 kV, 20 A and 3.5 ms/14 Hz was designed and implemented. The prototype, now in operation, is capable of delivering long (3.5 ms) high quality dc-pulses (0-99% rise time of less than 100 µs and flat top ripple

less than that of 0.15%) of high voltage (115 kV) and high power (peak power > 2 MW) while on its own maintaining excellent AC grid power quality (low flicker operation < 0.2%, sinusoidal current absorption with total harmonic distortion < 3%, and unitary power factor).

TOPOLOGY AND PRINCIPLE

To reach the above stated requirements, the klystron modulator requires four power electronic conversion stages, and is divided in two parts, Fig. 3.

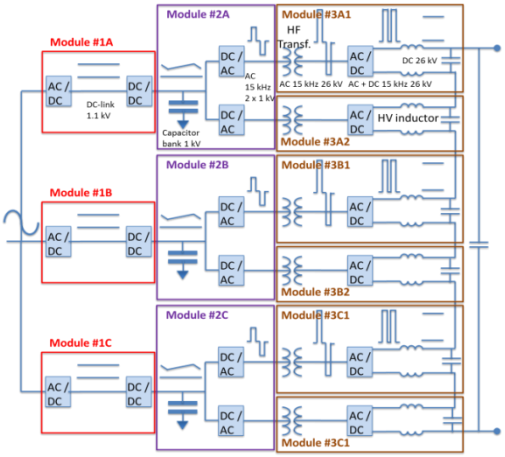

Figure 3: SML modulator topology.

The system front end connects to the AC grid and charges the capacitor banks storing the energy needed in pulsing while ensuring input side requirements are met. This is accomplished in two power electronic conversion stages, as follows. The first conversion stage is an active rectifier (i.e. AC/DC converter) which, knowing input grid voltage and system load, outputs on the AC side three properly selected SPWM voltages, effectively creating a stable dc-link voltage while shaping line currents to be sinusoidal and in phase with the line voltage, effectively reducing line current harmonics and reactive power to a minimum, Fig. 4, below.

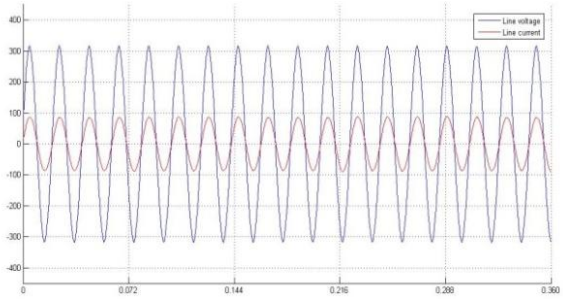

Figure 4: Input line voltage and current (for one phase)

The second conversion stage is a step down (i.e. DC/DC) converter charging the capacitor banks. The motivation for this second stage may be understood from the following reasoning. In pulsing, energy is taken from the capacitor banks, reducing the available voltage. Clearly, this voltage should be replenished before the next pulse is due. With the knowledge of the capacitor bank voltage, it is clear that through the use of this second conversion stage, the charging current may be controlled to exhibit inverse behavior with respect to the capacitor bank voltage, Fig. 5, below, yielding constant charging power, the level of which is set such that the energy is replenished just in time for the next pulse. Hence, despite sourcing high (both pulse and average) power loads, flicker-free modulator operation is attained.

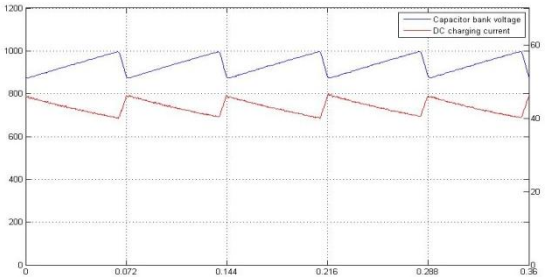

Figure 5: Capacitor bank voltage and charging current.

In summary, the two first conversion stages effectively charge the capacitor banks while shaping the line current so as to be both sinusoidal and in phase with the line voltage. Furthermore, the input power is controlled to be constant, yielding flicker-free operation. The topology utilizes three such systems operating in parallel, charging three independent capacitor banks each feeding two high voltage modules (described below), significantly increasing the power capability of the topology. It should be noted that this first part of the system contains only standard industrial low voltage power electronic equipment, all placed in conventional electrical cabinets, Fig. 6.

Figure 6: View of low voltage converter stage cabinets.

Following the capacitor bank, a DC/AC power electronic converter synthesizes a 1 kV AC square wave fed to a high voltage module consisting of a high frequency transformer stepping up the voltage to 25 kV, a passive AC/DC converter rectifying the voltage, and a passive filter, producing a smooth DC output voltage, Fig. 7. As was previously mentioned, each capacitor bank feeds two such modules, i.e. the entire system encompasses six high voltage modules, on the output interconnected in series, producing a 115 kV pulse, Fig. 8. This voltage is again,

using passive components, filtered before being sent to the load.

Figure 7: Open view of high voltage module

It is again noted that the high voltage assembly is comprised only by passive components, facilitating diagnostics and maintenance.

Figure 8: Open view of high voltage oil tank assembly

EXPERIMENTAL RESULTS

Below, Fig. 9, the complete interconnected system from AC grid to high voltage output connected to a high voltage resistive dummy load with the same electrical characteristics as the final load is shown.

Figure 9: Complete modulator prototype and test setup.

With this setup, as shown in Fig. 10, high voltage dc pulses up to 100 kV have been generated continuously. It is stressed that these measurements were obtained simultaneously to those shown in Fig. 4 and Fig. 5, i.e. while attaining sinusoidal line current, unitary power factor, and flicker-free operation.

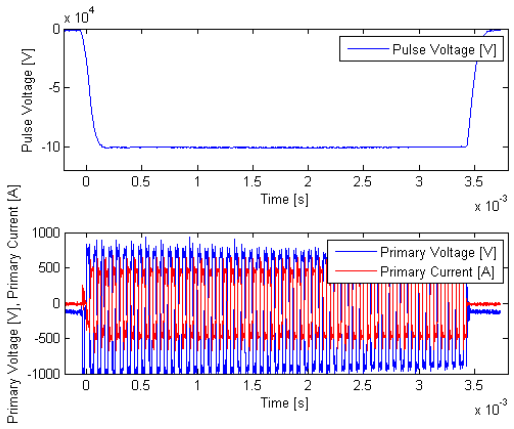

Figure 10: HV output pulse and primary side quantities.

CONCLUSIONS

The new SML topology has been proven experimentaly as an alternative to conventional topologies for long pulse klystron modulators. The topology is modular and formed by two main stages:- the low voltage stage uses standard power electronic components and fits in standard electrical cabinets; the high voltage stage stands in a oil tank and comprises custom design sub-systems (HV transformers, rectifier bridges, LC filters, etc.) althout all of them based on standard components assembly.

Experimental results have been obtanied with a reduced scale prototype rated for 1/5th of the full current capability althoug all other parameters are identical to the full scale units. The output pulse reached so far has an amplitude of 100kV, a current amplitude of 18A, a pulse width of 3.5ms, a repetition rate of 14Hz and a rise-time of 150µs. The flat-top droop is compensated to better than 1%. The HF ripple could not been measured accurately yet but it is unperceptible when observed with the current measurement system (HV compensated divider and oscilloscope).

Form the grid point of view, it has been demonstrated that the line current is sinusoidal with a THD below 3% and of unitary power factor. The fluctuation of the line current amplitude is below 5% leading to a voltage flicker well below the standard limit of 0.3%.

REFERENCES

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[2]- Carlos A. Martins, *"Solid State Klystron Modulators for Long Pulse (>100µs) Linac's:- Topologies and Design Issues"*, 3rdOpen Collaboration Meeting on Superconducting Linacs for High Power Proton Beams (SLHiPP-3), 17th-18th April 2013, Louvain-La-Neuve, Belgium;

[3]- Carlos A. Martins, *"The SML long pulse klystron modulator concept"*, 5th Open Collaboration Meeting on Superconducting Linacs for High Power Proton Beams (SLHiPP-5), 18th-19th March 2015, Lund, Sweden