

# ICS Update

@ 3rd ESS Beam Diagnostics Forum

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[www.europeanspallationsource.se](http://www.europeanspallationsource.se)

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- MicroTCA overview;
- MicroTCA infrastructure:
  - MTCA crates;
  - MTCA Carrier Hub;
  - Power Modules;
- Advanced Mezzanine Cards:
  - MRF Event Receiver;
  - CPU cards;
  - IOxOS IFC1410/IFC1420;
- Software Stacks / Showcase

## Glossary:

- **MicroTCA** : Micro Telecommunication Computing Architecture
- **MCH** : MicroTCA Carrier Hub
  - manages the other boards, provides interconnection switch capabilities, clock distribution, etc
- **PM** : Power Module
- **CU** : Cooling Unit
- **AMC** : Advanced Mezzanine Card
  - basic constituent of the MTCA system, can provide support for a RTM
- **RTM** : Rear Transition Module
  - provides real estate area for additional electronics
- **MMC** : Module Management Controller
  - monitors the status of the AMC
- **MCMC** : MicroTCA Carrier Management Controller;

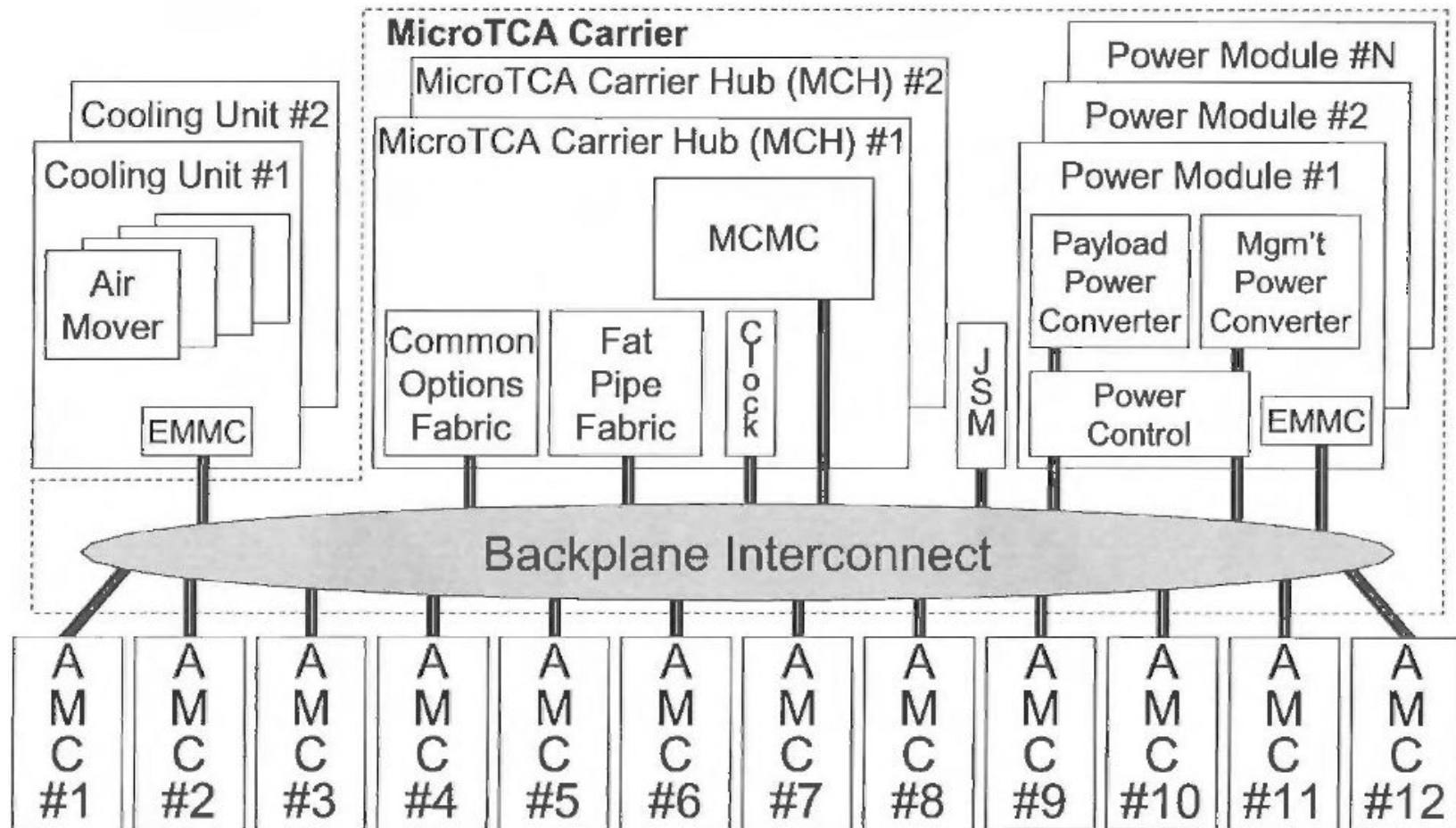
## Why MicroTCA ?

*“MicroTCA is a modular standard.*

*By configuring highly diverse collections of AdvancedMCs in a MicroTCA Shelf, many different application architectures can be easily realized.*

*The common elements defined by MicroTCA are capable of interconnecting these AdvancedMCs in many interesting ways—powering and managing them, all at high efficiency and low cost.”*

# MicroTCA Infrastructure



# MicroTCA Chassis (1)



Need to support 2 different chassis types:

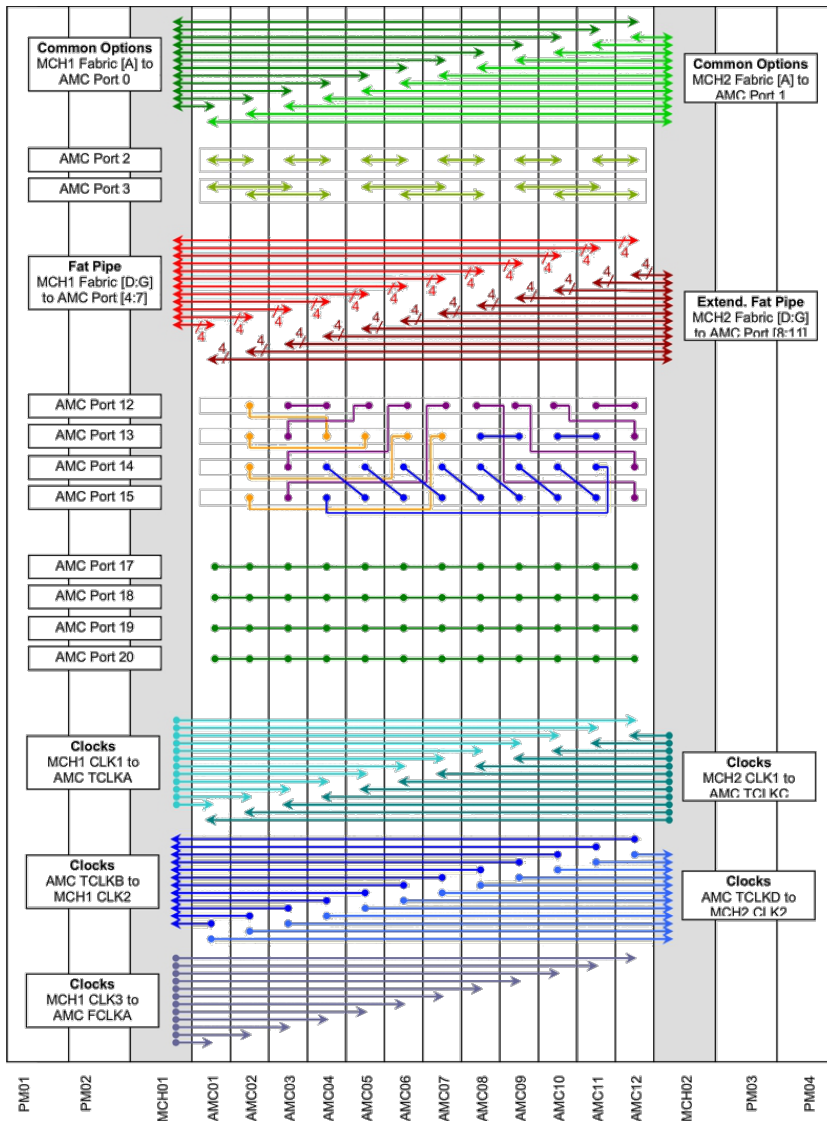
- 12 slots 9U for systems requiring more than 6 AMC(s) and/or more than 4 RTM(s);
- 6 slots 3U to reduce the number of racks deployed.

Front to rear cooling scheme

Tradeoffs:

Supported Components	9U	3U
MCH(s)	2	1
PM(s)	4 (3+1)	2
CU(s)	2 (push-pull)	2 (pull only)
AMC(s)	12	6
RTM(s)	12	4

# MicroTCA Chassis (2)



## 9U backplane interconnections:

- 2 GbE links (1 towards each MCH)
- 2 high speed AMC to AMC links (BP specific)
- Redundant PCIe 4x
- 4x LVDS type AMC to AMC links (BP specific)
- 8x MLVDS lanes
- 4x AMC Clock input lines (2 for each MCH)
- 1x FAT Pipe Reference CLK

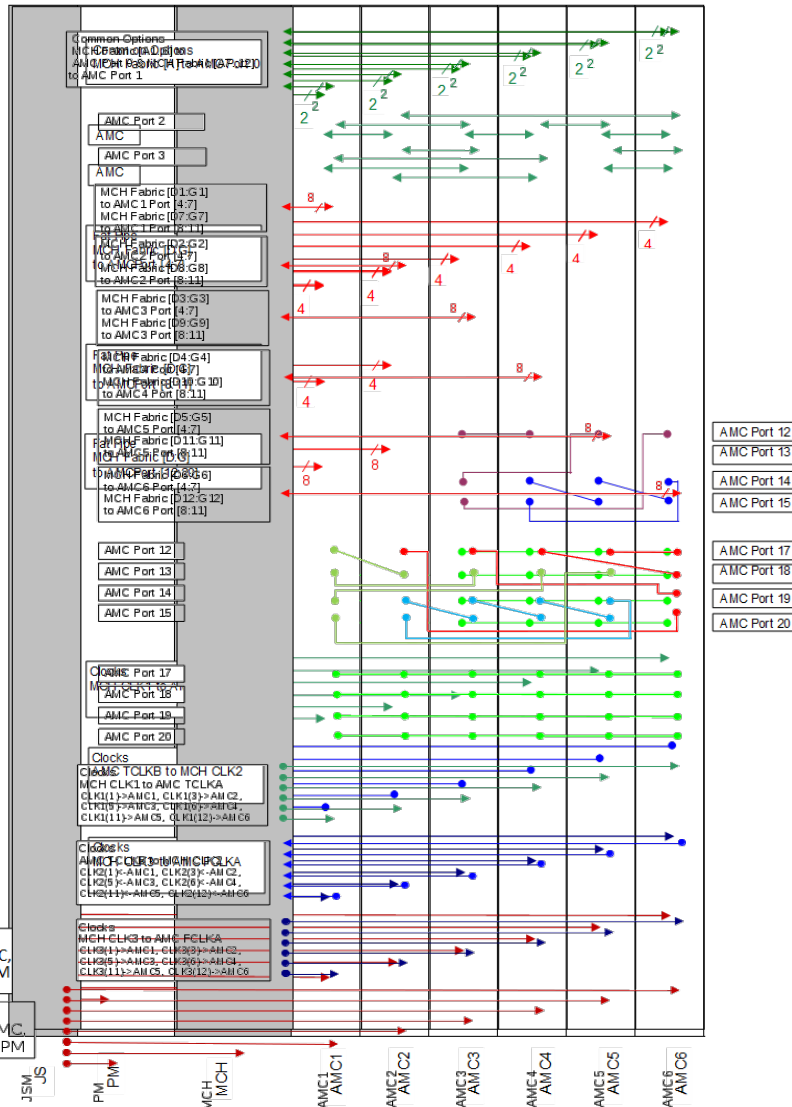
# MicroTCA Chassis (3)

## 3U backplane interconnections:

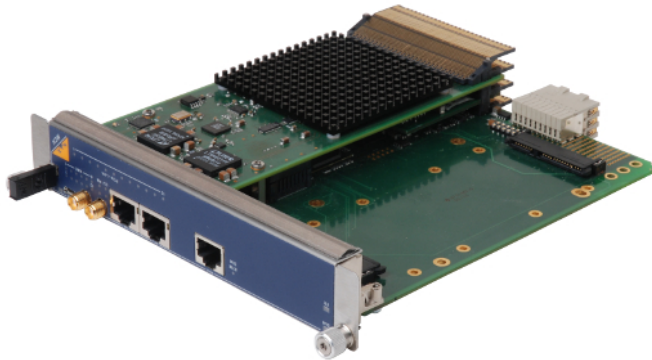
- 2 GbE links
- 2 high speed AMC to AMC links (BP specific)
- PCIe 8x and 4x
- 4x LVDS type AMC to AMC links
- 8x MLVDS lanes
- 2x AMC Clock lines
- 1x FAT Pipe Reference CLK

## New backplane design (available week 26):

- PCIe 8x to all AMCs
- 4x LVDS AMC to AMC provided to all slots
- 8x MLVDS lanes span all AMCs







## MicroTCA Carrier Hub :

N.A.T. , MCMC implementation offers broad compatibility

- PCIe gen.3 48 port switch;
- GbE switch;
- Clock input/output on backplane CLK1 and CLK2 plus front panel SMA;
- IPMI message forwarding on GbE;



## Power Modules:

- Wiener (1KW)
- N.A.T. (600W)

Both will be used. Choice according to:

- Noise requirements;
- Redundancy;



## Timing system based on Micro-Research Finland products:

- clocks from/to TCLKA/TCLKB
- driving/receiving differential triggers AMC RX/TX ports 17 to 20 (MLVDS)
- 24 differential lanes to RTM (no RTM designed yet)
- front panel 4 x TTL outputs, 2 x TTL inputs (to be replaced by UIO modules)
- VHDCI front panel connector for IFB-300 interface box
- Delay compensation and feedback





## Concurrent Technologies AM900:

- Intel i7 x86-64 architecture
- Up to 16GB DDR3 memory
- PCIe upstream

## IOxOS IFC1410/1411:

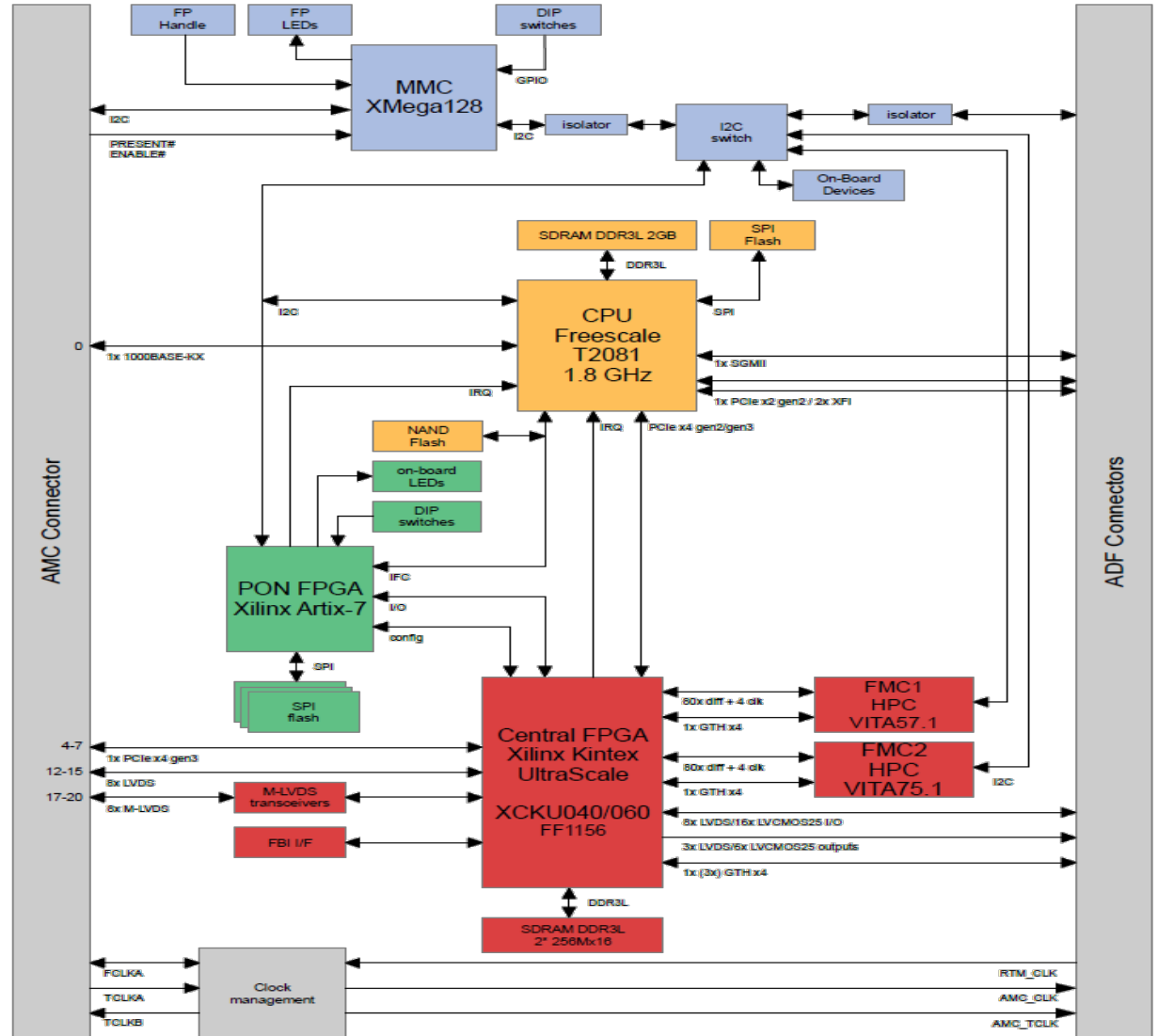
- T208x Freescale PPC architecture
- 2GB DDR3 memory
- PCIe EP (upstream capability under development)
- Xilinx Kintex Ultrascale FPGA
- FMC support (2 HPC IFC1410 / 1 HPC IFC1411)
- ADC onboard (10ch IFC1420 only)
- RTM support (D1.4 IFC1410 / A1.1 IFC1411)



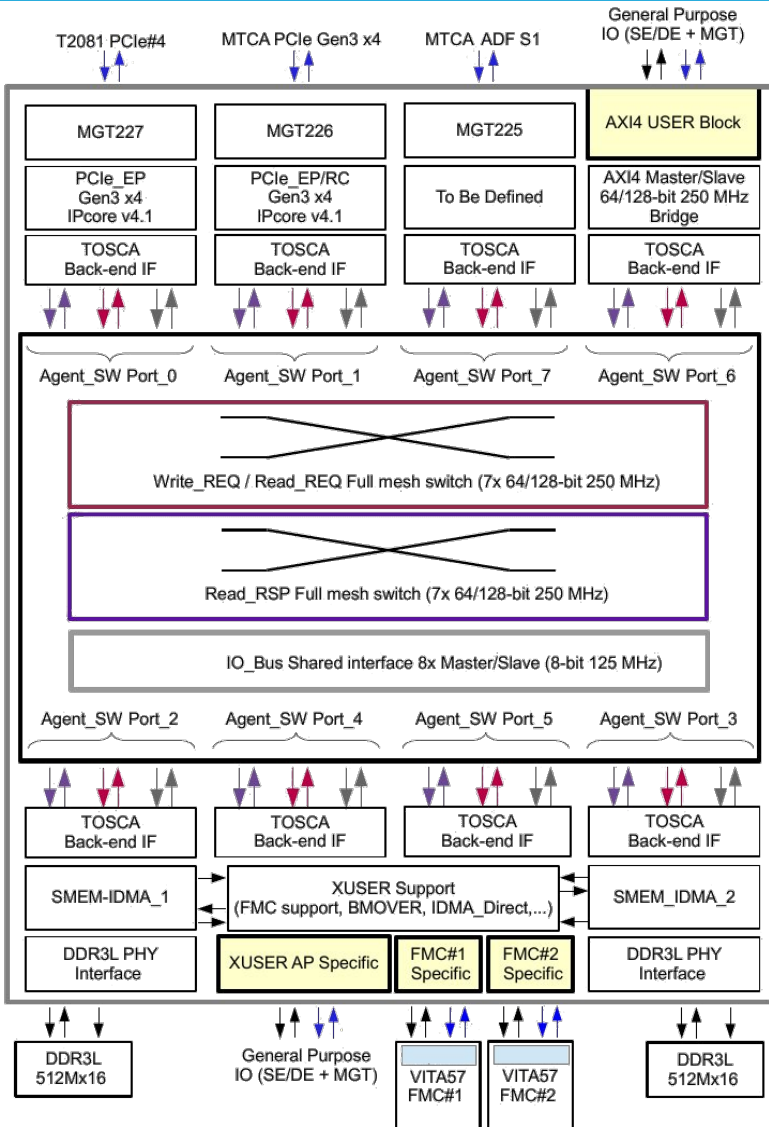
# MicroTCA AMC boards: IFC14xx

## IFC1410 block diagram :

- MMC & sensors section;
- PPC CPU section;
- Configuration management;
- Main FPGA/application specific section;



# MicroTCA AMC boards: IFC14xx



## IFC1410 Firmware infrastructure:

- Separate Data and Control interconnect infrastructure;

### Data:

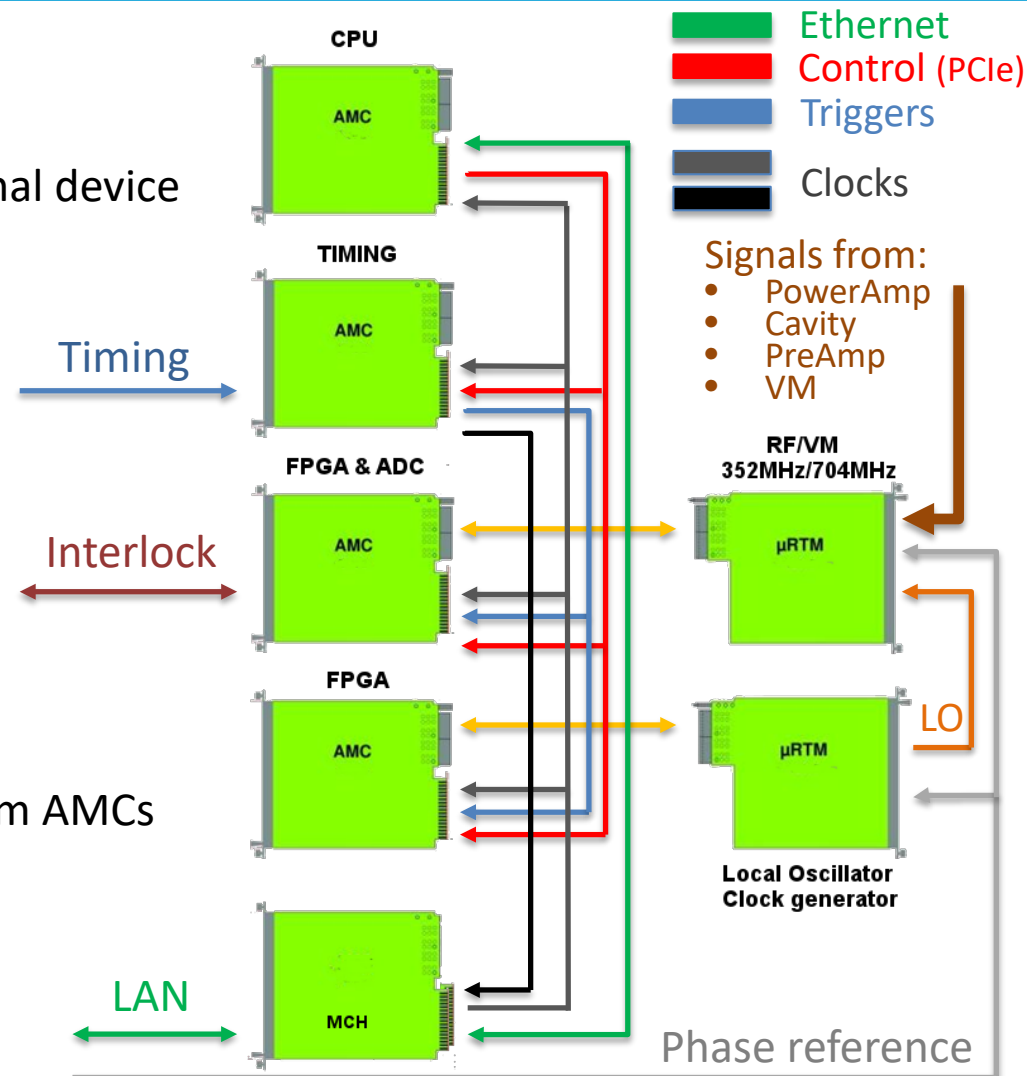
- Full mesh switch;
- Every agent SW has two master and slave interfaces for request and response communications;
- Communication based on PCIe TLPs

### IO Control:

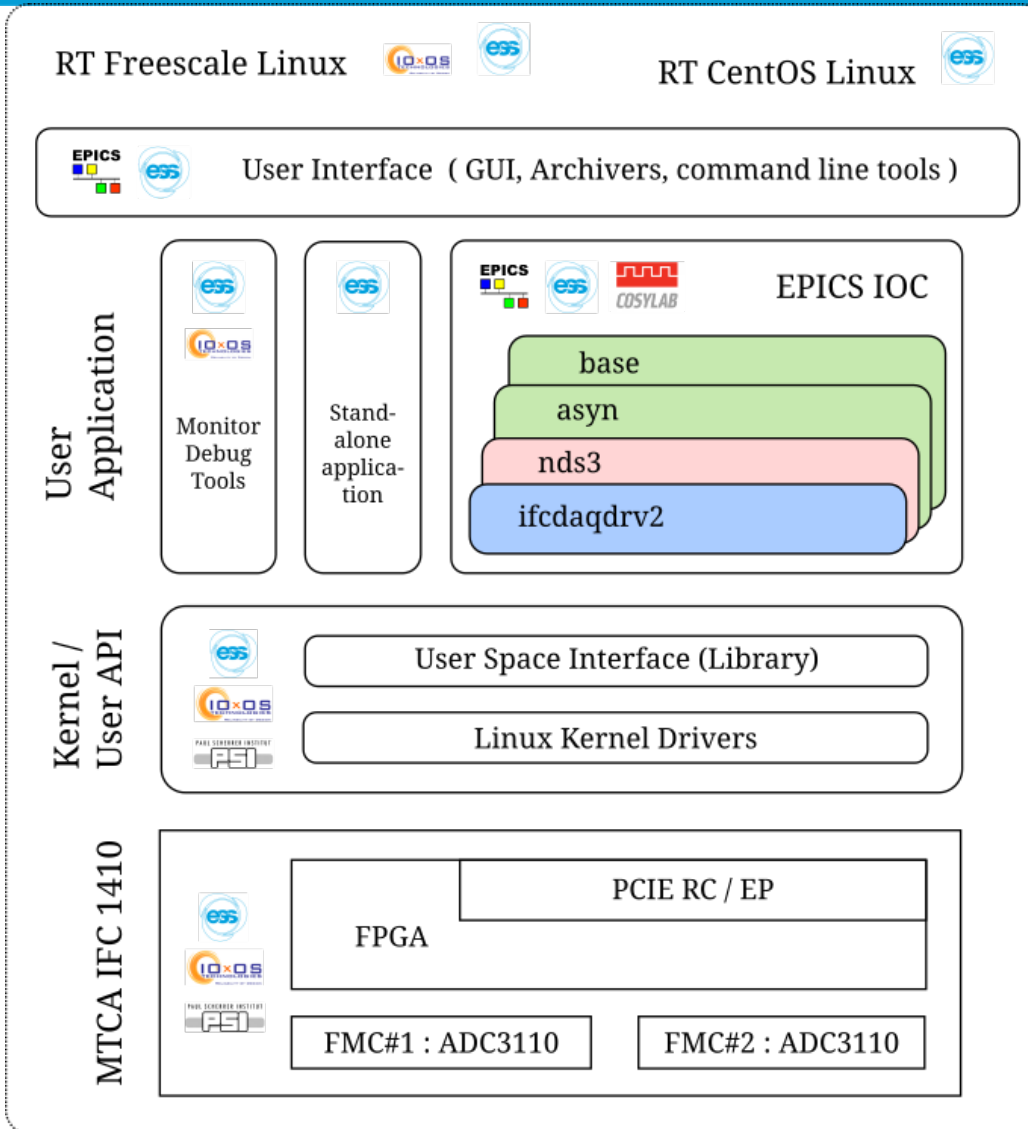
- Shared parallel bus;
- Master and slave interfaces for each agent switch;
- Round Robin arbiter to assign bus mastership

# MicroTCA system example

- **Timing:**  
Gets synchronization info from external device and provides:
  1. clock to MCH
  2. triggers to all AMCs
  3. machine configuration settings
- **MCH:**  
Monitors AMCs status, distributes clocks and provides interconnections
- **CPU:**  
Manages a subset of AMCs
  1. configures and collects data from AMCs
  2. runs EPICS IOCs
- **AMC & RTM:**  
Application specific. May provide interlocks and information to MPS



# MTCA Software Stacks / 2017.04



CentOS Linux 7.3 64bit  
NXP Freescale Linux 64bit

EPICS base 3.15.4  
with ESS patch

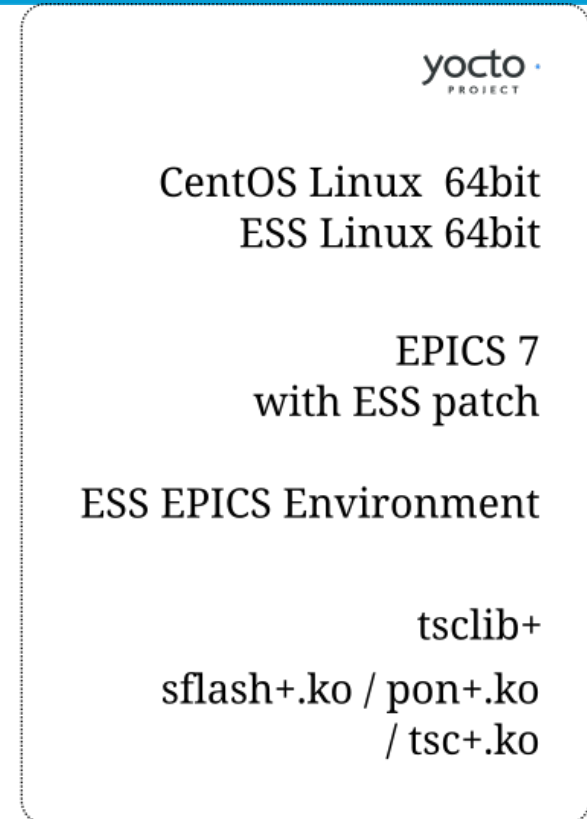
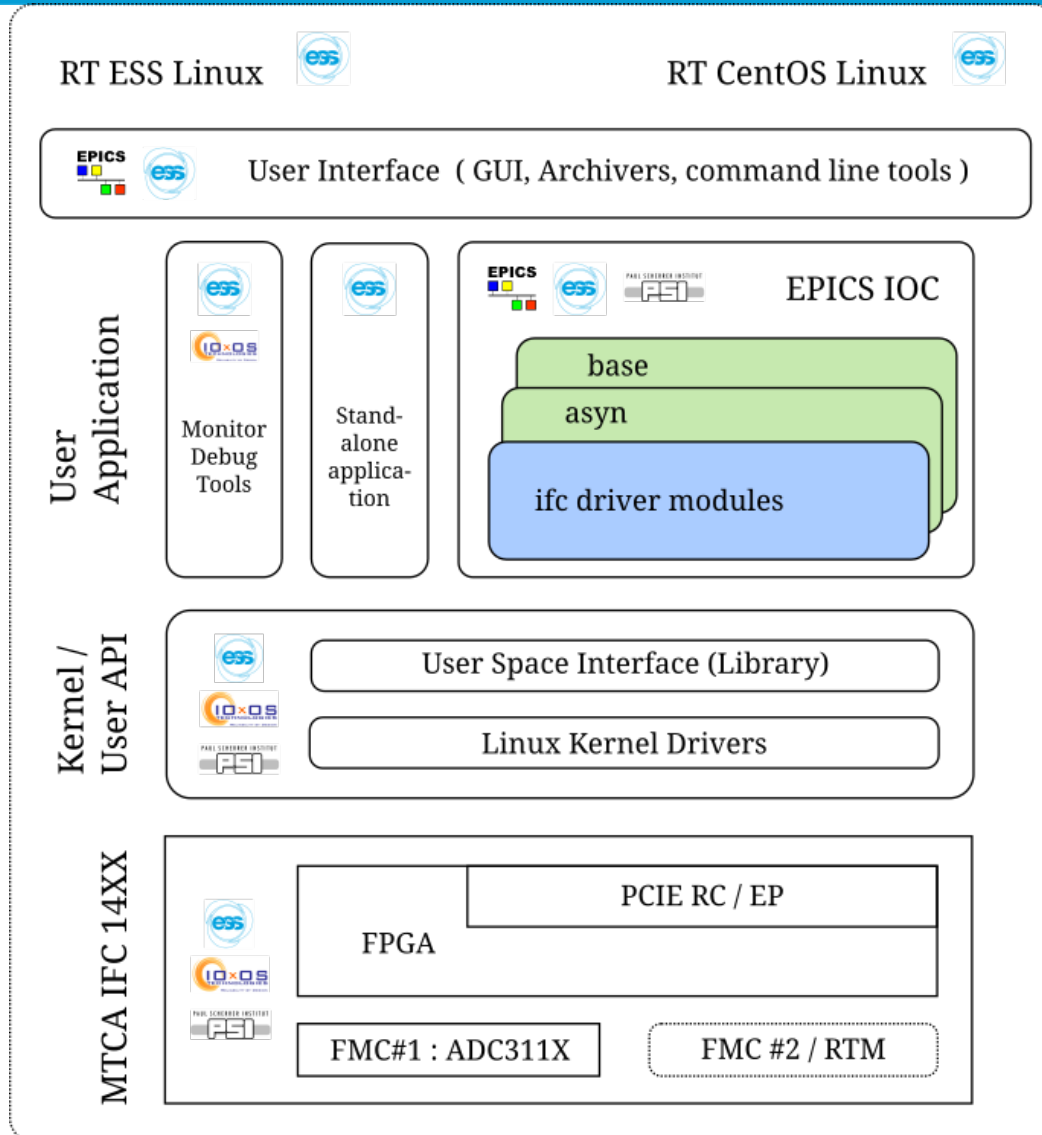
ESS EPICS Environment

tslib  
sflash.ko / pon.ko  
/ tsc.ko

End Point

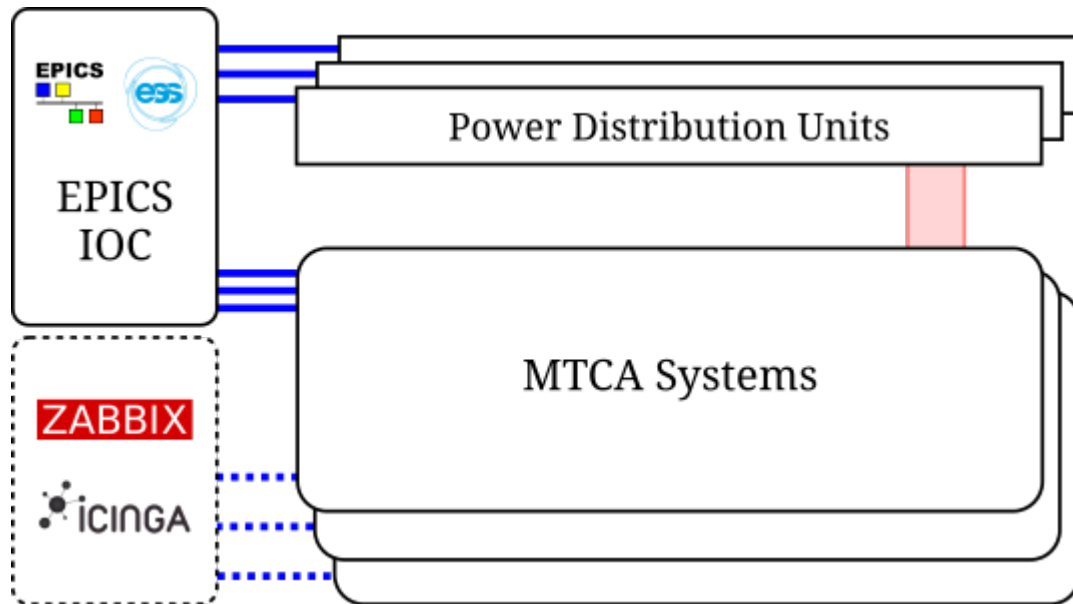
2017.04

# MTCA Software Stacks / Plan





## MTCA Infrastructure Monitoring System



- Slow > 1 Hz
- Read Only (very limited Write)
- Most PDUs support SNMP
- MTCA MCH supports
  - RCMP (IPMI)
  - SNMP
- EPICS modules
  - ipmiComm (SLAC)
  - devSNMP (FRIB)
  - snmpLib (RAON)
- Existent Open Source Tools
  - ZABBIX
  - ICINGA

# MicroTCA system Showcase

