Detector Data Links to DMSC

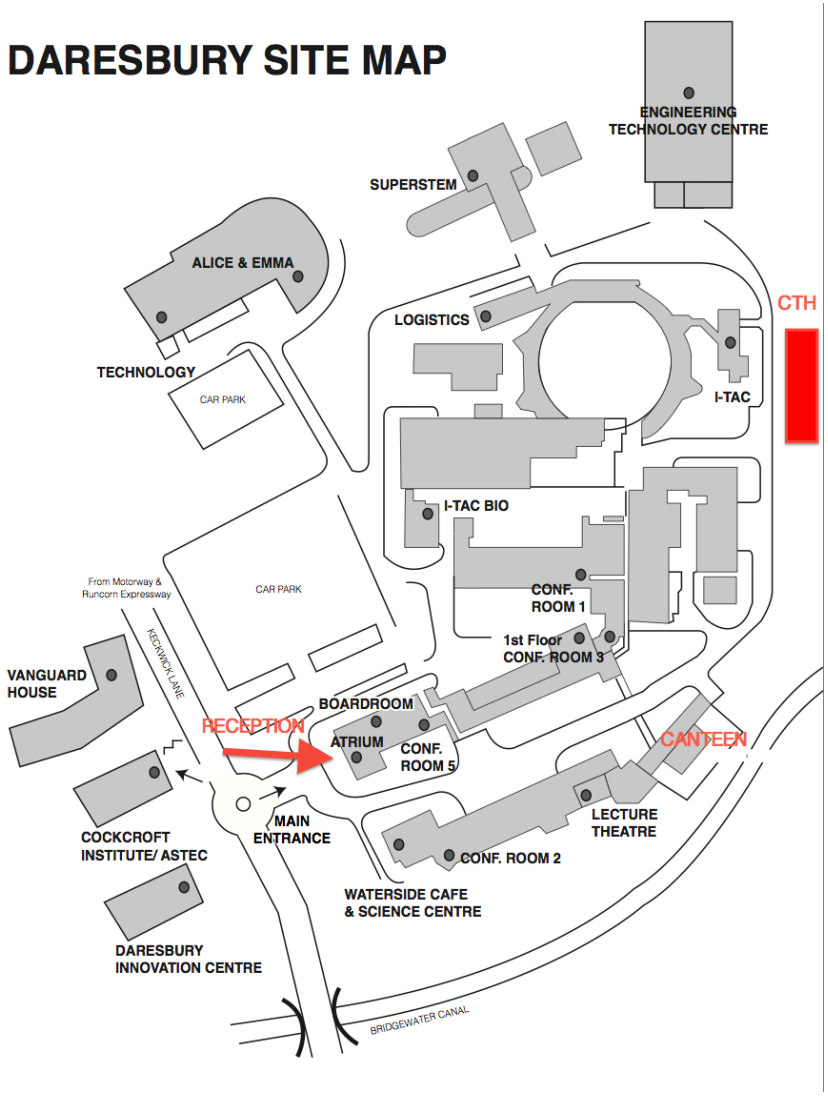
Introduction

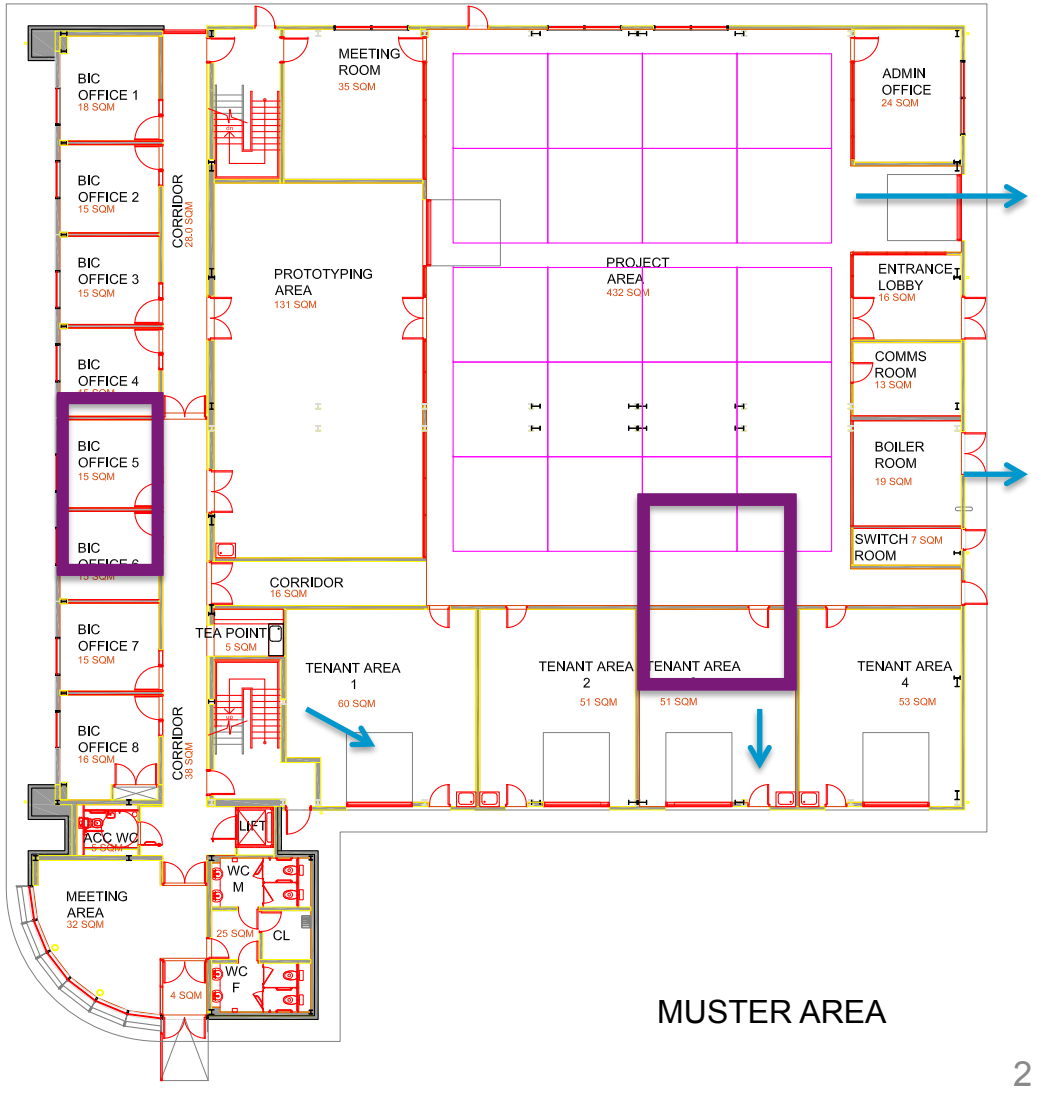
DG-DMSC EF Data Link Meeting
Daresbury 9th May 2017

Background & Safety info Daresbury CTH

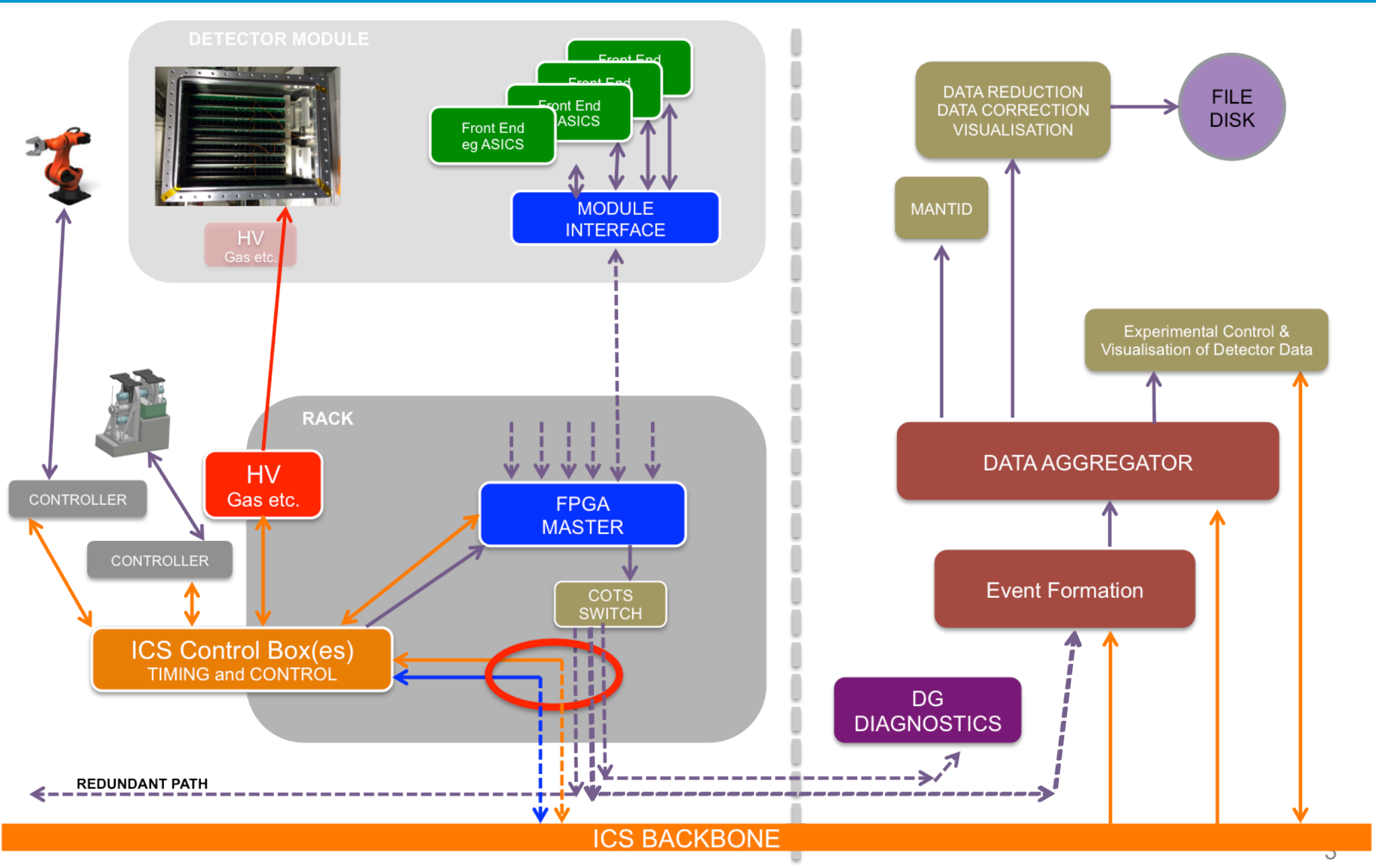
EUROPEAN SPALLATION SOURCE

Daresbury CTH..... *.....a true Island of sanity*

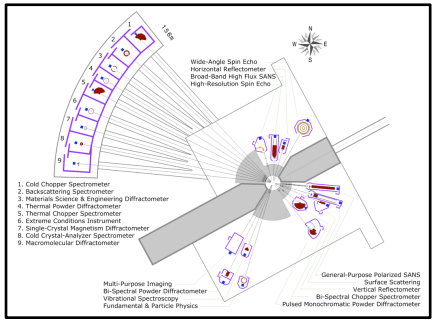




Data Paths in a Typical Detector Installation



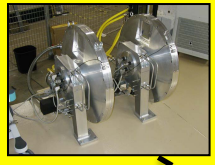
Data Acquisition, Reduction & Control



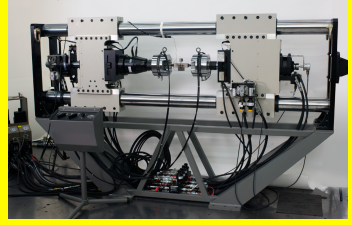
NEUTRON TECHNOLOGIES

Motion Control

Sample Environment



Choppers



Fast Sample Environment

Detectors & Monitors

INTEGRATED CONTROL SYSTEMS

Timing

EPICS

Control Box

Fast Data Readout

DATA MANAGEMENT & SOFTWARE CENTRE

Data Aggregator & Streamer (ADARA)

Instrument Control Room

User Control Interface

Mantid

Live, Local & Remote Data Reduction

Data Analysis Interfaces

Automated Data Reduction

Mantid

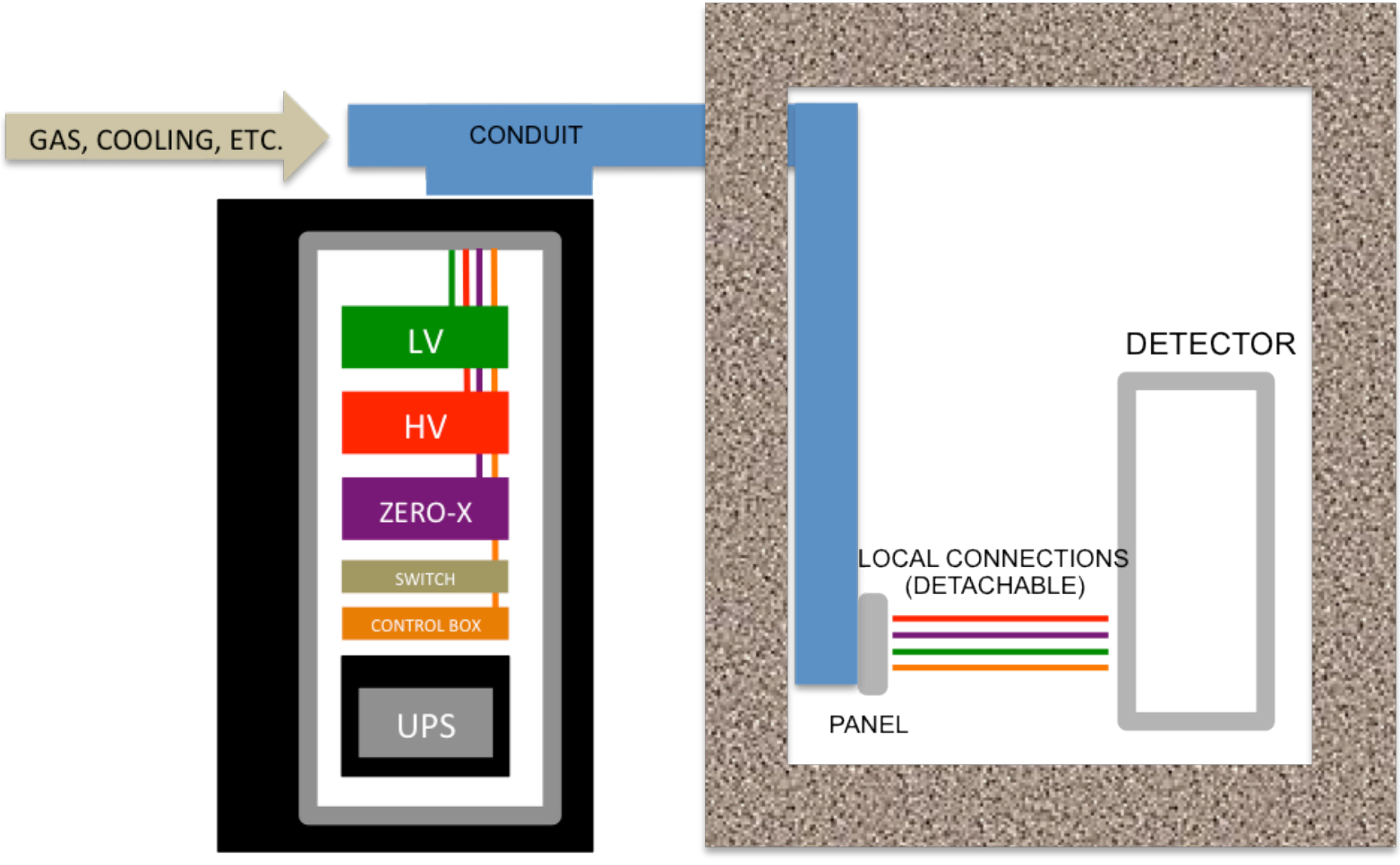
Lund Server Room

Automated Data Reduction

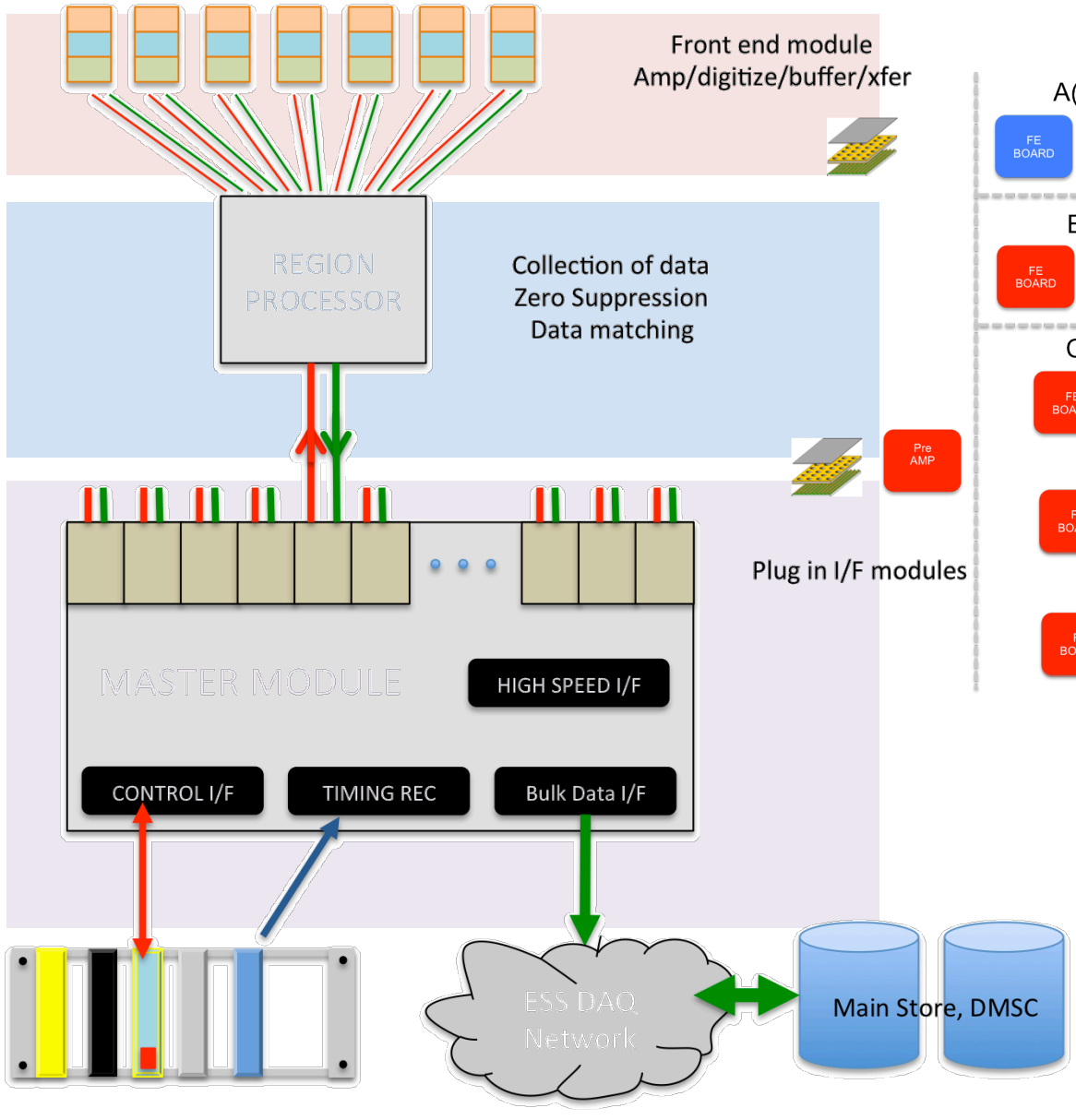
Mantid

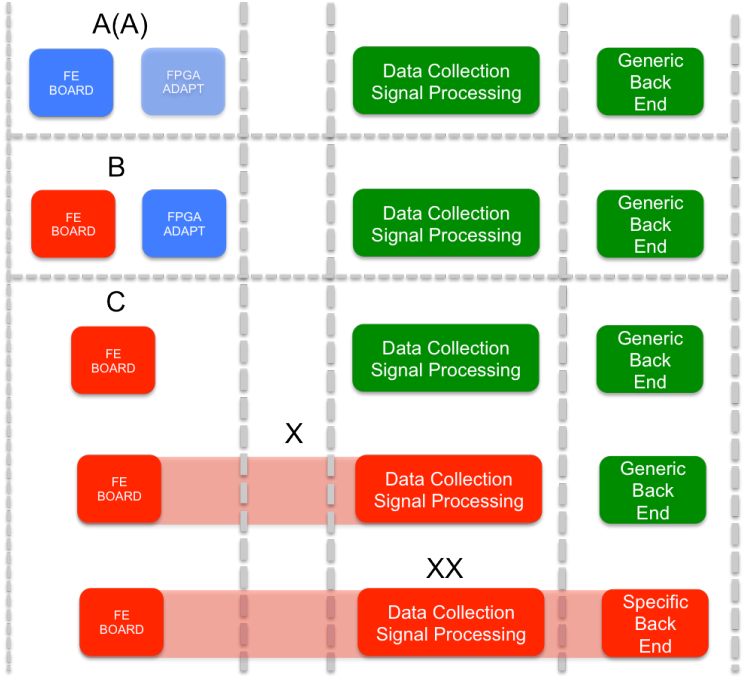
Copenhagen Server Room

Layout of Detector Electronics

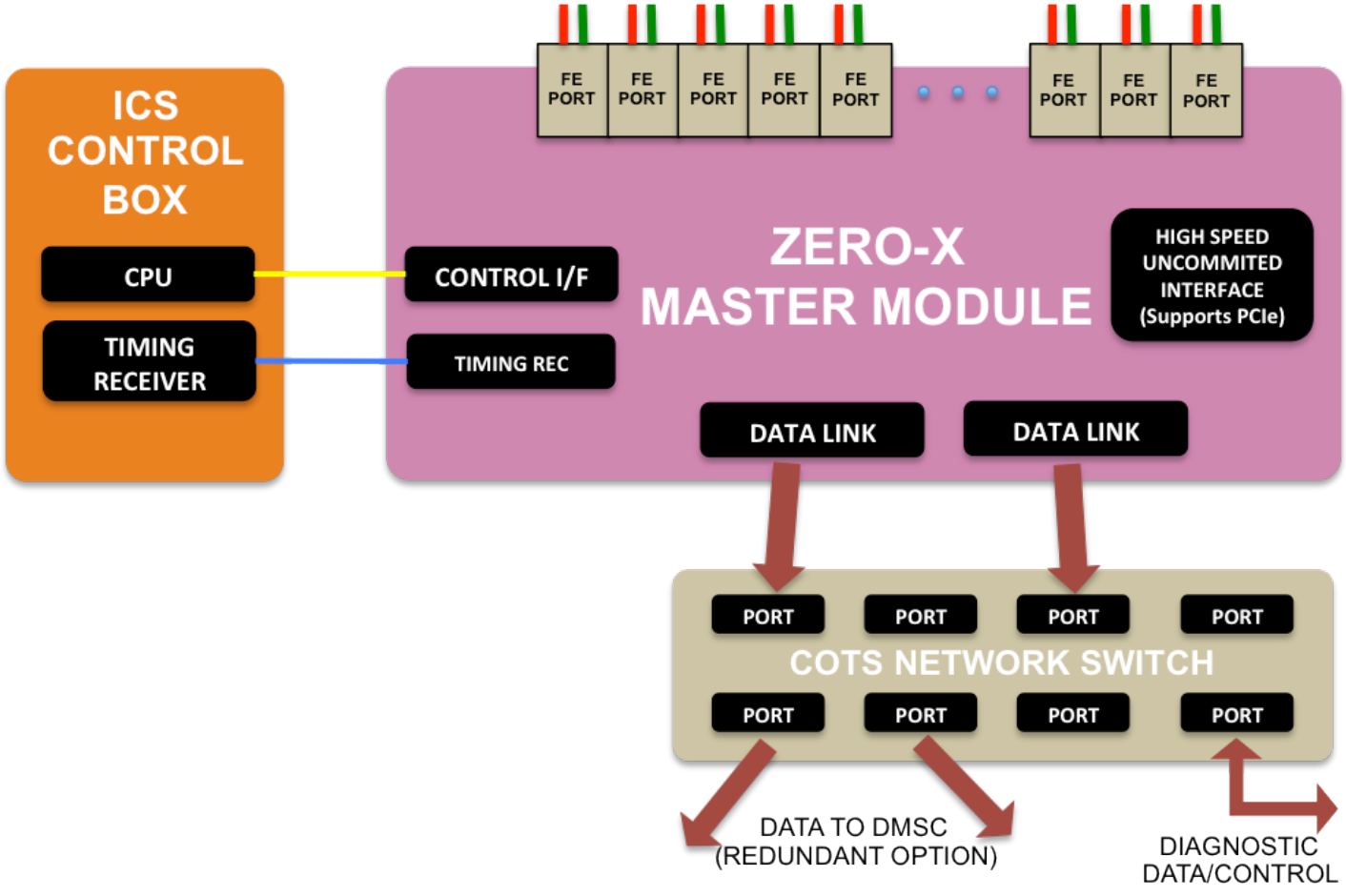


Detector Integration Models





Centralized 'Master' Interface of DG Readout



A word about FPGAs.....

7-Series and UltraScale devices have dedicated error detection and correction circuits.

Development platform ISE-> Vivado.
Only Vivado supported at ESS

Programmable System Integration
- Up to 3.6M system logic cells
- Up to 8GB of HBM Gen2 integrated in-package
- Up to 500Mb of total on-chip integrated memory
- **Integrated 100G Ethernet MAC** with RS-FEC and 150G Interlaken cores
- Integrated blocks for PCI Express® Gen 3x16 and Gen 4x8

Increased System Performance
- 21.2 TeraMACs of DSP compute performance
- 1.6X fabric performance versus Virtex-7
- **Up to 128 transceivers operating at 32.75Gb/s to deliver multi-terabit systems**
- 460GB/s HBM bandwidth, and 2,666Mb/s DDR4 in the mid-speed grade

BOM Cost Reduction
- A 5:1 card reduction for 1Tb OTN transponder
- UltraRAM for on-chip memory integration
- VCXO and fractional PLL integration reduces clocking component cost

Total Power Reduction
- **Up to 60% lower power vs. 7 series FPGAs**
- Voltage scaling options for performance and power
- Tighter logic cell packing reduces dynamic power

Xilinx SEU; Past, Present and Future

			CRAM	BRAM
1998	250 nm	Virtex	160	160
2002	130 nm	Virtex-II Pro	437	770
2012 (Now)	28 nm	7 series Artix and Zynq	87	79
2015 (Now)	20 nm	UltraScale	29(7)	50(7)

Soft Event Rates at sea level New York

Events per million bits per 10^9 hours.
Configuration memory (CRAM) and Block Memory (BRAM) in user design.

Things were definitely getting worse so this *had* to be addressed by design.

Xilinx FPGAs now have a lower susceptibility than they have ever had.

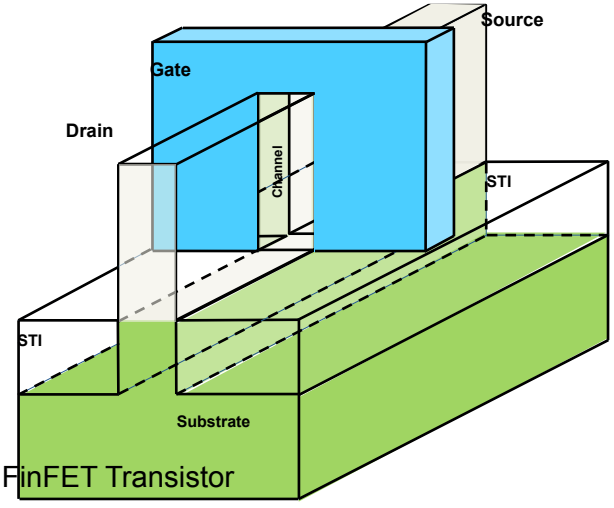
Coming soon…

Tests indicate

<5 FIT/Mb

Advanced 16nm FinFET
5× reduction in sensitive area

Design Rules
40+ Patents & Trade Secrets



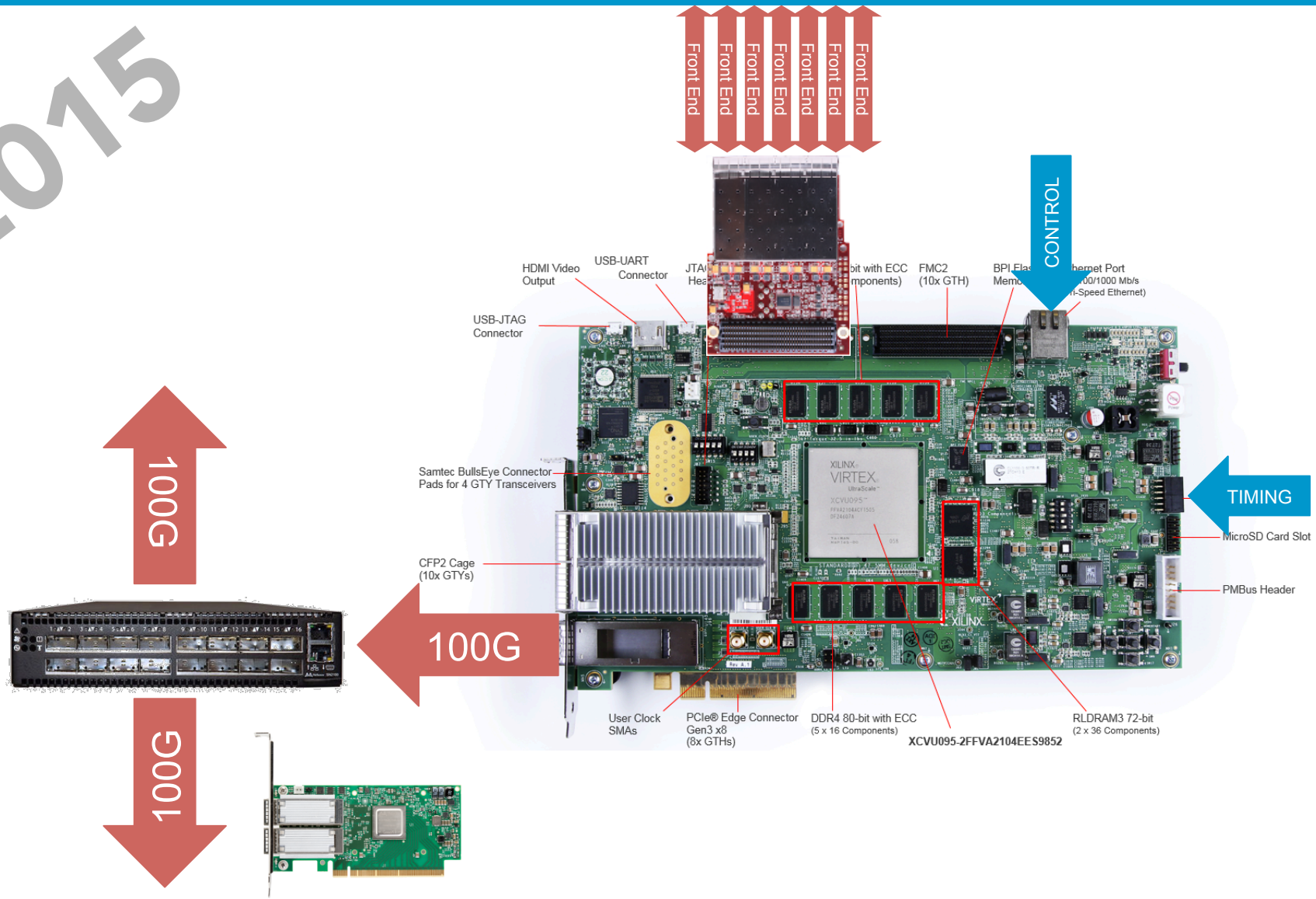
FinFET Transistor

16nm UltraScale+ is on target to be 30 times less susceptible than 7-Series.

Last year's model !!! Ultrascale
Used for test generators

EUROPEAN SPALLATION SOURCE

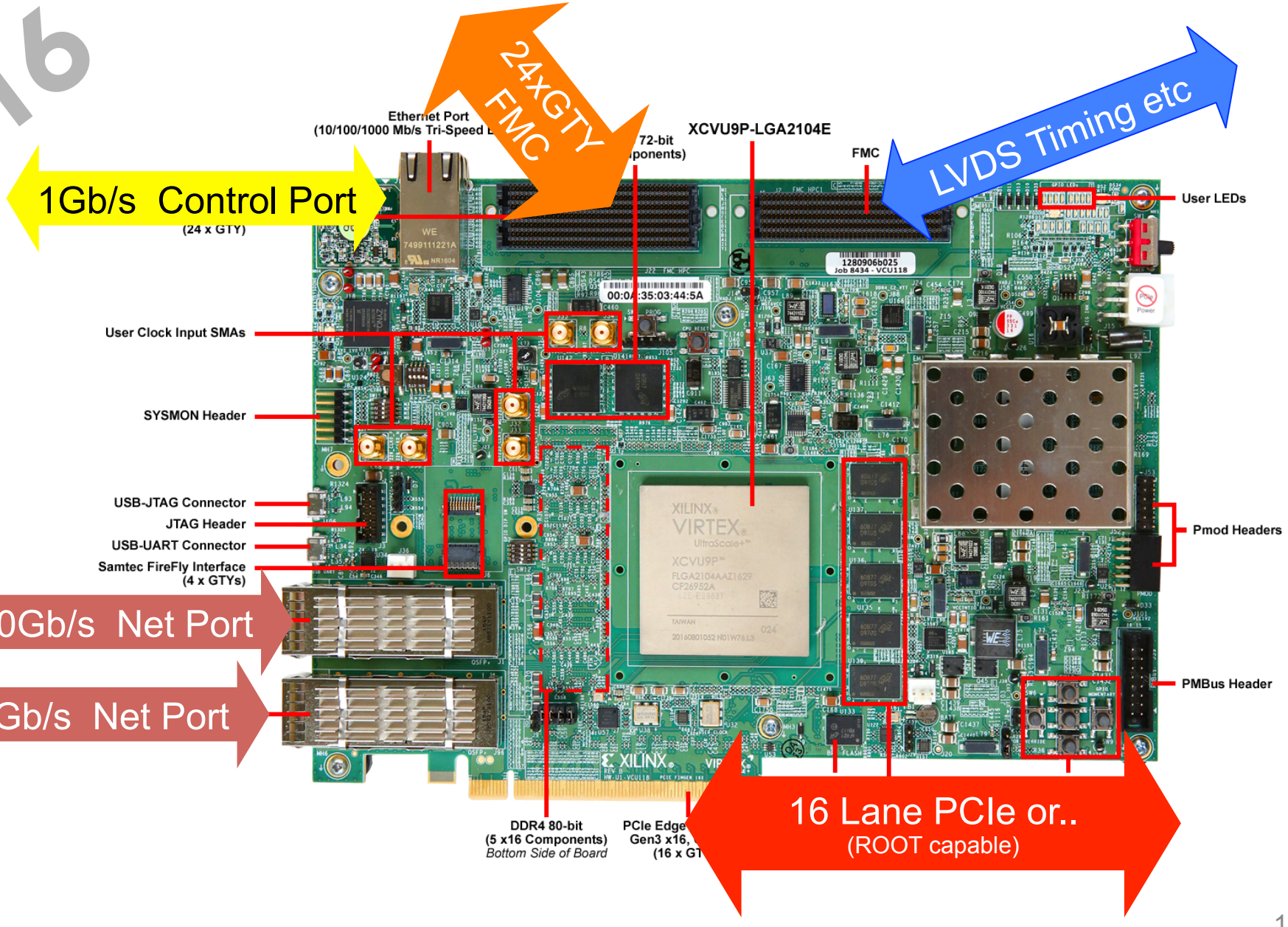
2015



Candidate for production use – Ultrascale+

EUROPEAN SPALLATION SOURCE

2016



Plan for the day……

Lots of talks, limited time.

Please only ask questions for clarification, discussion later !!!

Overall aims:

- *Simplicity*
- *Independent*
- *Unlimited bandwidth*
- *Flexibility to accommodate new instruments and technologies*
- *Good value: equipment and manpower costs, maintenance and operations effort*

Detector Data links to Event Formation

Tuesday, 9 May 2017 from **09:00** to **16:30** (GB)
at **Daresbury (CTH Boardroom)**

Manage

Description Meeting to discus the physical link and protocol connecting the back end readout master of detector readout systems to the event formation workstation.

Participants Steven Alcock; Richard Hall-Wilton; Rob Halsall; Morten Jagd Christensen; Scott Kolya; Jonas Nilsson; Tobias Richter; Maged Sallam; Martin Shetty

Material: Slides

Tuesday, 9 May 2017

09:30 - 16:30 Presentations

- 09:30 **Introduction** *20'*
  Speaker: Dr. Scott Kolya (European Spallation Source ERIC)
- 09:50 **Data Link Technology** *30'*
  Speaker: Steven Alcock (European Spallation Source ERIC)
- 10:20 **Fibre Link Technology** *20'*
  Speaker: Mr. Maged Sallam
- 10:40 **Introduction to ESS Data Processing** *20'*
  Speaker: Tobias Richter (European Spallation Source ERIC)
- 11:00 **Coffee Break** *10'*
- 11:10 **EF Date Receiver and Processing Framework** *30'*
  Speaker: Morten Jagd Christensen (European Spallation Source ERIC)
- 11:40 **What we do with the data** *20'*
  Speaker: Martin Shetty (European Spallation Source ERIC)
- 12:00 **DG -> EF Data Protocol Proposal** *30'*
  Speaker: Dr. Scott Kolya (European Spallation Source ERIC)
- 12:30 **Lunch** *1h0'*
  Daresbury Lab Restaurant
- 13:30 **Discussion** *3h0'*


STOP
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SPALLATION
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