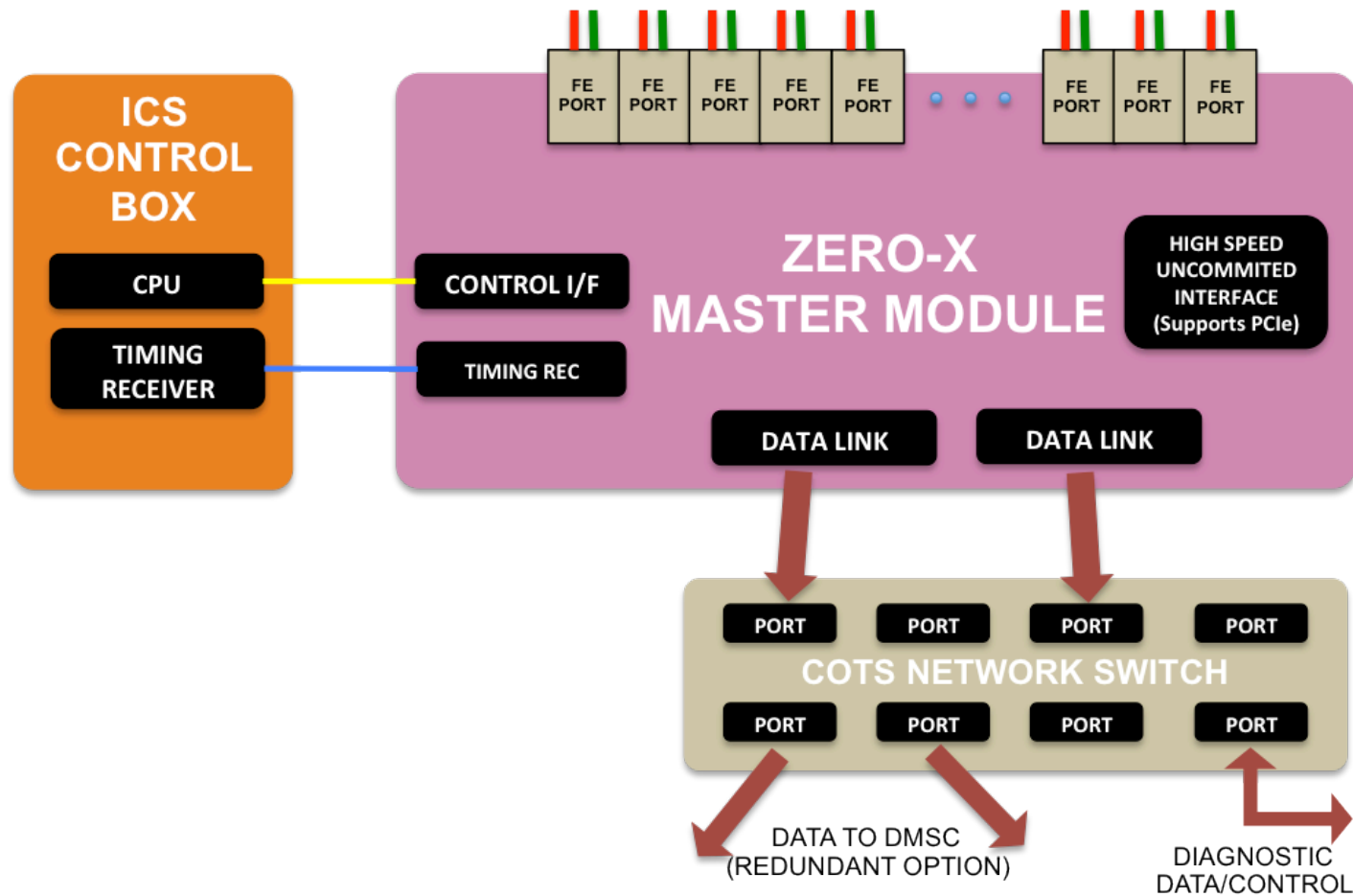




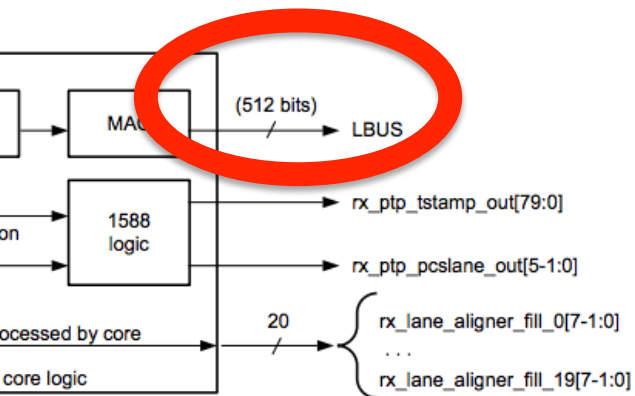
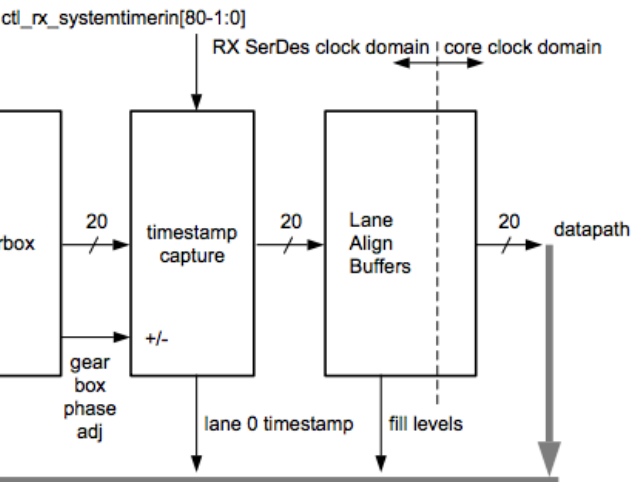
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Detector Data Links to DMSC Protocol

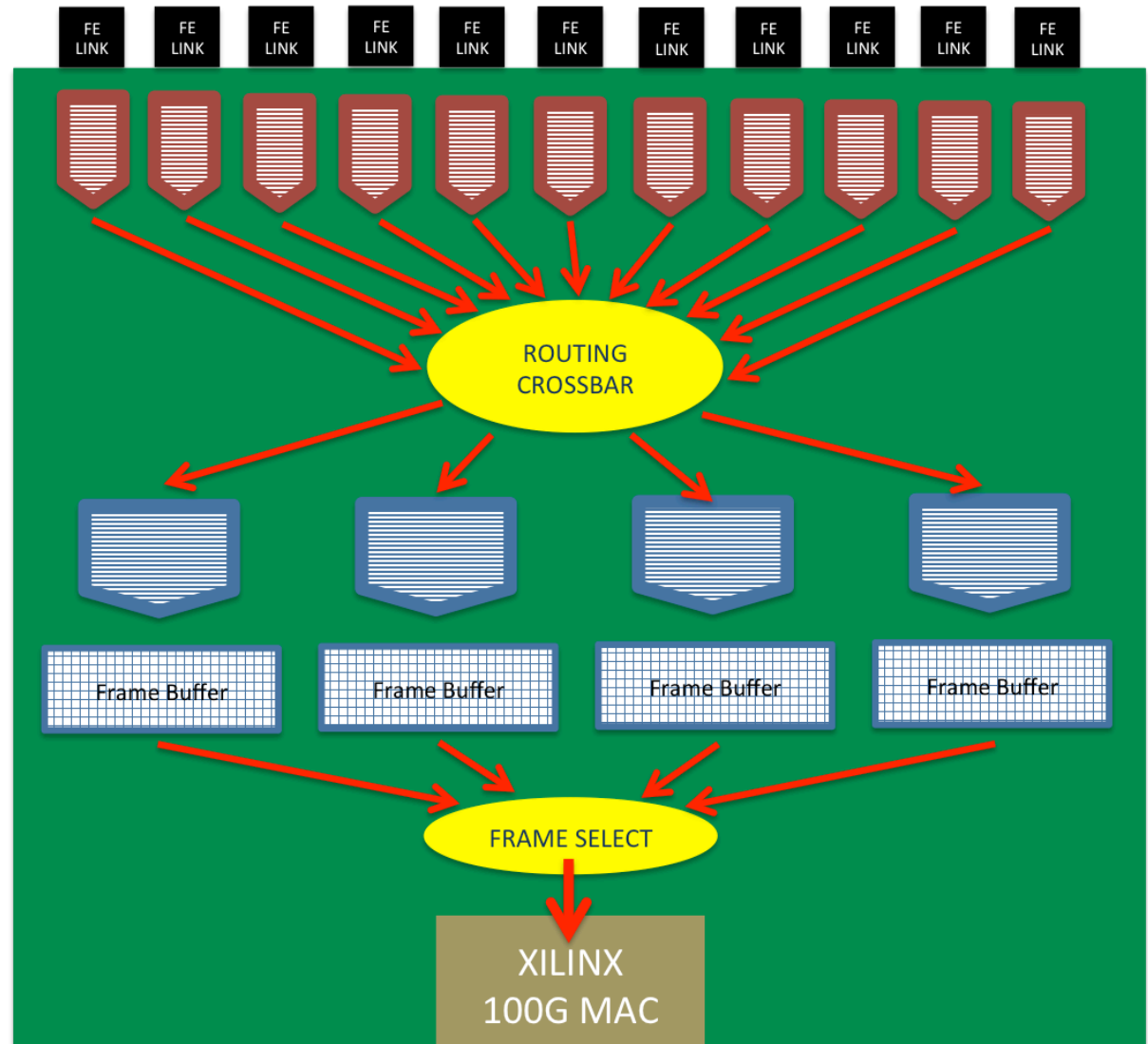
DG-DMSC EF Data Link Meeting
Daresbury 9th May 2017



Backend operation – Frame engines



X14342



Architecture determines what is possible...

The internal architecture used in the FPGA determines the ‘envelope of the possible’

Multiple streams of input data, may be out of time.

One request (Martin) was to ensure data arrive in chronological order.

Time sorting would consume significant resources – for discussion

We make the assumption that for some instruments at full luminosity, multiple EF units may be required and that some load balancing may be needed.

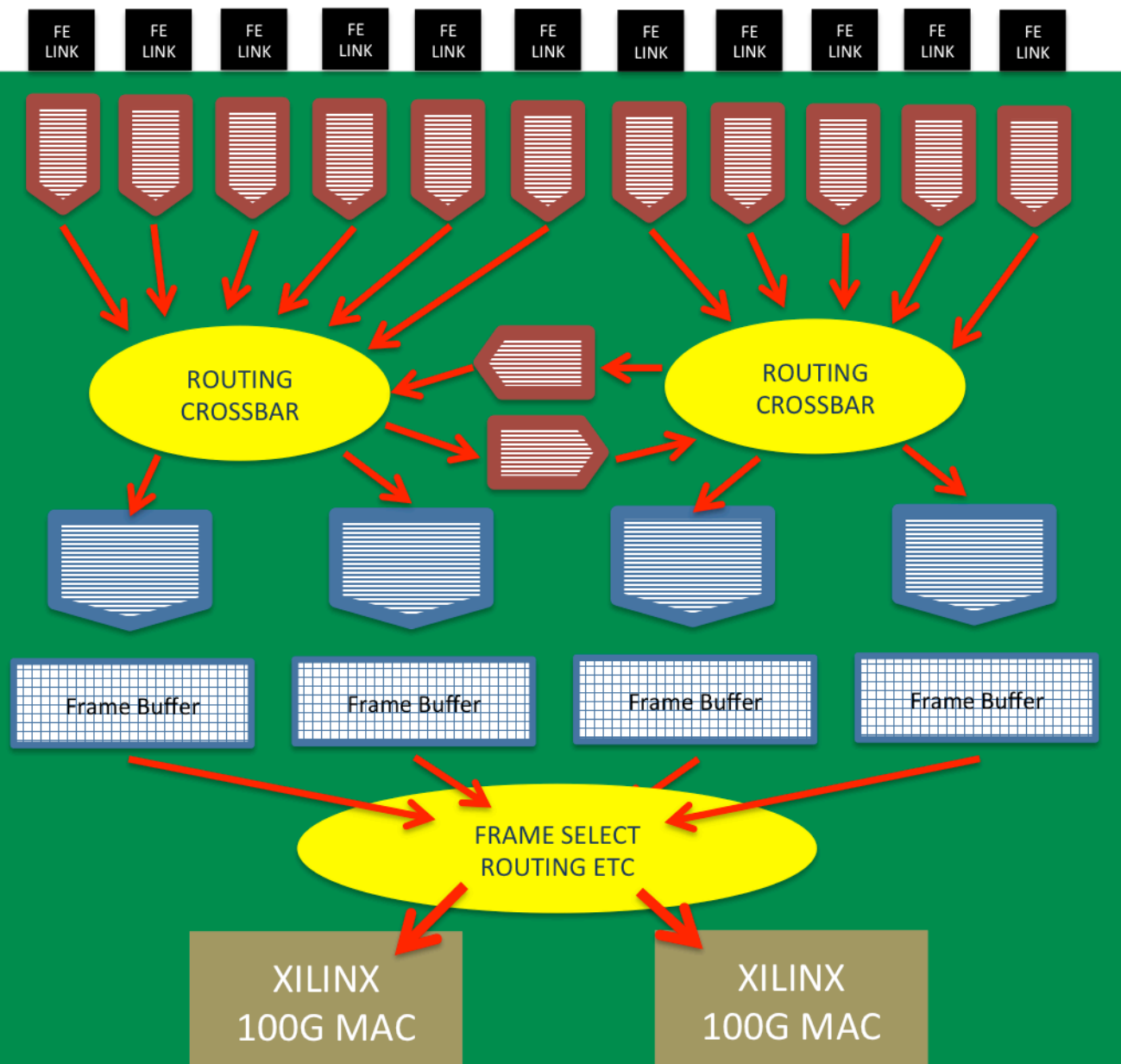
Data can be directed to different engines, and potentially engines can transmit to different destinations.

Must ensure relevant data stays together, eg anode/cathode for 2D match.

Ancillary data?

Some fast computation may be possible in the master, eg to expand a data format to help the software. Balance of network bandwidth used (bandwidth inside EF) vs. compute requirements. Should data fall naturally onto words or long-word boundaries? Should certain bits be extracted into byte fields?

We would be happy to investigate the feasibility of any beneficial processing.



Data from front end links (24 max speed 10G/25G)

Packets from front end received into FIFO.

Complete data packets routed to output FIFO for that type of data. Typically use one engine per output type (engines may 'overlap', eg one engine might have several distinct input FIFO buffers)

When there is enough data a full frame can be constructed in the Frame Buffer. Destination MAC can be different for each buffer. We can set a maximum latency, transmit partially full frame. Load sharing multiple destinations possible.

When at least one Frame Buffer is ready we can fire a packet as soon as we are ready.

Output packets need to be scheduled so that they will not overload the destination link speed. A programmable delay will be introduced. This can also reflect any limitations in the receiving workstation

It will be possible to reduce the overall rate of transmission by increasing this delay, but note that transmission will in any case only reflect the data rate (very low rate of status packets)

It will be possible to assign priority for transmission, and to mark some data as disposable (eg monitoring data could be dropped if data rate becomes too high)

CONNECTION/SESSION MANAGMENT- VIA ICS

NETWORK LAYER
(RawEthernet, UDP, etc.)

INSTRUMENT LAYER
(ID, Sequence, wordcounts etc.)

DATA LAYER
Module Format

DATA LAYER
Module Format

DATA LAYER
Module Format

DATA PACKET

DATA PACKET

DATA PACKET

The encapsulating network layer moves the data from point to point – not a real network with routing concerns etc.

Use raw Ethernet!

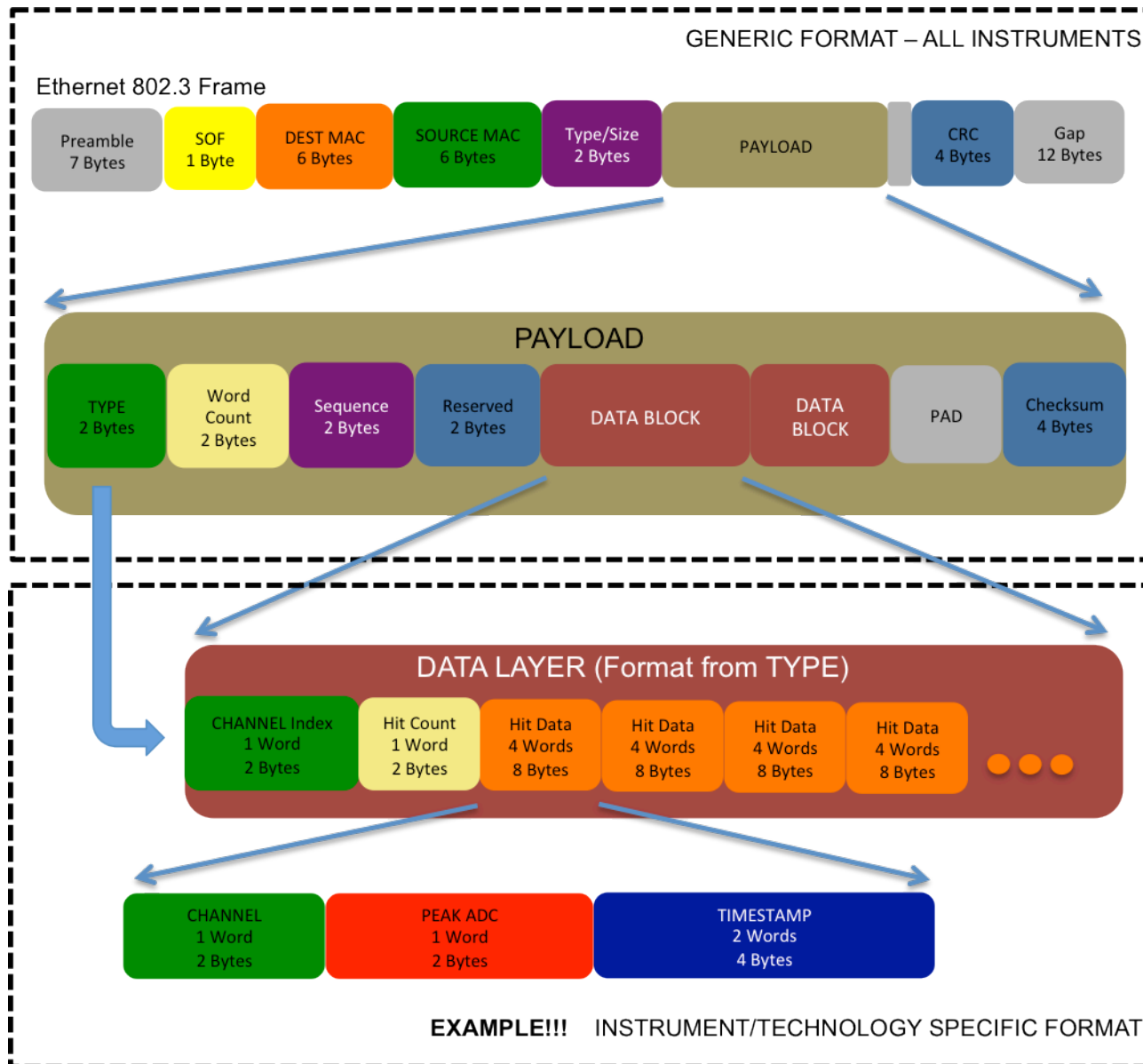
Destination address, maximum bandwidth (for packet scheduling) etc. configured through ICS.

The network layer could be exchanged without problems, eg this could be replaced by a simple FIFO interface in hardware (this was the original specification for this link).

The instrument layer is generic for all instruments that use the standard ESS back end readout (that is almost all of them)

The data layer depends on the instrument and detector technology being used. May not be unique to an instrument, the same or very similar format for the data protocol may be used

Data Paths in a Typical Detector Installation



PAYLOAD:

It is not forbidden (but it is unusual) to have more than one payload block per Ethernet frame.

TYPE

Used to define the type of data. Also defines source (eg different type for each engine)

SEQUENCE

Will be ascending number for that engine. Reset to zero at start of run.

CHECKSUM

To be defined.

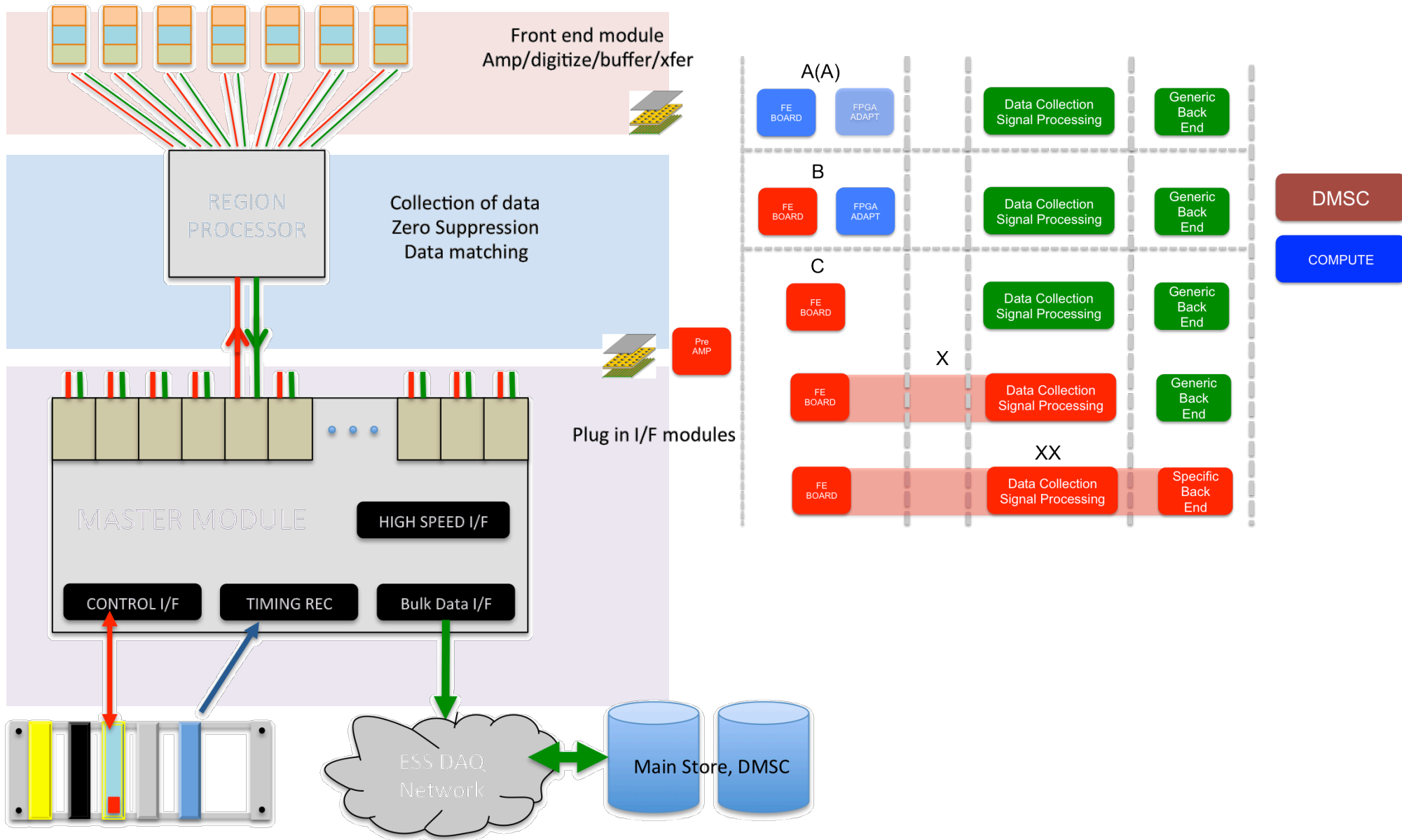
PADDING

Overall, we need to align to 512 bit (64 byte) boundaries. Gaps/Padding will be present to ensure this

Detector Baseline for Early Instruments (2017)

Instrument	Installation Start (est.)	Lead Institute	Main Detector Technology	Main Detector Developer	Front End Readout	FE Readout Developer	Integration Model
LOKI	Q1 2019	ISIS	BandGEM	Milan	Gemma/Gemini	Milan/INFN	B/X
			B10 Straws	ISIS (PT Inc)	VMM	ISIS/STFC/ESS	A
NMX	Q1 2019	ESS	Gd-GEM	CERN/ESS (BrightnESS)	VMM	CERN/ESS (BrightnESS)	A/X
ODIN	Q3 2019	TUM/PSI	MCP, Silicon, etc	Lots	Lots	Lots	X/XX
BEER	Q4 2019	HZG/NPI	A1CLD, AmCLD	HZG/DENEX	Delay Line	HZG/DENEX	Probably C
SKADI	Q4 2019	FZJ/LLB	SoNDE Pix Scinit	SoNDE	IDEAS ASIC	SoNDE	Probably B
DREAM	Q4 2019	FZJ	Jalouise	Julich/CDT	CIPIX	CDT	B/C
ESTIA	Q1 2020	PSI/ESS/LU/HU	Multi-Blade	Wigner/ESS (BrightnESS)	VMM	ESS Led (IK + BrightnESS)	A
C-SPEC	Q2 2020	ESS/TUM/LLB	Multi-Grid	ILL/CERN (BrightnESS)	VMM	ESS Led (IK + BrightnESS)	A
CAMEA/BIFROST	Q1 2021	DTU	He3 Tubes	Commercial	Commercial?	Commercial?	Probably X/XX
HEIMDAL	Q1 2021	PSI/DK/NO	Jalouise	Julich/CDT	CIPIX	CDT	B/C
FREIA	Q3 2021	ISIS	Multi-Blade	Wigner/ESS (BrightnESS)	VMM (MB)	ESS Led (IK+ BrightnESS)	A
T-REX	Q4 2021	ESS/FZJ	Multi-Grid	ILL/CERN (BrightnESS)	VMM	ESS Led (IK+ BrightnESS)	A
MAGIC	Q4 2021	FZJ/CDT/LLB	Jalouise	Julich/CDT	CIPIX	CDT	B/C
MIRACLES	Q1 2022	ESS-B	He3 Tubes	Commercial	Commercial?	Commercial?	Probably X/XX
VESPA	Q3 2022	CNR	He3 Tubes	Commercial	Commercial?	Commercial?	Probably X/XX
VOR??	???	ESS/WIGNER	Multi-Grid	ILL/CERN (BrightnESS)	VMM	ESS Led (IK+ BrightnESS)	A

Detector Integration Models



VMM - Pulse readout

(example, not definitive)



Data produced by ASIC (VMM2) is 38 bits for each 'hit', of pulse over threshold.

Time is measured at shaped peak.

Shaper has peaking time of 25,50,100,200nsec

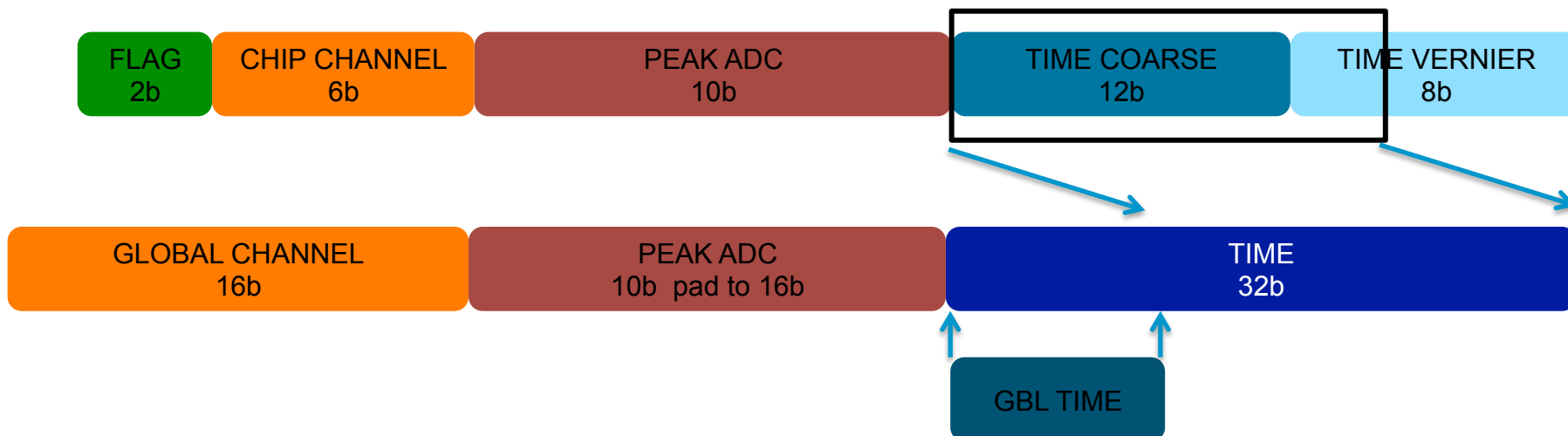
Eight gain ranges.

Dual polarity

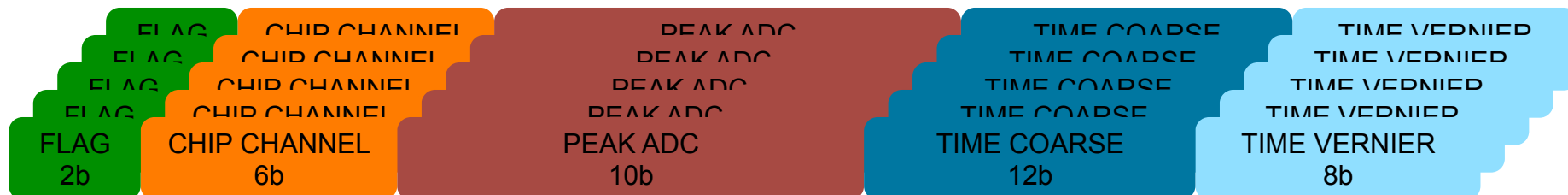
Timing designed to run at 40Mhz counter (100usec wrap), 256 bit vernier, but*

Actual sequencing and operation of chip not certain (to us), will be verified with first parts. VMM2 parts available soon.

Front-end or back-end FPGAs can slice/combine/format data as required



VMM Data Merging (Pre-clustering) Options

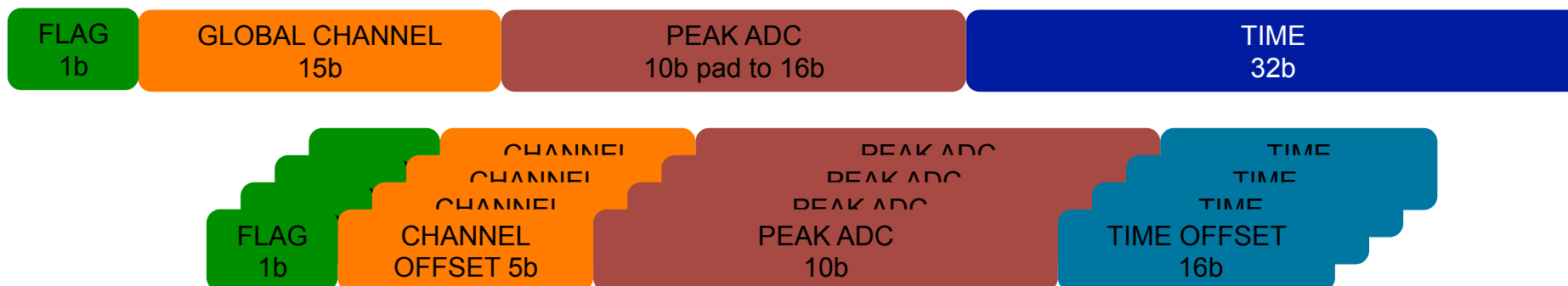


Charge sharing between grids means several channels may be hit by a single pulse (or deliberately triggered using the 'neighbour' feature).

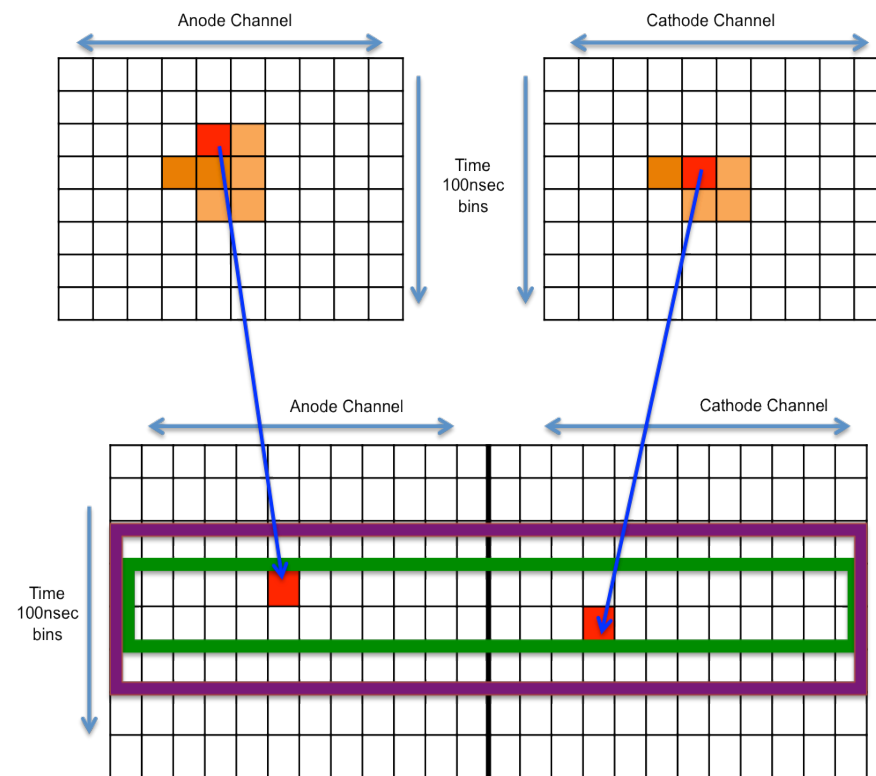
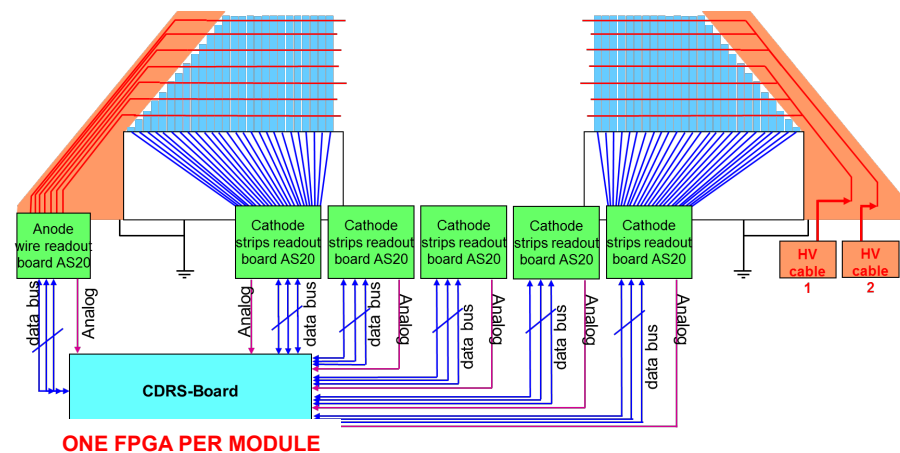
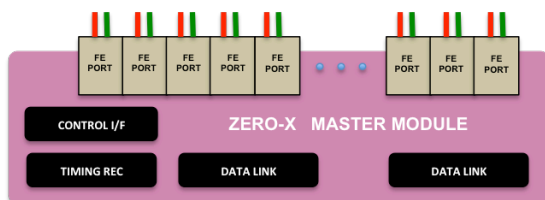
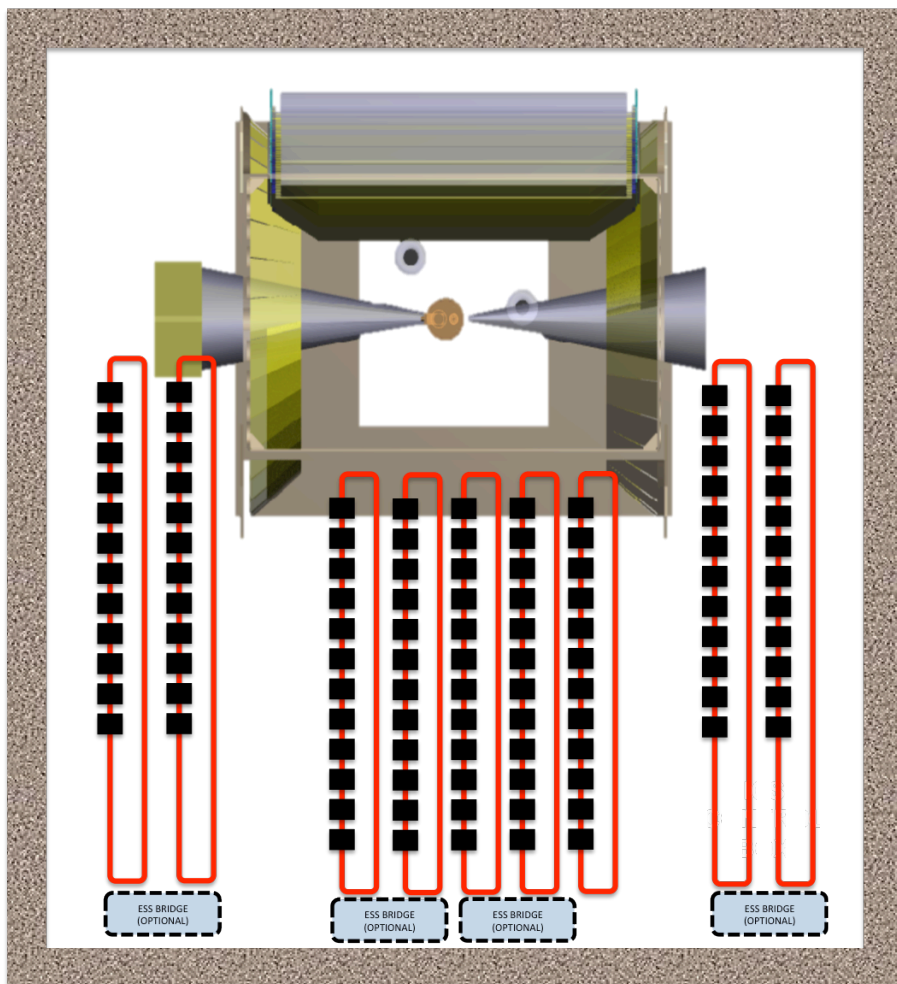
Can consider using a 'delta' format to reduce the overall data volume from a chip. Clustering to be studied on the basis of simulated data.

Index a group of adjacent hits against the first hit, no need to repeat full time or channel info.

Whatever we do, it will always be possible to expand back to individual channel, pulse height, and time info offline. I.e. lossless compression.



Jalousie CIPix – DREAM Instrument



Jalousie ClPix Hit Readout

(example, not definitive)

The technology (chamber, readout, etc.) is derived from POWTEX which has the following 64 bit hit structure:



The width of the timestamp is overkill!!

When operating with a chopper this is adapted to:



For ESS CDT recommend going from 64 bits to 128 bits, arguing bandwidth is cheap and this gives flexibility. However, 64 bits would be adequate, especially using the compression techniques we are likely to use elsewhere.

Key points for discussion...

Network selection.

Raw Ethernet, basic UDP, something else????

Timing resolution and timestamp sizes

Official ESS timestamps are 64 bit. 32 bit timestamps rollover at:

- 429 secs for 100nsec
- 43 secs for 10nsec
- 47 secs for 11.4 nsec (corresponds to ESS global clock of 88Mhz)

We can guarantee latency significantly below that, but we probably need some additional timestamp reference data, eg send data every time a rollover occurs? Or just 64 bit?

Data ordering

Multiple streams of input data, may be out of time.

Time sorting would consume significant resources.

Data Distribution

Multiple EF units, need to understand what goes where. In what ways are we able to partition systems?

Which instruments are the most likely to generate big data rates, and what technology do they use?

(Eg Multiblade, blades are essentially independent)

Ancillary Data

What ancillary data is needed for processing (config/status/monitoring/calibration) and where should that be sent?



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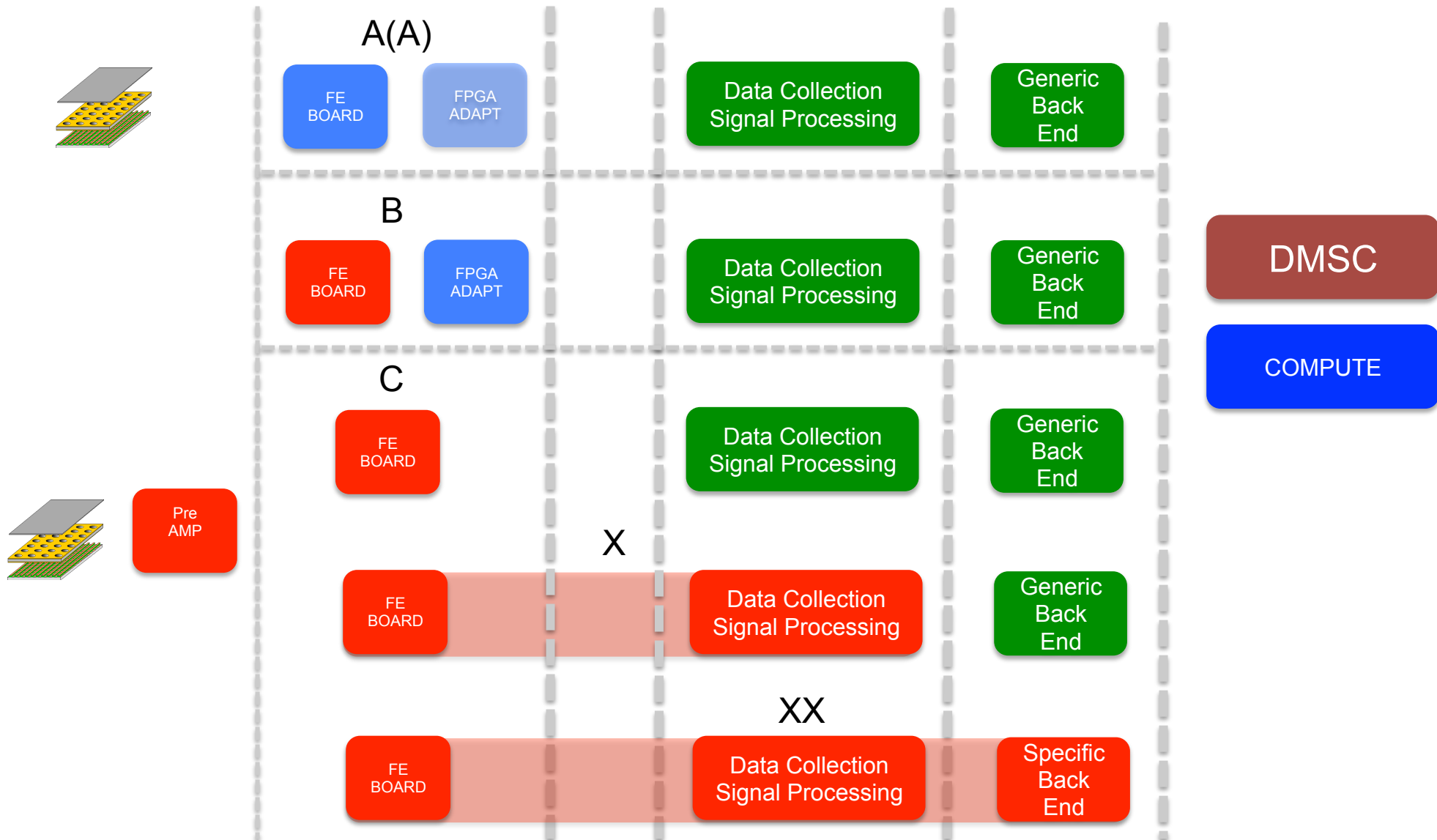




EUROPEAN
SPALLATION
SOURCE

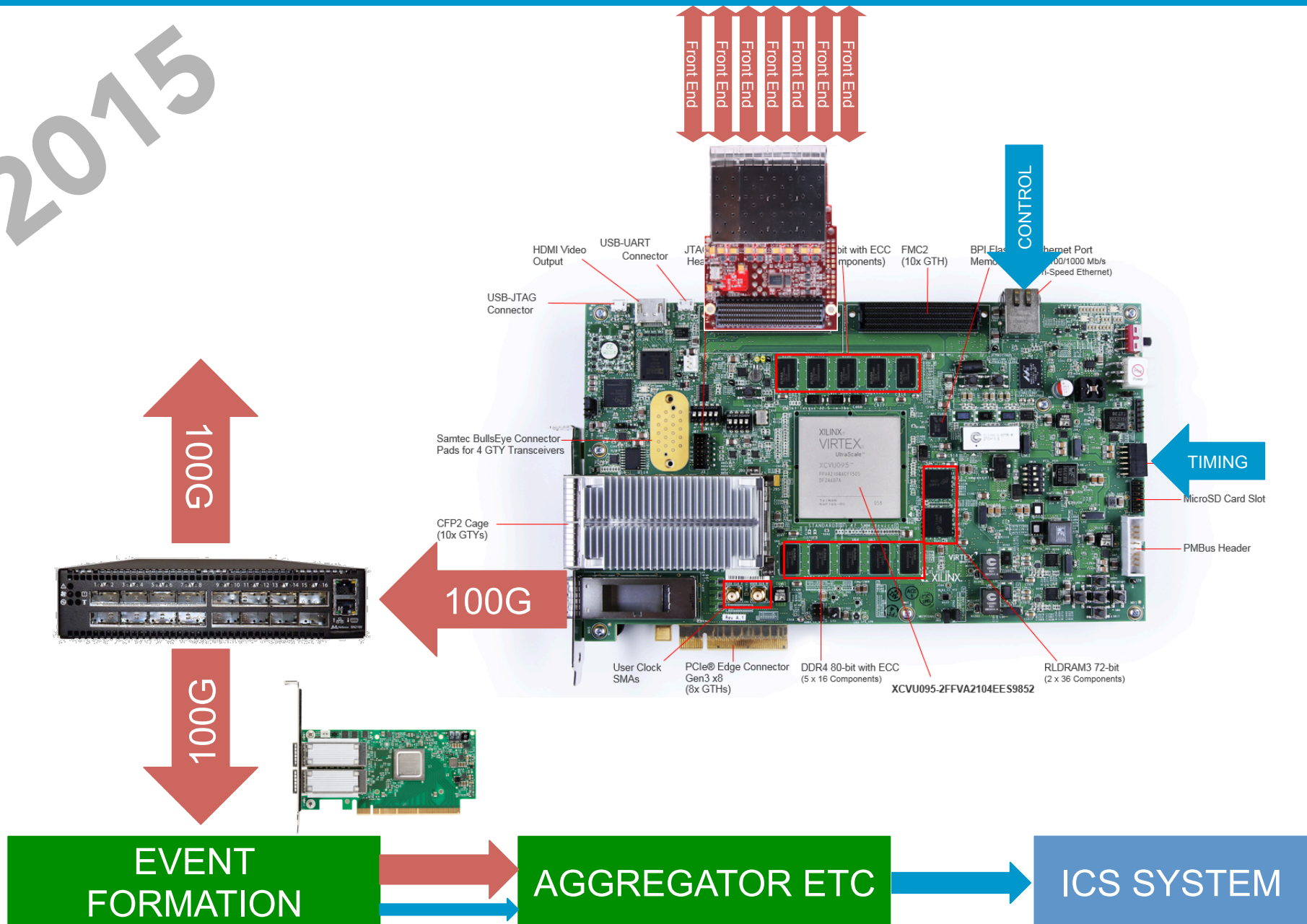
Backup Slides

Detector Integration Models



Last year's model !!! Used for test generators

2015



Candidate for production use – Ultrascale+



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SPALLATION
SOURCE

2016

