GEMINI User Manual

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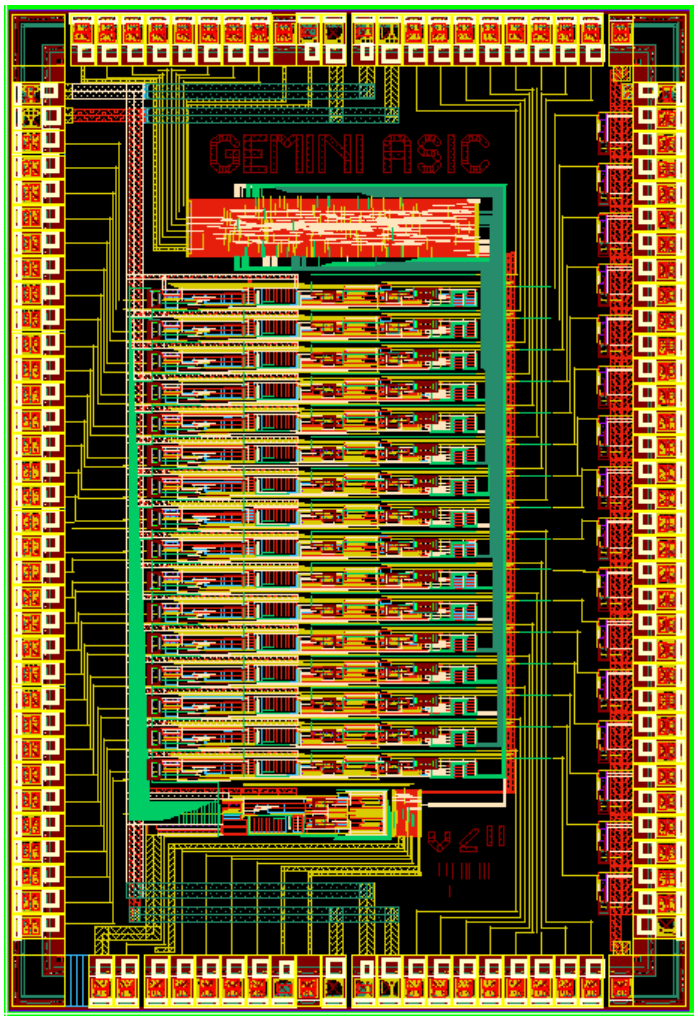

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Introduction

This manual is intended to be a brief guide for the **GEMINI** users, explaining its main functioning, possible configurations and performance.

Design Overview

The **GEMINI** ASIC has been developed by the Microelectronic Group at University of Milano-Bicocca in collaboration with the IFP-CNR and the LNF INFN institutions. It has been thought to be dedicated to Triple GEM detector structures, but it can easily be re-adapted for detectors with similar performance. It is made of 16 detecting channels, each including an auto-triggered *Charge Sensitive Preamplifier* (CSP) with auto-tuned feedback capacitor and a *Discriminator* with a channel independent programmable threshold.
The automatic calibration feature is provided in background by a dedicated unit, able to reach a feedback capacitor resolution less than 5%. The comparator programmable threshold is realized through the inclusion of a 9-bit R-2R Ladder DAC, with 1.2 mV LSB and 500 mV full-scale. The 9-bit threshold digital word can be set through an on-chip I^2C interface, with dedicated registers.
Two output signals for each channel are generated. The main output is digital. In fact, an LVDS signal is available for event counting rate up to 5 Mcps.
In addition, making off-chip spectroscopy measures or checking the detector signal is possible via the analog CSP output.

Changelog

- Pin Table image (Figure 1.1) corrected

1

Main Features

1.1 Package

The package chosen for the GEMINI is a Ceramic Quad-Flat Pack (CQFP) with 144 pins and 0.5 mm pin pitch. The package datasheet is included in page 15.

1.2 Pin List

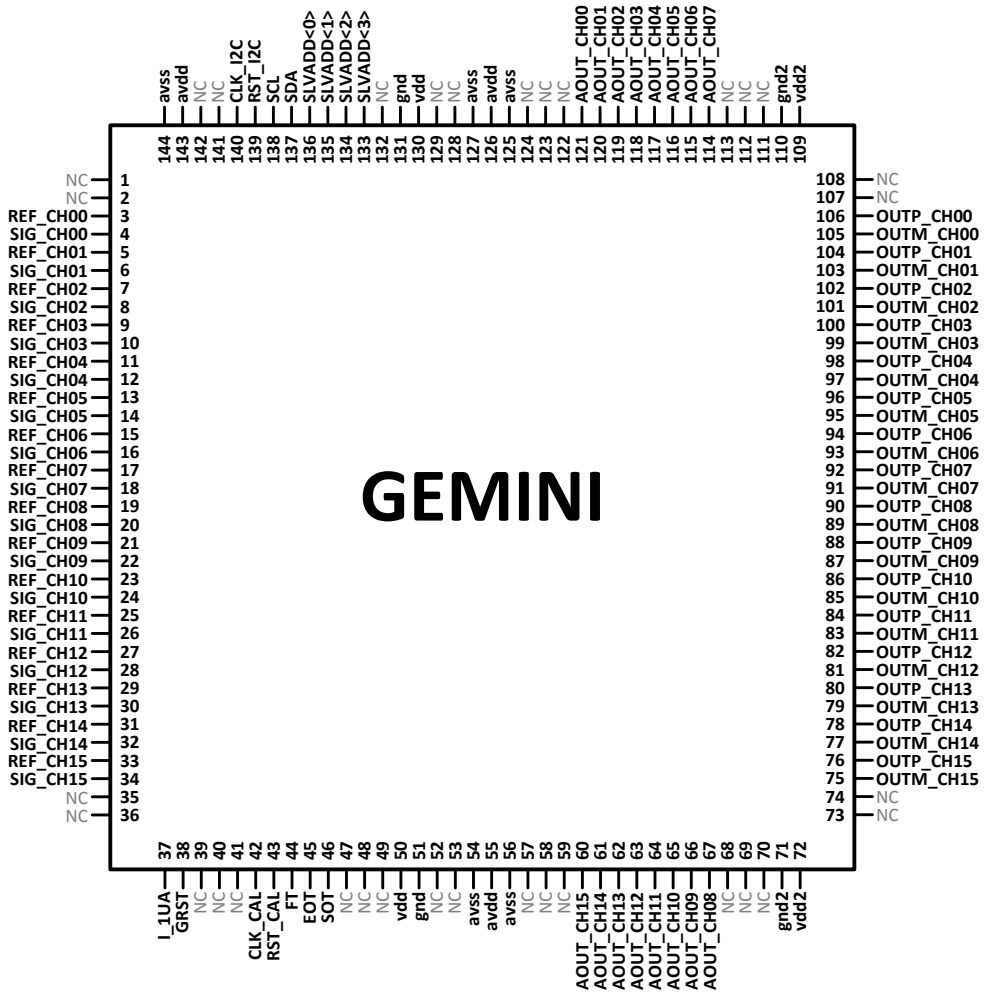

Figure 1.1: GEMINI package pins

#	Direction	Domain	Name	Description
1-2	-	-	-	**NOT CONNECTED**
3	Input	Analog	REF_CH00	Ch. 00 Common Mode Voltage
4	Input	Analog	SIG_CH00	Ch. 00 Signal Input
5	Input	Analog	REF_CH01	Ch. 01 Common Mode Voltage
6	Input	Analog	SIG_CH01	Ch. 01 Signal Input
7	Input	Analog	REF_CH02	Ch. 02 Common Mode Voltage
8	Input	Analog	SIG_CH02	Ch. 02 Signal Input
9	Input	Analog	REF_CH03	Ch. 03 Common Mode Voltage
10	Input	Analog	SIG_CH03	Ch. 03 Signal Input
11	Input	Analog	REF_CH04	Ch. 04 Common Mode Voltage
12	Input	Analog	SIG_CH04	Ch. 04 Signal Input
13	Input	Analog	REF_CH05	Ch. 05 Common Mode Voltage
14	Input	Analog	SIG_CH05	Ch. 05 Signal Input
15	Input	Analog	REF_CH06	Ch. 06 Common Mode Voltage
16	Input	Analog	SIG_CH06	Ch. 06 Signal Input
17	Input	Analog	REF_CH07	Ch. 07 Common Mode Voltage
18	Input	Analog	SIG_CH07	Ch. 07 Signal Input
19	Input	Analog	REF_CH08	Ch. 08 Common Mode Voltage
20	Input	Analog	SIG_CH08	Ch. 08 Signal Input
21	Input	Analog	REF_CH09	Ch. 09 Common Mode Voltage
22	Input	Analog	SIG_CH09	Ch. 09 Signal Input
23	Input	Analog	REF_CH10	Ch. 10 Common Mode Voltage
24	Input	Analog	SIG_CH10	Ch. 10 Signal Input
25	Input	Analog	REF_CH11	Ch. 11 Common Mode Voltage
26	Input	Analog	SIG_CH11	Ch. 11 Signal Input
27	Input	Analog	REF_CH12	Ch. 12 Common Mode Voltage
28	Input	Analog	SIG_CH12	Ch. 12 Signal Input
29	Input	Analog	REF_CH13	Ch. 13 Common Mode Voltage
30	Input	Analog	SIG_CH13	Ch. 13 Signal Input
31	Input	Analog	REF_CH14	Ch. 14 Common Mode Voltage
32	Input	Analog	SIG_CH14	Ch. 14 Signal Input
33	Input	Analog	REF_CH15	Ch. 15 Common Mode Voltage
34	Input	Analog	SIG_CH15	Ch. 15 Signal Input
35, 36	-	-	-	**NOT CONNECTED**
37	Input	Analog	I_1UA	1 μA Reference Current
38	Input	Analog	GRST	General Channel Reset
39-41	-	-	-	**NOT CONNECTED**
42	Input	Digital	CLK_CAL	12.5 MHz Clock for Calibration
43	Input	Digital	RST_CAL	Calibration Reset Signal
44	Input	Digital	FT	Force Manual Tuning Enable
45	Output	Digital	EOT	End of Tuning Flag
46	Input	Digital	SOT	Start of Tuning Enable

#	Direction	Domain	Name	Description
47-49	-	-	-	**NOT CONNECTED**
50	I/O	Digital	vdd	Digital Supply Voltage (2 V)
51	I/O	Digital	gnd	Digital Ground (0 V)
52-53	-	-	-	**NOT CONNECTED**
54	I/O	Analog	avss	Analog Ground (0 V)
55	I/O	Analog	avdd	Analog Supply Voltage (2 V)
56	I/O	Analog	avss	Analog Ground (0 V)
57-59	-	-	-	**NOT CONNECTED**
60	Output	Analog	AOUT_CH15	Ch. 15 Analog Output
61	Output	Analog	AOUT_CH14	Ch. 14 Analog Output
62	Output	Analog	AOUT_CH13	Ch. 13 Analog Output
63	Output	Analog	AOUT_CH12	Ch. 12 Analog Output
64	Output	Analog	AOUT_CH11	Ch. 11 Analog Output
65	Output	Analog	AOUT_CH10	Ch. 10 Analog Output
66	Output	Analog	AOUT_CH09	Ch. 09 Analog Output
67	Output	Analog	AOUT_CH08	Ch. 08 Analog Output
68-70	-	-	-	**NOT CONNECTED**
71	I/O	Digital	gnd2	Digital LVDS Ground (0 V)
72	I/O	Digital	vdd2	Digital LVDS Supply Voltage (2 V)
73, 74	-	-	-	**NOT CONNECTED**
75	Output	Digital	OUTM_CH15	Ch. 15 LVDS Output (Minus)
76	Output	Digital	OUTP_CH15	Ch. 15 LVDS Output (Plus)
77	Output	Digital	OUTM_CH14	Ch. 14 LVDS Output (Minus)
78	Output	Digital	OUTP_CH14	Ch. 14 LVDS Output (Plus)
79	Output	Digital	OUTM_CH13	Ch. 13 LVDS Output (Minus)
80	Output	Digital	OUTP_CH13	Ch. 13 LVDS Output (Plus)
81	Output	Digital	OUTM_CH12	Ch. 12 LVDS Output (Minus)
82	Output	Digital	OUTP_CH12	Ch. 12 LVDS Output (Plus)
83	Output	Digital	OUTM_CH11	Ch. 11 LVDS Output (Minus)
84	Output	Digital	OUTP_CH11	Ch. 11 LVDS Output (Plus)
85	Output	Digital	OUTM_CH10	Ch. 10 LVDS Output (Minus)
86	Output	Digital	OUTP_CH10	Ch. 10 LVDS Output (Plus)
87	Output	Digital	OUTM_CH09	Ch. 09 LVDS Output (Minus)
88	Output	Digital	OUTP_CH09	Ch. 09 LVDS Output (Plus)
89	Output	Digital	OUTM_CH08	Ch. 08 LVDS Output (Minus)
90	Output	Digital	OUTP_CH08	Ch. 08 LVDS Output (Plus)
91	Output	Digital	OUTM_CH07	Ch. 07 LVDS Output (Minus)
92	Output	Digital	OUTP_CH07	Ch. 07 LVDS Output (Plus)
93	Output	Digital	OUTM_CH06	Ch. 06 LVDS Output (Minus)
94	Output	Digital	OUTP_CH06	Ch. 06 LVDS Output (Plus)
95	Output	Digital	OUTM_CH05	Ch. 05 LVDS Output (Minus)
96	Output	Digital	OUTP_CH05	Ch. 05 LVDS Output (Plus)

#	Direction	Domain	Name	Description
97	Output	Digital	OUTM_CH04	Ch. 04 LVDS Output (Minus)
98	Output	Digital	OUTP_CH04	Ch. 04 LVDS Output (Plus)
99	Output	Digital	OUTM_CH03	Ch. 03 LVDS Output (Minus)
100	Output	Digital	OUTP_CH03	Ch. 03 LVDS Output (Plus)
101	Output	Digital	OUTM_CH02	Ch. 02 LVDS Output (Minus)
102	Output	Digital	OUTP_CH02	Ch. 02 LVDS Output (Plus)
103	Output	Digital	OUTM_CH01	Ch. 01 LVDS Output (Minus)
104	Output	Digital	OUTP_CH01	Ch. 01 LVDS Output (Plus)
105	Output	Digital	OUTM_CH00	Ch. 00 LVDS Output (Minus)
106	Output	Digital	OUTP_CH00	Ch. 00 LVDS Output (Plus)
107, 108	-	-	-	**NOT CONNECTED**
109	I/O	Digital	vdd2	Digital LVDS Supply Voltage (2 V)
110	I/O	Digital	gnd2	Digital LVDS Ground (0 V)
111-113	-	-	-	**NOT CONNECTED**
114	Output	Analog	AOUT_CH07	Ch. 07 Analog Output
115	Output	Analog	AOUT_CH06	Ch. 06 Analog Output
116	Output	Analog	AOUT_CH05	Ch. 05 Analog Output
117	Output	Analog	AOUT_CH04	Ch. 04 Analog Output
118	Output	Analog	AOUT_CH03	Ch. 03 Analog Output
119	Output	Analog	AOUT_CH02	Ch. 02 Analog Output
120	Output	Analog	AOUT_CH01	Ch. 01 Analog Output
121	Output	Analog	AOUT_CH00	Ch. 00 Analog Output
122-124	-	-	-	**NOT CONNECTED**
125	I/O	Analog	avss	Analog Ground (0 V)
126	I/O	Analog	avdd	Analog Supply Voltage (2 V)
127	I/O	Analog	avss	Analog Ground (0 V)
128, 129	-	-	-	**NOT CONNECTED**
130	I/O	Digital	vdd	Digital Supply Voltage (2 V)
131	I/O	Digital	gnd	Digital Ground (0 V)
132	-	-	-	**NOT CONNECTED**
133	Input	Digital	SLVADD<3>	I^2C Slave Address MSB
134	Input	Digital	SLVADD<2>	I^2C Slave Address Bit 2
135	Input	Digital	SLVADD<1>	I^2C Slave Address Bit 1
136	Input	Digital	SLVADD<0>	I^2C Slave Address LSB
137	I/O	Digital	SDA	I^2C Serial Data Bus
138	Input	Digital	SCL	I^2C Serial Clock Bus
139	Input	Digital	RST_I2C	I^2C Reset
140	Input	Digital	CLK_I2C	I^2C Clock Reference
141, 142	-	-	-	**NOT CONNECTED**
143	I/O	Analog	avdd	Analog Supply Voltage (2 V)
144	I/O	Analog	avss	Analog Ground (0 V)

Table 1.1: GEMINI Pin List

2

Channel Basics & Settings

2.1 Specifications

The specifications imposed for GEMINI in order to be efficiently compliant with the detector are listed in table 2.1.

Parameter	Value	Parameter	Value
Count Rate	> 3 Mcps	Max Pixel Capacitance	40 pF
# of Channels	16	Q-to-V Gain	1 mV/fC
Sensitivity	< 3 fC	Reset Trigger	Event-Based
Max Detection Jitter	9 ns	Gain Accuracy	5%

Table 2.1: GEMINI specifications

2.2 Structure

In Fig. 2.1 the GEMINI read-out scheme is depicted, together with a channel main signals example plot.
The SoC is made of 16 channels where, with the inclusion of a *Charge-Sensitive Preamplifier* (CSP), the signal from the detector is converted from charge domain to voltage domain.
Then, the *Discriminator* (DISC) compares the CSP output voltage level with a threshold, set by an *R-2R Resistive DAC* and specific for each detecting channel, generating the Event Detection output signal. This output is then converted into LVDS standard through a dedicated driver.
The channel also produces an analog output signal, which is the buffered CSP output.

2.2.1 The Charge-Sensitive Preamplifier

The CSP composes of a Class-A Miller Operational Amplifier (Opamp) with the C_F capacitor connected in feedback, in parallel with a switch.
The Q-V Gain imposed by specifications, i.e. 1 mV/fC, sets directly C_F to 1 pF.
With a 40 pF C_D (pixel capacitance) maximum value, dimensioning the Opamp to obtain 65 dB DC-Gain and 80 μV_{RMS} of in-band integrated noise means that the Signal-to-Noise-Ratio lies in a range between 19 dB and 43 dB, with minimum (30 fC) and maximum (500 fC) charge respectively, while the charge collection efficiency is 98%.

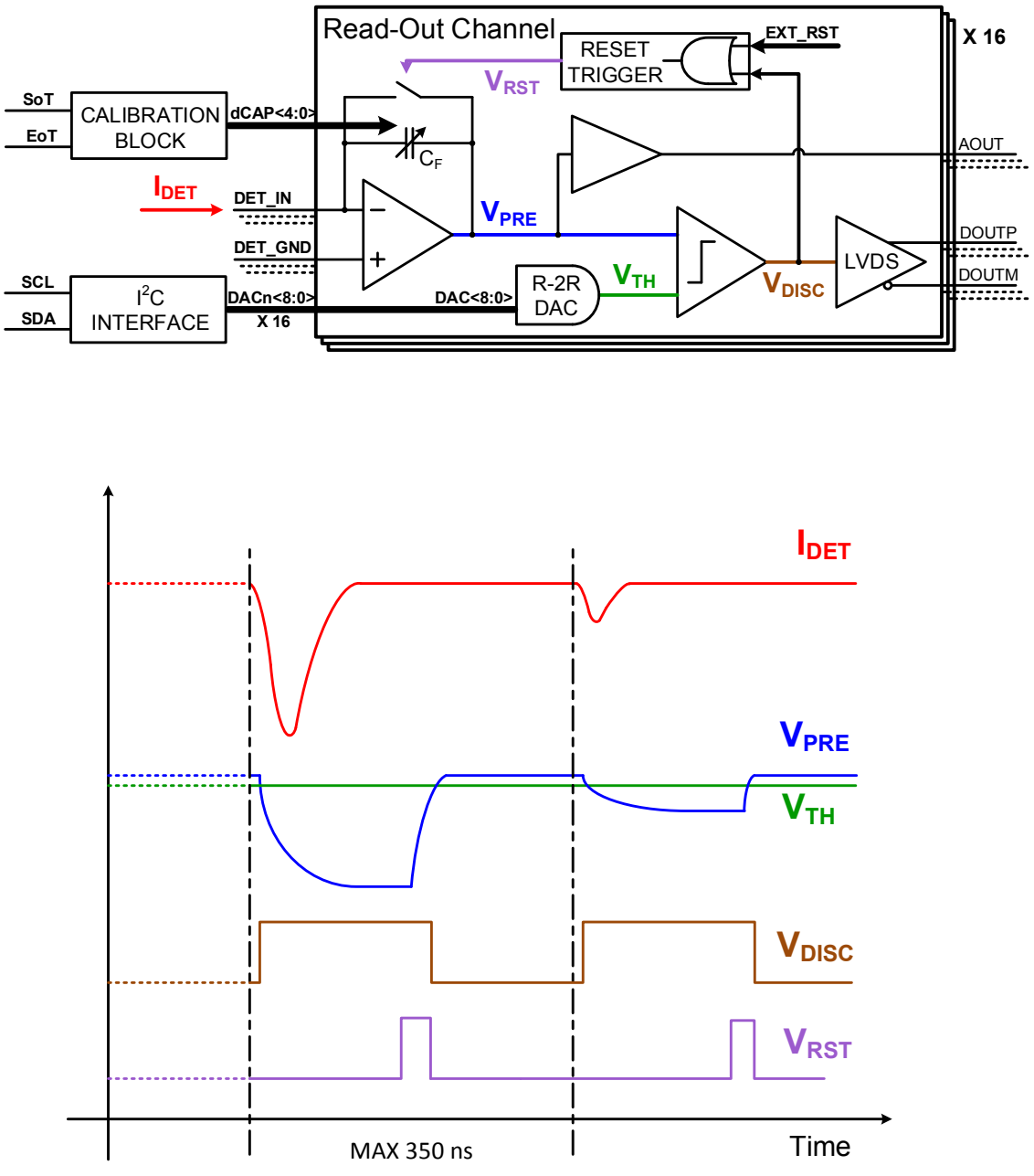

Figure 2.1: GEMINI SoC Block Scheme

2.2.2 The Discriminator

As regards the DISC, the main target is to reduce the input stage offset, in order to achieve the sensitivity and the detection jitter required (3 fC and 9 ns respectively). This means that the maximum tolerated offset is 3 mV after the CSP conversion, as well as for the R-2R Resistive DAC LSB, representing the minimum threshold.
Designing the DISC with a mirrored structure and exploiting the inter-digitated layout technique allows to limit the offset within specs. At the same time, since the detector charge polarity is intrinsically negative (the signal is generated by electrons), the CSP output signal embeds a decreasing behavior. For this reason, a PMOS DISC input stage has been preferred to NMOS.
Dealing with the threshold, the 9-bit R-2R Resistive DAC has a 1.2 mV LSB and 500 mV full-scale. The input digital words, independent for each channel, are stored into dedicated registers managed from the I^2C interface.
The event-driven reset signal is generated starting from the DISC output. In fact, with the simple use of a passive RC net and an OR logic gate, the reset pulse delay set. In detail, the RC time constant is applied to the DISC output signal and send to one OR input. When the voltage is high enough the OR switches high, closing the CSP feedback switch. The other OR input has been used as a general channel reset (*GRST* pin). In this case, a time constant of 150 ns has been set.

2.3 Calibration

The channel structure of GEMINI relies on capacitors, included in the CSP feedback and in the CSP Opamp for stability compensation. For correct functioning, their maximum spread has not to exceed 5%. In fact, the CSP feedback capacitor (C_F) value controls the CSP gain, as well as the loop gain and the Opamp phase margin. But the CMOS integration process, due to its nature, leads to statistical variations of all parameters involved in a circuit, and its precision by itself is not enough. The solution for this issue consists in designing a calibration circuit, able to tune the capacitance actual value directly on-chip and automatically, including only a precise current reference and a stable clock signal. Practically, cited critical capacitors have been implemented with a switchable binary-weighted capacitor arrays. A logic unit algorithmically manages the array opportunely with a digital word, limiting the maximum error in capacitances with respect to the nominal value (ϵ_c) as in Eq. (2.1). ΔC represents the maximum capacitance spread due to CMOS process variations.

$$\epsilon_c = \frac{\Delta C}{2^{N-1}} \tag{2.1}$$

Note that fixing the number of array bits N corresponds to fixing the maximum error. In this project 5-bit arrays have been chosen to obtain the desired spread range.

2.4 Digital Control: I²C interface

The GEMINI embeds an I²C interface for controlling the calibration and channel settings. It exploits the I²C bidirectional 2-line feature for managing up to 16 ASICs at the same time (256 channels) with a single external master device, achieving a strong improvement in portability. As regards the channels, I²C data registers store the 16 9-bit digital words for setting the DISC thresholds, via the R-2R DACs. The I²C interface also controls directly the calibration unit option for manually setting the capacitors digital word, through a dedicated I²C register.

2.4.1 I²C Registers Address

In the chip GEMINI, 32 8-bit registers have been included. Their main task is to store the threshold 9-bit digital word to be set as the R-2R DACs input for each channel, DACxx<8:0>. Since the I²C protocol is based on 8-bit words, two registers for each channel are needed. The bit description is shown in Fig. 2.2, where *xx* stands for 00 to 14, and *yy* for 00 to 15. In fact, the R15H register includes also the 5-bit manual tuning digital word *EXT_FT*, in case of manual calibration mode selection (*FT* pin HIGH). In Tab. 2.2 I²C addresses are shown.

RxxH<7:0>

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	Not Used	DACxx<8>

RyyL<7:0>

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
DACyy<7>	DACyy<6>	DACyy<5>	DACyy<4>	DACyy<3>	DACyy<2>	DACyy<1>	DACyy<0>

R15H<7:0>

<7>	<6>	<5>	<4>	<3>	<2>	<1>	<0>
EXT_FT<4>	EXT_FT<3>	EXT_FT<2>	EXT_FT<1>	EXT_FT<0>	Not Used	Not Used	DAC15<8>

Figure 2.2: I²C registers bit description

Name	Address	Name	Address	Name	Address	Name	Address
R00H	0x00	R04H	0x08	R08H	0x10	R12H	0x17
R00L	0x01	R04L	0x09	R08L	0x11	R12L	0x18
R01H	0x02	R05H	0x0a	R09H	0x12	R13H	0x19
R01L	0x03	R05L	0x0b	R09L	0x13	R13L	0x1a
R02H	0x04	R06H	0x0c	R10H	0x14	R14L	0x1b
R03H	0x06	R07H	0x0e	R11H	0x15	R15H	0x1c
R04L	0x07	R07L	0x0f	R11L	0x16	R15L	0x1d

Table 2.2: I²C registers address

3

Functioning Settings

In this chapter the steps to be followed in order to put GEMINI in correct functioning are described.

3.1 Step 1: Power-Up

To correctly bias the GEMMA chip, the user should set the pins as indicated in Tab. 3.1.

Pin	Bias Level	Power Absorption
avdd	2 V	47 mW
avss	0 V	-
vdd	2 V	1 mW
gnd	0 V	-
vdd2	2 V	125 mW
gnd2	0 V	-

Table 3.1: Power Supplies

As regards the channels input, the pins labeled as *REF_CHxx* have to be biased to 1 V, the CSP input common mode.
The *I_1UA* pin should be biased with a 1 µA DC-current flowing from *avdd* to *avss* with a 1% precision.
At the chip power-up, the *GRST* pin should be put HIGH for a few µs in order to reset the channels and allow the CSP Feedback Capacitance C_F to completely discharge.

3.2 Step 2: I^2C registers settings

The embedded I^2C interface is supplied with the digital power domain (*vdd* - *gnd*). So, in order to comply with different supply voltages, an off-chip level shifter is required. The *SDA* and *SCL* buses are required to be connected in pull-up configuration with a 4.7 kΩ off-chip resistor. The clock for I^2C interface and internal registers is to be set via the *CLK_I2C* pin, also with digital supply bias levels.
The I^2C interface is in slave mode. The *SLVADD<3:0>* pins set the I^2C device address, for identifying the specific chip. Up to 16 chips can be connected to the same master device.
The *RST_I2C* pin should be set HIGH at the chip startup for at least 10 *CLK_I2C* periods.

The possible operations on internal registers are 4, with related time diagrams shown in Fig 3.1:

- Single Write (Figure 3.1a)
- Multiple Write (Figure 3.1b)
- Single Read (Figure 3.1c)
- Multiple Read (Figure 3.1d)

In the diagrams, HW_ADDR represents the 4-bit chip address, REG_ADDR is the internal register address (listed in Tab. 2.2) and DATA is the actual 8-bit word sent to or received from the register. Note that the multiple write/read mode allows the user to write/read the registers in sequence without re-addressing, starting from the register indicated in REG_ADDR.

3.3 Step 3: Calibration settings

The calibration of the CSP feedback capacitance C_F in Fig. 2.1 is expected to run in background. Running it during measurements can affect the results. It is advisable to run calibration at chip startup.
The clock reference, *CLK_CAL*, should be set to 12.5 MHz with digital supply bias levels (2 V - 0 V), which are the same for every pin related to calibration.
In order to start it correctly, the *RST_CAL* pin should be set HIGH for at least 800 ns. To start the calibration, the *SOT* pin should be set HIGH. The *EOT* pin will become HIGH when the calibration ends.
If another calibration is required, setting LOW and consequently HIGH the *SOT* pin restarts the calibration.
Whenever the user would set manually the 5-bit calibration digital word EXT_FT<4:0>, it has to be written into R15H I^2C register, in bits <7:4>. After that, the *FT* pin (normally LOW) should be set HIGH, and the calibration word will be sent to channels (commonly).
It is possible to check the actual C_F value by analyzing the *AOUT_CHxx* output voltage with an *a priori* known charge pulse as channel input.

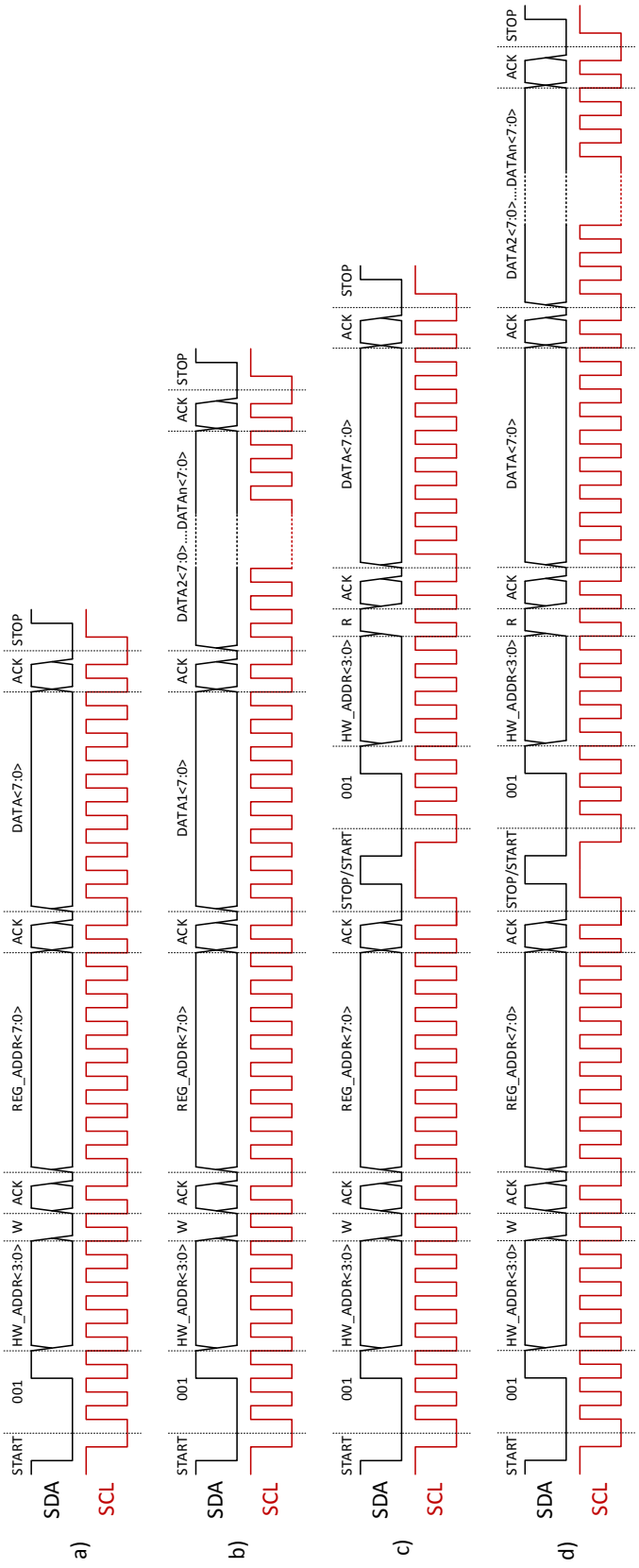

Figure 3.1: GEMINI I^{2}C Time Diagrams

4

Performance

The GEMMA layout is depicted in title page, occupying 6.89 mm^2.
After parasitic extraction, a Monte-Carlo post-layout simulation has been run, including temperature variation between −40 °C and 120 °C, as well as 10% maximum supply voltage spread. The input pixel capacitance has been set to 40 pF. This worst-case scenario represents an optimum testbench also for radiation hardness. Although measurements while irradiating samples are a must, these results can prove for an overall robustness.
Fig. 4.1 and 4.2 show the results. Together with the input signal, the channel analog and the digital outputs are shown.
Note the effect of event-triggered reset on output signals. This evident spread in reset time ($\simeq$ 25 ns) is justified by reset time constant variation (passive RC net) due to CMOS process variations. This variation is not critical, since the output signal does not contain any information in the time duration. On the contrary, the trailing edge is very precise through simulation corners, with a 6.2 ns maximum spread.
In Tab. 4.1 the main GEMINI performance has been shown.

Parameter	**Value**
CMOS Technology	AMS IBM 180 nm
# of Channels	16
Max. Pixel Capacitance	40 pF
Max. Count Rate	5 Mcps
Sensitivity	2.5 fC
Power Consumption	2.7 mW/ch (With LVDS Driver: 10.7 mW/ch)
Analog Outputs	Preamp Output (for each channel)
Digital Outputs	LVDS Event Detection (for each channel)
Max. Digital Output Jitter	6.2 ns
Q-V Gain	1 mV/fC
Dynamic Range	From 30 fC to 500 fC
CSP Common Mode Voltage	1 V
Reset Mode	Event-Triggered or External

Table 4.1: GEMINI Performance

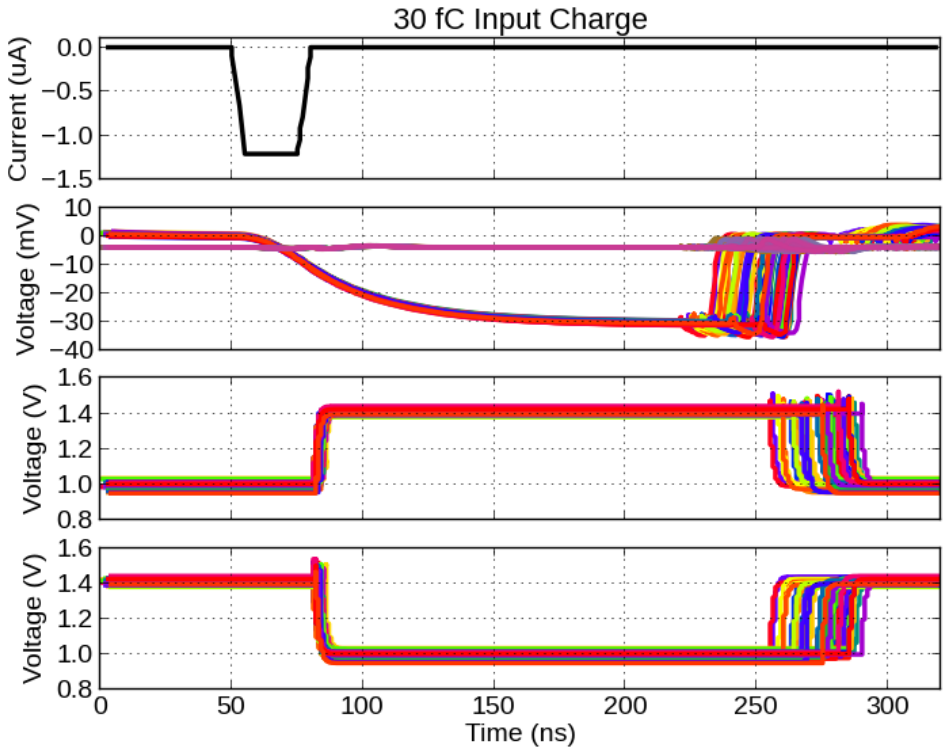

Figure 4.1: Post-Layout Monte-Carlo Simulation Results (30 fC input charge)

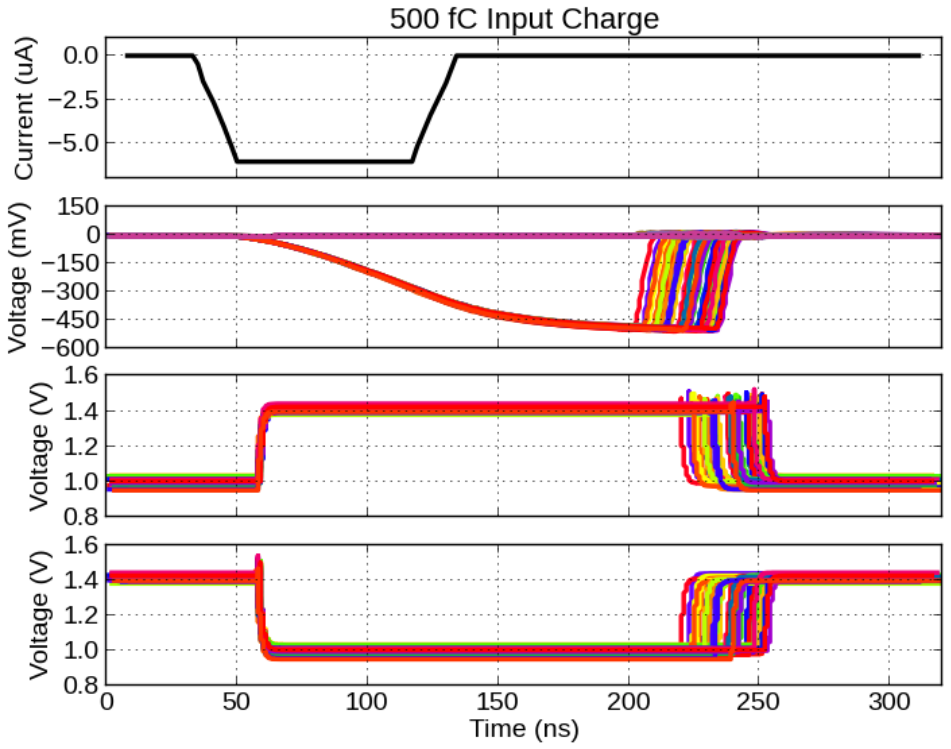

Figure 4.2: Post-Layout Monte-Carlo Simulation Results (500 fC input charge)

Package Datasheet