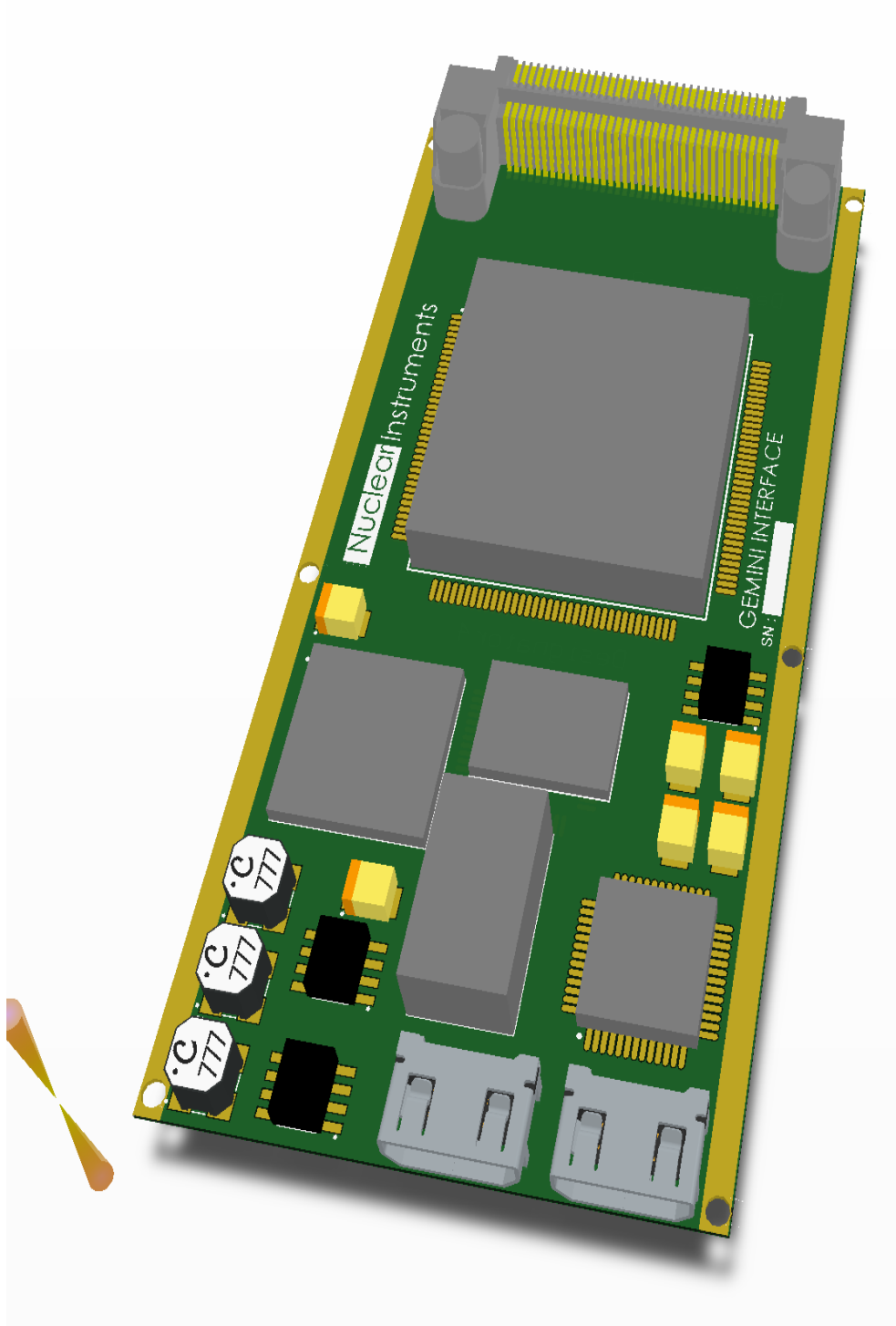
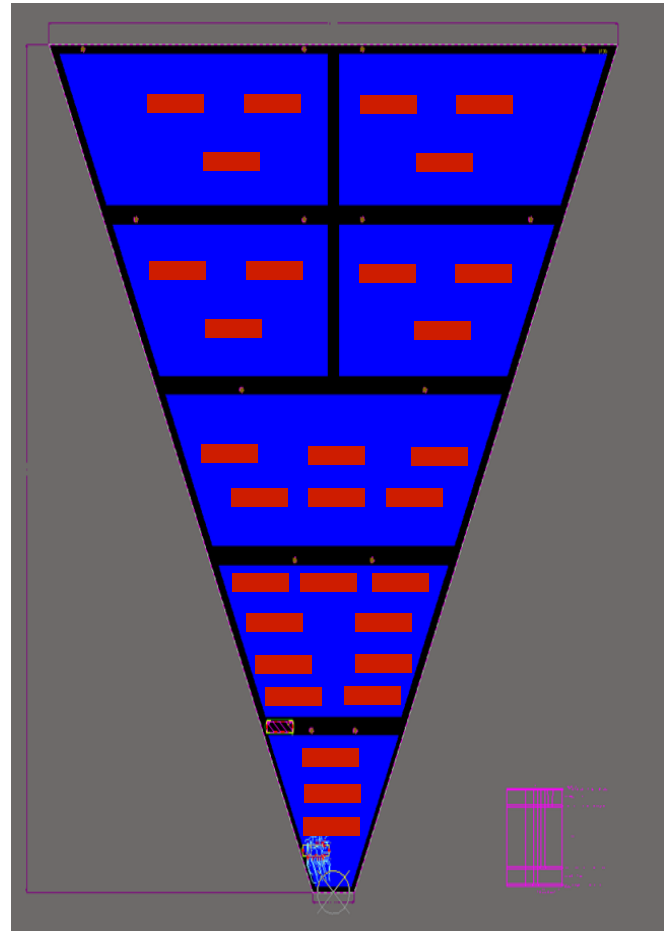
EUROPEAN SPALLATION SOURCE

Band-GEM Readout Meeting

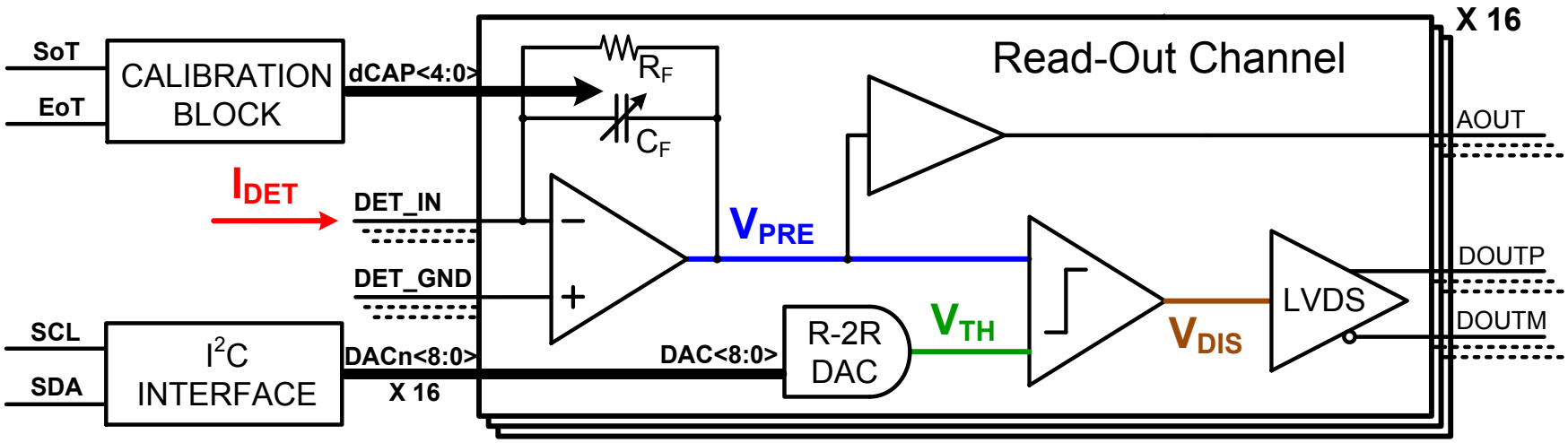
Milan-ESS Meeting
11th April 2017

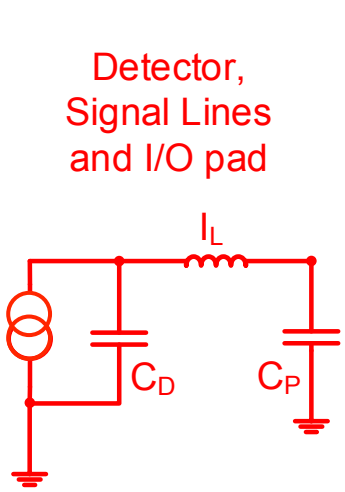

Nuclear Instruments
GEMINI INTERFACE
SN :

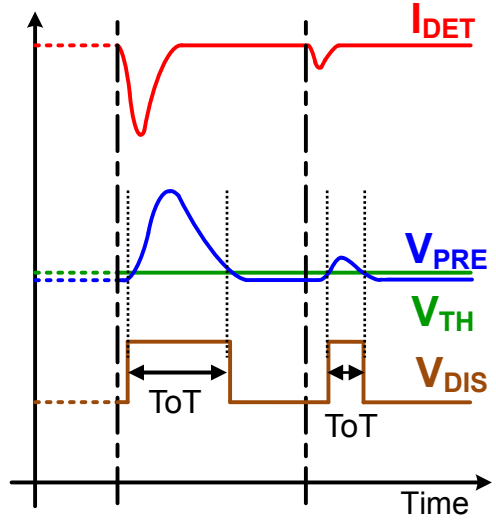
- 32 channels board
- 29 devices per Slice of the detector (261 total)
- Small FPGA with ethenet connectivity on shared cable
- Integrated 1 Gbps switch for deisy chain connection
- Power supply, connectivity and syncronization on the same cable.
- Possibility to distribute the number of board in daisy chain to optimize the bandwidth

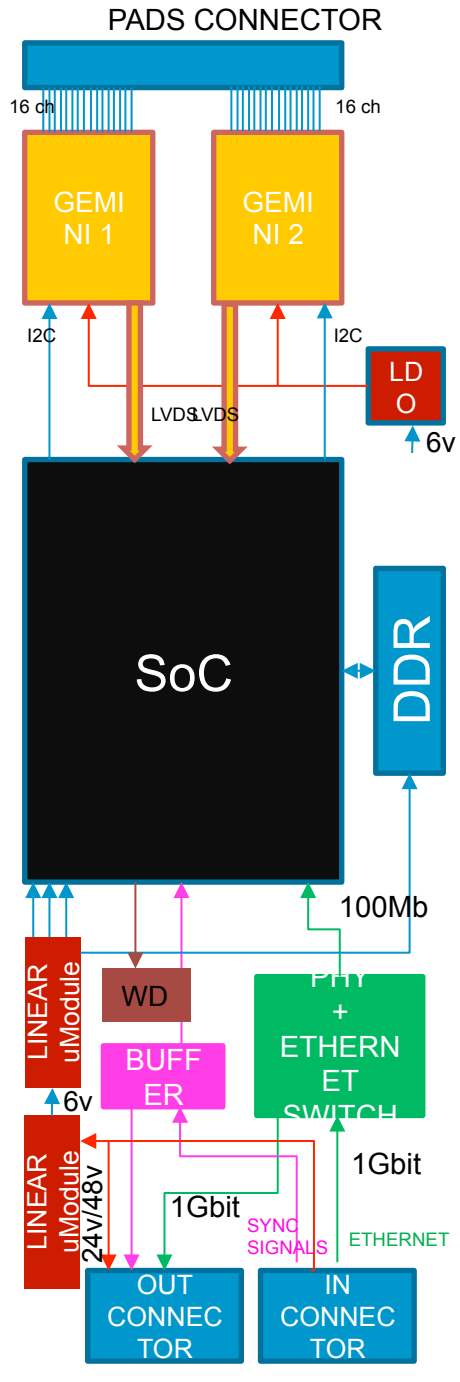


The GEMINI chip: brief reminder









Power Supply:

- Input voltage: 24/48 V to limit current in cables
- Switching LT Power uModule to convert from input voltage to 6V
- 6V rail power a secondary LT uModule to create FPGA and memory voltages
- Ultra low noise LDO to power Gemini Chip

SoC:

- Preferred: SmartFusion 2
  - Extremely Low Power
  - No external flash required
- Alternative: Zynq 7020 (actual board is using Zynq)

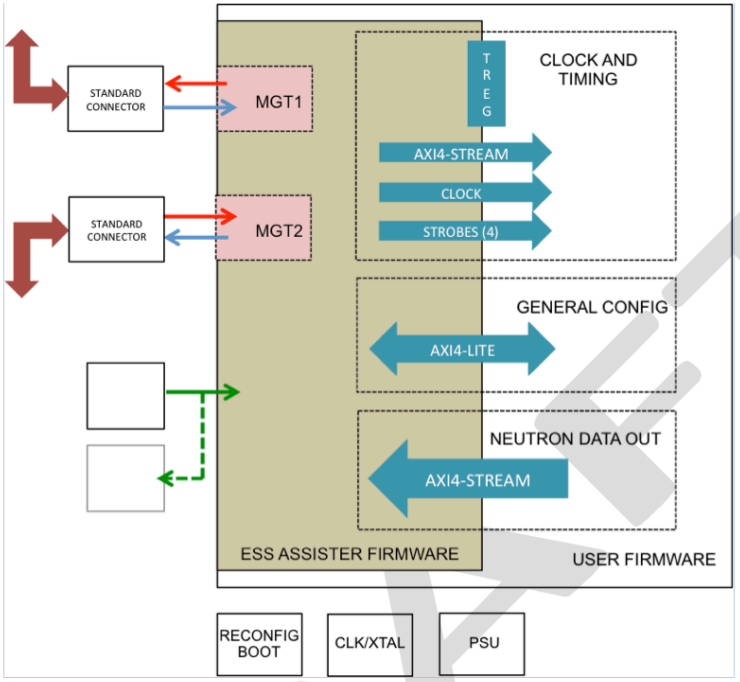
Key Questions

- 32 Channels per board/FPGA. Would 64 channels work?
  - Geometry
  - Pin connections (does Gemini have to be differential out)
  - Data rate/bandwidth
- ESS has a standard analogue connector for it's generic front ends
- Gemini chip, revisions, still as described last year? No chips to ESS?
- Desired level of integration??

  Full integration to front end, run assister firmware etc.

  Module integration, bridge for each octant

  System level integration, bridge at master.



Summary of Meeting

To be compiled during the meeting....