In-Kind Contribution

Radiofrequency Local Protection System (RF-LPS)

AIK 8.4

Signal Conditioning Boards for

RF-LPS of Medium Beta Linac

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SUMMARY

This Critical Design Review data package contains the documents, descriptions and designs for the Signal Conditioning Boards (SCBs) for Radiofrequency Local Protection System (RF-LPS) of Medium Beta Linac (Figure 1).

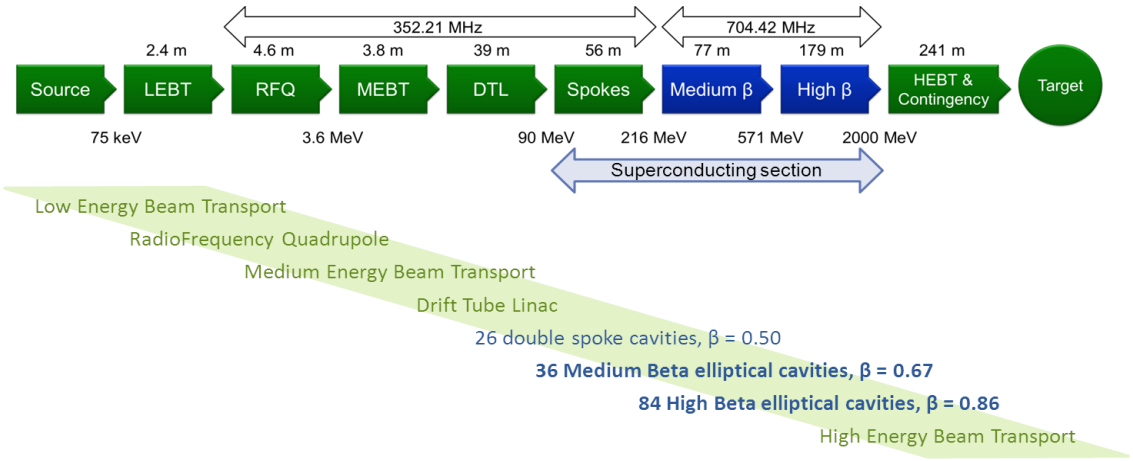

Figure 1 The linear accelerator of ESS ERIC.

The data package shall include but not be limited to (Schedule 4.4.2) [1]:

- System Requirement Document,
- System Design Description and related documents and data (drawings, general arrangement drawings, P&ID, FE models, etc),
- Updated Interface Control Documents,
- System Integration Plan,
- Component Operation and Maintenance Manual,
- System Verification Plan,
- Plan for sustainable selection of materials,
- Documentation to initiate a competitive tender for the procurement of the facility element and to support the project activities,
- Complete documentation package for the procurement of the facility element including as a minimum a statement of work, manufacturing follow-up description, applicable and reference documentation,
- Project Schedule for construction,
- Risk register.

The procedure and timetable before the CDR (Schedule 4.3.3) [1]:

- CDR documents listed above shall be submitted 4 weeks before the review.
- Written comments of the review board, 3 working weeks before the review.
- Written answers to the board, 1 working week before the review.
- Agenda of the review meeting, 1 week before the review.

Documents created during the CDR:

- Report on the review process and decision.

1. SCOPE

1.1. IKC Agreement

MTA Atomki shall provide

- ESS type interlock and control system Medium beta linac
- ESS type interlock and control system High beta linac

This overall contribution is set to the ESS Cost Book value of2200 k€. 120 interlock systems will be needed, to the total cost of2200 k€. These will be used for the medium and high beta sections of the linac. (Schedule 4.1) [1]

The expected results of AIK 8.4 project are: medium beta and high beta interlock systems for the local protection of radiofrequency unit. This should be considered as an in-kind contribution of Government of Hungary to ESS in its construction phase, realised by MTA Atomki. According to the In-Kind Contribution Agreement, MTA Atomki alone has the full technical, financial and commercial responsibility towards ESS ERIC for the performance of the Agreement (IKC Agreement, page 1, paragraph G) [1].

MTA Atomki is an academic research institute, its main profile are research and development. After the acceptance of the developed systems, the altogether 120 interlock systems to be delivered to ESS site will be manufactured by a subcontractor. MTA Atomki is fully responsible for the compliance with the In-Kind Contribution Agreement by all of its subcontractors (IKC Agreement 16.2.2) [1].

1.2. Reviews during the project

The reviews shall be organized as defined in the ESS Design Review Standard Operating Procedure. (Schedule 4.3.3 and 4.3.4) [1]

The process, inputs and outputs of CDR and next reviews focusing on the Signal Conditioning Boards are summarized in Table 1.

The Critical Design Review (CDR) assesses if the design meets all facility element requirements with acceptable risk and within the cost and schedule constraints. The CDR demonstrates that the maturity of the design is appropriate to support proceeding with full-scale fabrication, assembly, integration, test and future operation and decommissioning. (Schedule 4.3.3) [1]

The Factory Acceptance Test (FAT) is performed at the vendor prior to shipping to a client. The vendor tests the system in accordance with the clients approved test plans and specifications to show that system is at a point to be installed and tested on site.

The System Acceptance Review (SAR) examines the facility element and its documentation, and inspection, demonstration, test data and analyses that support its verification as defined in the Verification Plan and Report. The SAR ensures that all the system requirements have been satisfied and that the integration activities of the facility element can start as defined in the facility element Integration Plan. (Schedule 4.3.4) [1]

The SAR shall be organized by ESS ERIC and will involve program members of the partner as well as any other stakeholders at the discretion of the review chairman. The chair of the review board is appointed by ESS ERIC. The membership of the board is communicated to the review participants at the earliest possible time. (Schedule 4.3.4) [1]

The successful completion of the SAR is a prerequisite for crediting values to MTA Atomki. (Schedule 4.3.4) [1]

1.3. Critical Design Review

A Critical Design Review (CDR) is a multi-disciplined technical review to ensure that a system can proceed into fabrication, demonstration, and test and can meet stated performance requirements within cost, schedule, and risk. Soon after the CDR the serial production can start.

The purpose of this data package is to collect all the information concerning the Signal Conditioning Boards to prove that both Analogue Conditioning Board (aCB) and Digital Conditioning Board (dCB) satisfy the requirements taking into account the ESS standards and are ready to serial production.

Table 1 The process, inputs and outputs of CDR and next reviews focusing on the Signal Conditioning Boards of Medium Beta section.

Initial step		Design and prototype of Signal Conditioning Board	Stage 1 Development phase
CDR 2017-06-28	Input	Signal Conditioning Board design, prototype and documentation	
	Process	Critical Design Review of Signal Conditioning Board Examination: the prototype works according to the requirements and the documentation is correct Place of review: ESS	
	Output	Acceptance or rejection of the system	
Next step		In case of rejection: modifications shall be made	
		In case of acceptance: production can start	Stage 2 Production phase
FAT 1 2017 Nov	Input	Signal Conditioning Board (1-8 units) and documentation	
	Process	Factory Acceptance Test of Signal Conditioning Board (1-8 units) Examination: the units work according to the requirements and the documentation is correct Place of review: Hungary	
	Output	Acceptance or rejection of the units	
Next step		In case of rejection: fix or new units shall be manufactured	
		In case of acceptance: the units shall be delivered to ESS site	
FAT 2 2018 Feb	Input	Signal Conditioning Board (9-16 units) and documentation	
	Process	Factory Acceptance Test of Signal Conditioning Board (9-16 units) Examination: the units work according to the requirements and the documentation is correct Place of review: Hungary	
	Output	Acceptance or rejection of the units	

Next step		In case of rejection: fix or new units shall be manufactured	
		In case of acceptance: the units shall be delivered to ESS site	
FAT 3 2018 May	Input	Signal Conditioning Board (17-24 units) and documentation	
	Process	Factory Acceptance Test of Signal Conditioning Board (17-24 units) Examination: the units work according to the requirements and the documentation is correct Place of review: Hungary	
	Output	Acceptance or rejection of the units	
Next step		In case of rejection: fix or new units shall be manufactured	
		In case of acceptance: the units shall be delivered to ESS site	
FAT 4 2018 Aug	Input	Signal Conditioning Board (25-36 units) and documentation	
	Process	Factory Acceptance Test of Signal Conditioning Board (25-36 units) Examination: the units work according to the requirements and the documentation is correct Place of review: Hungary	
	Output	Acceptance or rejection of the units	
Next step		In case of rejection: fix or new units shall be manufactured	
		In case of acceptance: the units shall be delivered to ESS site	
SAR 2018 Sep	Input	Signal Conditioning Board (36 units) and documentation	
	Process	System Acceptance Review of Signal Conditioning Board (36 units) Examination: the system works according to the requirements and its documentation is correct Place of review: ESS	
	Output	Acceptance or rejection of the system	
Next / Last step		In case of rejection: fix the problem	
		In case of acceptance: Final Report and project closing	End of project

1.4. Task of MTA Atomki

Stage 1 of the contribution is the detailed design and engineering phase that prepares for and precedes potential procurement of the facility element. Within Stage 1 the design is detailed and verified by way of analysis and/or test down to the lowest level selected by MTA Atomki. (Schedule 4.2.1) [1]

Stage 1 starts upon successful completion of Preliminary Design Review of the facility system and ends with the successful completion of the Critical Design Review (CDR). (Schedule 4.2.1) [1]

Stage 1 is performed by ESS ERIC and MTA Atomki. MTA Atomki provides support for the exploratory work of the design of the prototype interlock system. Two experienced developers (PLC and LabView/FPGA) are assigned for on-site work at ESS. The resulting design and documentation will be transferred to MTA Atomki to continue the work on Stage 2. (Schedule 4.2.1) [1]

All partner national safety laws and legislation applicable to the design, development, manufacturing, installation, testing and operation of the supply shall be followed and fulfilled.

All operator national safety laws and legislation applicable to the design, development, manufacturing, installation, testing and operation of the supply shall be followed and fulfilled as defined in the requirement document for the facility element by ESS ERIC. (Schedule 5.5.1) [1]

Both MTA Atomki and ESS ERIC shall implement and maintain throughout the project a quality assurance and safety approach that covers all relevant aspects of ISO 9001 with respect to the scope of the IKC delivery and all specified reliability, quality assurance and safety requirements. (Schedule 5.5.1) [1]

The ESS programme participants shall develop the baseline [2] of the facility elements and is free to redefine the architecture of the facility elements. Full and part delivery milestones should be under change control. This means that both ESS ERIC and MTA Atomki need to agree on changes to the milestones. Each baseline change shall be documented as defined in the ESS Change Control Process. (Schedule 5.3) [1]

ESS ERIC and MTA Atomki agree that they shall share the risk associated with developing new technology (i.e., the risk that a solution required under the scope of works is not technically feasible). If such a risk materialises, this shall not be considered a defect, difference or non-compliance if MTA Atomki so notifies ESS ERIC prior to the delivery of the relevant project results. Together with any such notification, MTA Atomki shall submit evidence of the non-feasibility to ESS ERIC and they shall jointly find an alternate solution which in its technical, economic and other effects shall be as close as possible to the solution required under the scope of works and negotiate the arrangements required to implement such solution. (IKC Agreement 7.4.3) [1]

1.5. History

MTA Atomki made a lot of effort to develop an Interlock System consisting of a SIM (Slow Interlock Module) and a FIM (Fast Interlock Module) unit. SIM is based on Siemens platform and FIM is based on National Instruments cRIO platform. However, ESS ERIC made a decision that the required platform is MTCA (Micro Telecommunications Computing Architecture) and started their own development without MTA Atomki.

Because the real instrument (klystron) to be protected has not been available for a long time, MTA Atomki decided to develop simulators:

- a SIM simulator based on Siemens platform and
- a FIM simulator based on National Instruments PXI platform.

At the end, MTA Atomki got the task to develop Signal Conditioning Boards, analogue and digital (aCB and dCB) with the lead and closed co-operation of RF Group of ESS ERIC.

2. SIGNAL CONDITIONING BOARDS

2.1. Role of Signal Conditioning Boards

All field devices that provide physical (analogue and status) signals shall be connected to Integrated Control System devices so that the signals can be accessed by/through the control and the Local Protection Systems called Interlock Systems.

In electronics, signal conditioning means manipulating a signal in such a way that it meets the requirements of the next stage for further processing. Generally, the signals coming in and out from and to the field devices should be conditioned before those are connected to the Interlock Systems. We handle the analogue and digital signals separately therefore we developed Analogue and Digital Conditioning Board.

Technically, the main functions of Analogue and Digital Conditioning Boards - together Conditioning Box (CB) - can be summarized as follows:

- Based on the specifications the field devices convert, filter-out, translate both analogue and logical signals in a way which will result correct matching of the signals between the inputs and outputs of the systems connected in chain.

- The grounding policy is one of the most important issues in such an environment which is characterized by electromagnetic noise generated with high frequency and is electrically harsh enough due to the power.

- The electronics of the CB should be robust and immune against the electromagnetic noise coming from the environment. The ground loops are avoidable by using de-couplers, optical isolators.

- The logic implemented in the CB must be always simple and reliable in this way guarantee the requested safety.

2.2. Initial parameters and instructions

The experts of RF Group were intended to collect all technical details, requirements necessary for development of CB by participating regular meetings organised at ESS by different sections. The initial parameters and instructions were transferred from RF Group to Atomki in several turns and a lot of discussions were needed to clarify the requirements. For details see:

- **Annex 01 FIM conditioning board requirements**

2.3. Added value

The main role of Atomki was to prove and prototype the concept of the electronics and inspect the parameters and features of the design.

The preparation phase of the design was demanding and hard in terms of daily collaboration between the partners because of the missing exact technical information for the final solution.

The difficulties resulted from the nature of the present discovery research was fully understandable, but it caused a lot of troubles.

The added value of Atomki in terms of intellectual properties can be summarized as follows.

- Based on the expertise earned during previous projects, Atomki was capable to design and develop the electronics suitable to solve both analogue and digital signal conditioning.

- Experts of Atomki were ready and open to except ideas coming from other groups working on the same accelerator project but with different tasks to be solved.

- Atomki succeeded to establish fruitful relationship with ESS Bilbao working on warm part of the LINAC, dealing with almost the same tasks for Radiofrequency Local Protection System and Signal Conditioning Box.

- Finally Atomki created a good atmosphere together with colleagues of Power Converters Section of ESS, in this way we have opportunity to get real information from the RF key systems like modulator, klystron and related electronic devices to be protected.

3. SYSTEM REQUIREMENT DOCUMENT

As information for system requirement, the following documents were taken into account.

- **Annex 02 Technical report for linear technology RF detector LTC5530 and ADL5513**
- **Annex 03 ESS DIO Conditioning Board Hardware Manual**
- **Annex 04 RF detector - Interface between coupler and interlock**

4. SYSTEM DESIGN DESCRIPTION AND RELATED DOCUMENTS AND DATA

As information for system design description, the following documents were taken into account.

- **Annex 05 DIO_3118 Digital-IO Generic FMC**
- **Annex 06 DIO_3118 Proposal for Digital-IO Generic FMC**
- **Annex 07 DIO3118 SDR Input Connector**
- **Annex 08 DIO3118 SDR Output Connector**
- **Annex 09 External connectivity of the Klystron Modulator**
- **Annex 10 ADC_3117 High-Density ADC FMC Technical Specification**
- **Annex 11 Toshiba State Machine FIM**

5. UPDATED INTERFACE CONTROL DOCUMENTS

As information for updated interface control, the following documents were taken into account.

- **Annex 12 Digital isolation test report**
- **Annex 13 Technical report of the mother board plus daughter board**

6. SYSTEM INTEGRATION PLAN

System integration is defined in engineering as the process of bringing together the component sub-systems into one system (an aggregation of subsystems cooperating so that the system is able to deliver the overarching functionality) and ensuring that the subsystems function together as a system, and in information technology as the process of linking together different computing systems and software applications physically or functionally, to act as a coordinated whole. (Source: Wikipedia)

The Signal Conditioning Box is a passive electronic device in that sense it does not contain any controller, embedded unit to be integrated. It is dedicated to interface analogue/digital, input/output signals between FIM/SIM interlock and field devices (klystron, modulator, LLRF, PIN DIODE, voltage, current, pressure and temperature sensors etc).

However, FIM/SIM interlock systems have to be integrated into one global system. As information for system integration plan, the following documents should be taken into account.

- **Annex 14 Fast Interlock Module LEP Klystron**
- **Annex 15 ICS Handbook**
- **Annex 16 Slow Interlock Module CERN**

7. COMPONENT OPERATION AND MAINTENANCE MANUAL

As we are in prototyping phase and some changes are expected to be made after the CDR, component operation and maintenance manual is not completed.

8. SYSTEM VERIFICATION PLAN

8.1. General considerations

Verification is intended to check that a product, service, or system (or portion thereof, or set thereof) meets a set of design specifications. In the development phase, verification procedures involve performing special tests to model or simulate a portion, or the entirety, of a product, service or system, then performing a review or analysis of the modelling results. In the post-development phase, verification procedures involve regularly repeating tests devised specifically to ensure that the product, service, or system continues to meet the initial design requirements, specifications, and regulations as time progresses. It is a process that is used to evaluate whether a product, service, or system complies with regulations, specifications, or conditions imposed at the start of a development phase. Verification can be in development, scale-up, or production. This is often an internal process. (Source: Wikipedia)

Each Conditioning Box for Medium Beta interlock system (36 units) will have its own identification number. This ensures that all the individual units are identifiable, their characteristics and test results are traceable in the relevant documents.

The condition and technical features of the produced units will be checked at the appropriate level (visual inspection, simple test measurement and complete test measurement) before and after critical actions (e.g. before and after delivery, before installation) and in case of suspected damage.

Nonconforming or damaged products will be separated and their status recorded in the relevant document. The actions depend on the level of failure: fix, replace with supplementary unit or produce new units. All the corrective actions taken and the results will be recorded in the relevant document.

FAT and SAR are planned according to Table 1 (page 6).

8.2. Technical aspects

The klystron is a radiofrequency (RF) amplifier that works at high power levels. Although it can be safely operated, care must be taken in order to avoid possible hazards caused by unexpected conditions, such as currents and voltages exceeding the absolute ratings. In most applications an interlock unit is employed to stop the machine before it can cause harm to its operator or damage itself. An interlock system is an automatic device used to prevent undesired states in electrical, electronic, or mechanical instruments. The main objectives of interlock systems are continuously check the sensors that monitor the klystron state and report anomalous conditions to the integrated Interlock Network.

The interlock systems can be implemented in different ways. One of the possible solutions of the electronics for the klystron amplifier and related electronics is implemented in hardware on printed circuit boards. Indeed, the timing specifications and the need of a reliable system forbid any software solution, including real-time platforms. Moreover, even if implementation based on Field Programmable Gate Arrays (FPGA) could be considered, the klystron provider suggested the use non-volatile, non-programmable hardware. This type of interlock can be considered as a hard wired unit dedicated to prevent the field devices connected directly to the system. The system flexibility is minimal built into this kind of solutions, and not even satisfying when the technical parameters of the field devices have been changed slightly.

The other, completely novel method applied in construction of interlock systems is implemented in real-time based fast computer like MicroTCA.4 system. This system is equipped with all necessary resources which can easily cover any demands aimed by the protocol of the field devices, like klystrons.

This solution is far not a riskless option. The only benefit that can be mentioned is the excellent flexibility of the platform in terms of hot reconfiguration capability of the system in case of any changing in the technical parameters.

In the final version of the interlock system ready for serial manufacturing the arguments mentioned before must be taken into account with the highest priority.

Regarding the Signal Conditioning Boards the solution has to be realised in a way to fulfil all the system requirements with the maximal flexibility versus minimal complexity. In this field of business by law, the simplest solution is the best one.

9. VERIFICATION OF SIGNAL CONDITIONING BOARD PROTOTYPE

The functional and parametric tests of the SCB prototype were performed without connecting to real environment as the devices to be connected to each other via the Signal Conditioning Board, were not available.

9.1. Electronics for digital input channels

The main technical requirements on digital input channels of dCB are the noise immunity, overvoltage protection and low pass filtering for attenuation of RF environment and picked-up noises. The components used for satisfying these requests are the arresters, clamping-diodes and the passive low pass RC filters. The applied input topology of the electronics is symmetric which implements an excellent common mode noise rejection.

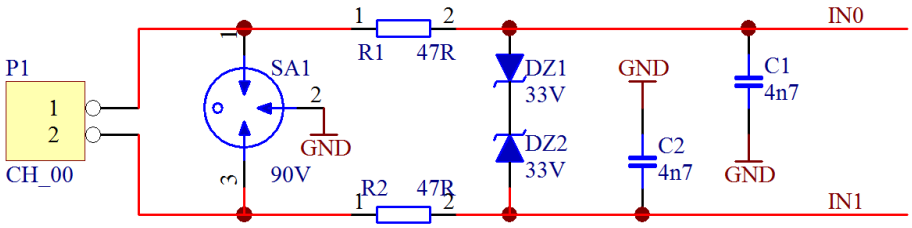

Figure 2 First stage of digital input cannels equipped with overvoltage protection and low pass filtering for attenuation of RF noises.

The circuits following the passive input protection stage is created for having enough flexibility for conditioning of commonly used digital signals driven by the field devices. The digital input channels are capable to receive +5 V or +24 V voltage standards for that the jumper gives opportunity to select the present, required standard. The LED based optical coupler is used for separation of grounds on different sides and a PCB mounted indicative colour LED gives information about the status on the input line. Both the LED and the open collector output stage are driven by the widely used powerful line driver with 300 mA driving capability.

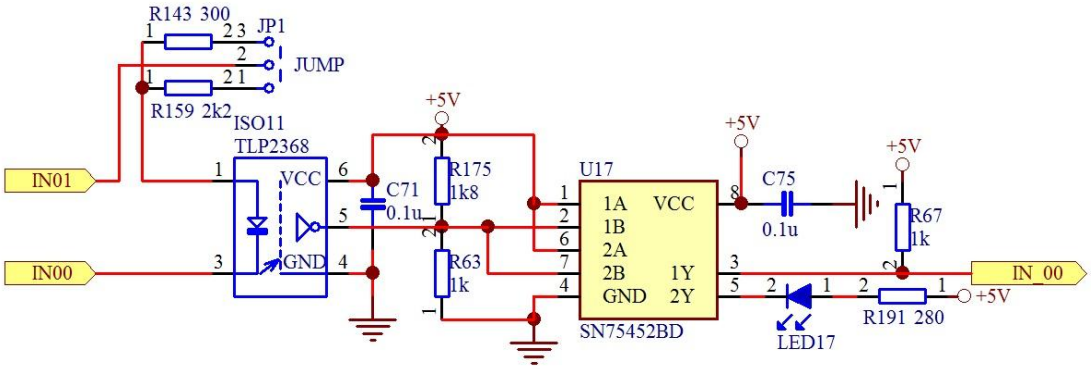

Figure 3 Circuit of an open collector output stage on input channels with LED based opto-coupler for isolation.

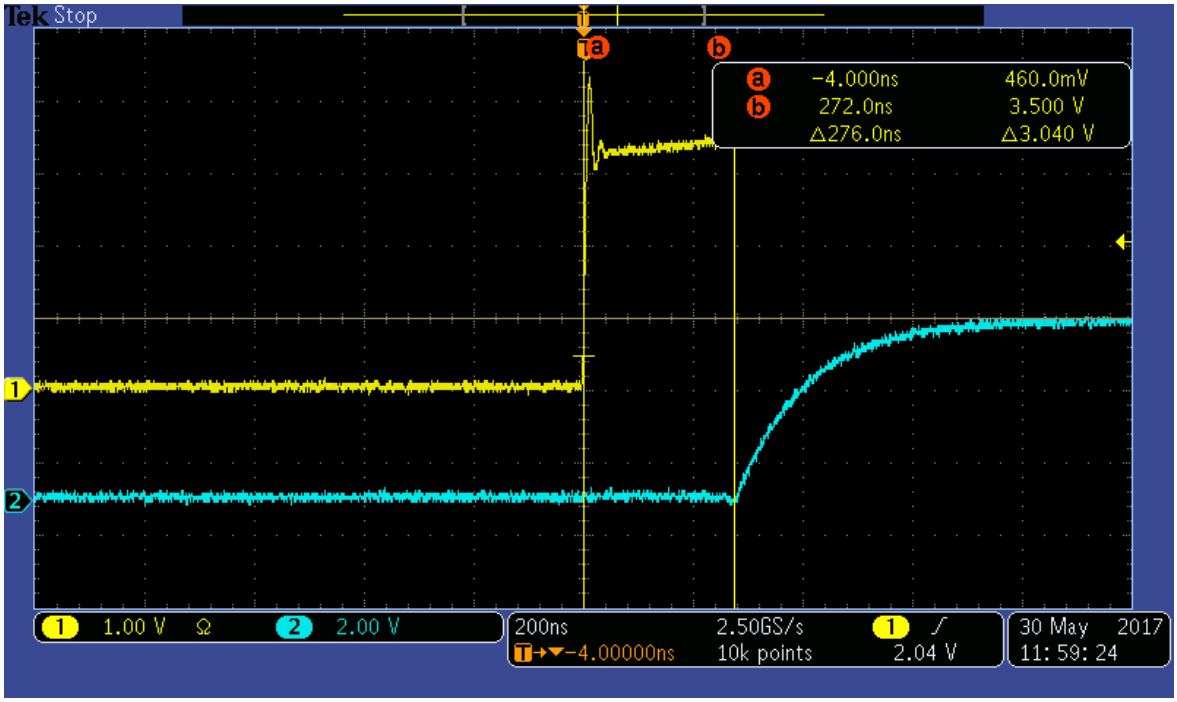

Figure 4 Oscillogram presenting 276 ns propagation delay of digital input channel at Low to High transient. The yellow curve represents the input and the blue is the output signal.

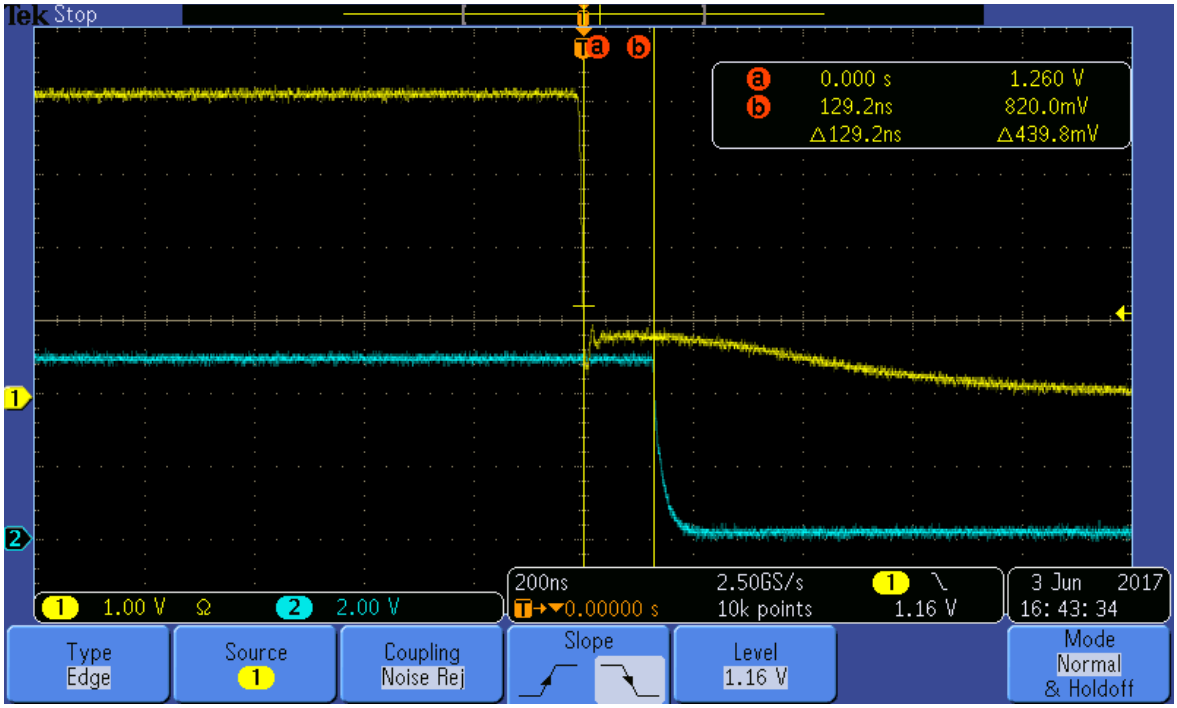

Figure 5 Oscillogram presenting 129 ns propagation delay of digital input channel at High to Low transient. The yellow curve represents the input and the blue is the output signal.

9.2. Electronics for digital output channels

Electronics dedicated for digital signal conditioning of output channels of the field devices (direction from MicroTCA to field devices) are consolidated in terms of requirements demanding the protocols, logics used (positive or negative) and the propagation delays caused by the components applied.

The circuit diagram in Figure 6 is constructed to convert, isolate MicroTCA, TTL control signals to the outputs using fast drivers with open collector outputs. The PCB LED indicators used for fast tracking of the output states are also mounted. The additional benefit of the LED lights is to make possible the easy trouble shooting.

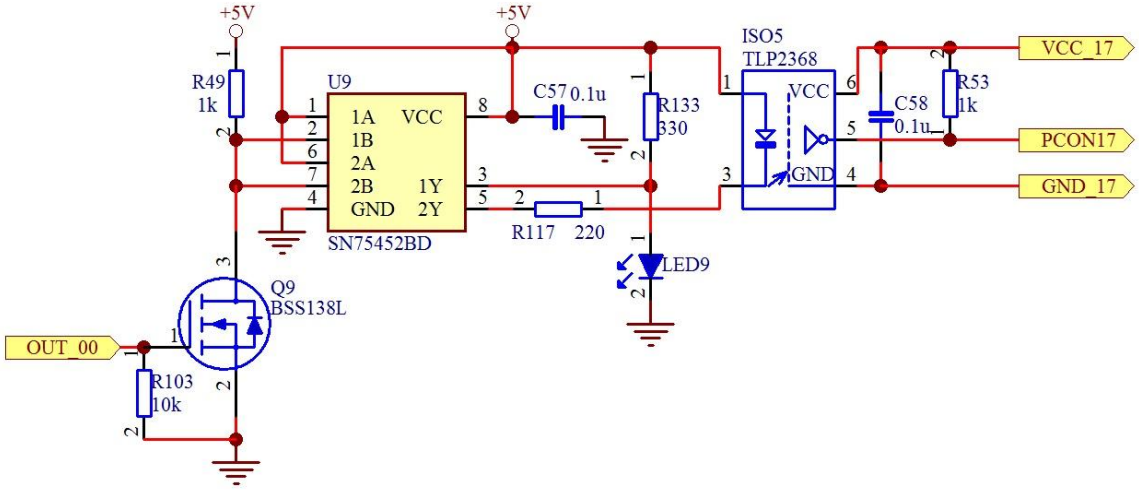

Figure 6 Typical schematics of output channels having optically isolated open collector outputs.

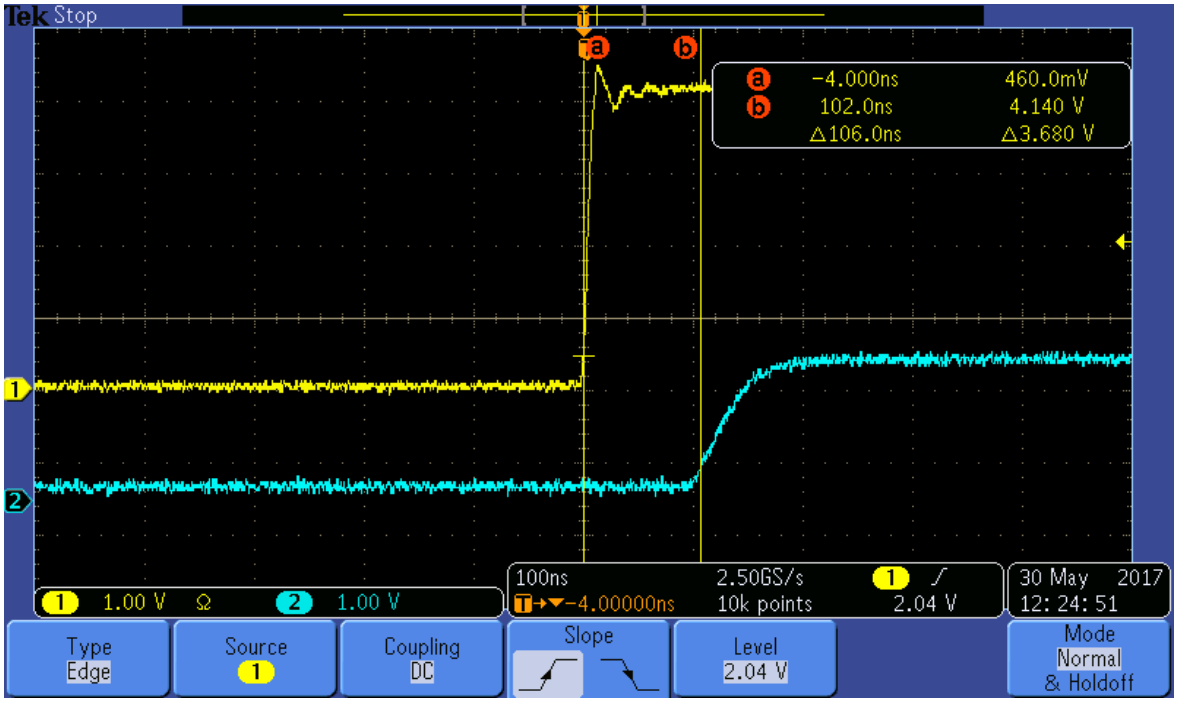

Figure 7 Oscillogram presenting 106 ns propagation delay at Low to High transient of output channel.

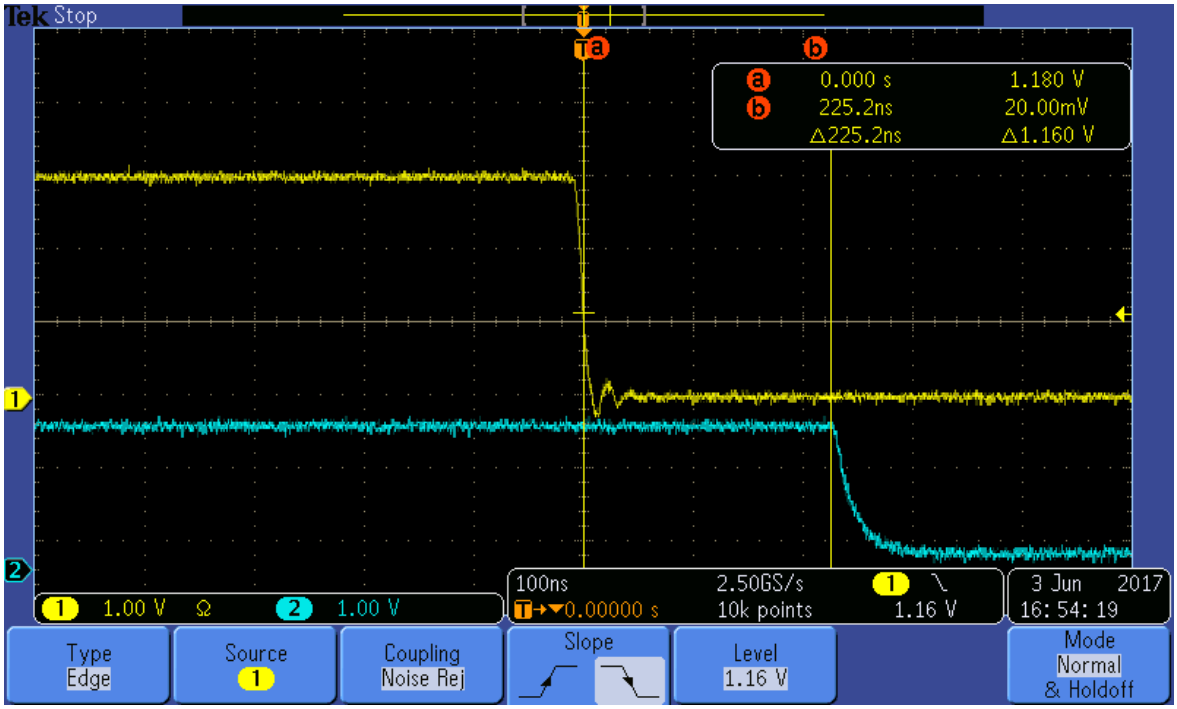

Figure 8 Propagation delay 225 ns observed at High to Low transient of output channel.

The difference between circuits presented in Figure 6 and circuit in Figure 9 is only the end-stage used: instead of open collector driver a full transistor is applied. The solution is frequently used in power inverters for driving the IGBT stages. The IS127 is an optically coupled isolator consisting of an infrared light emitting diode (LED) and a high voltage NPN silicon photodarlington transistor

which has an integral base-emitter resistor to optimise switching speed and elevated temperature characteristics.

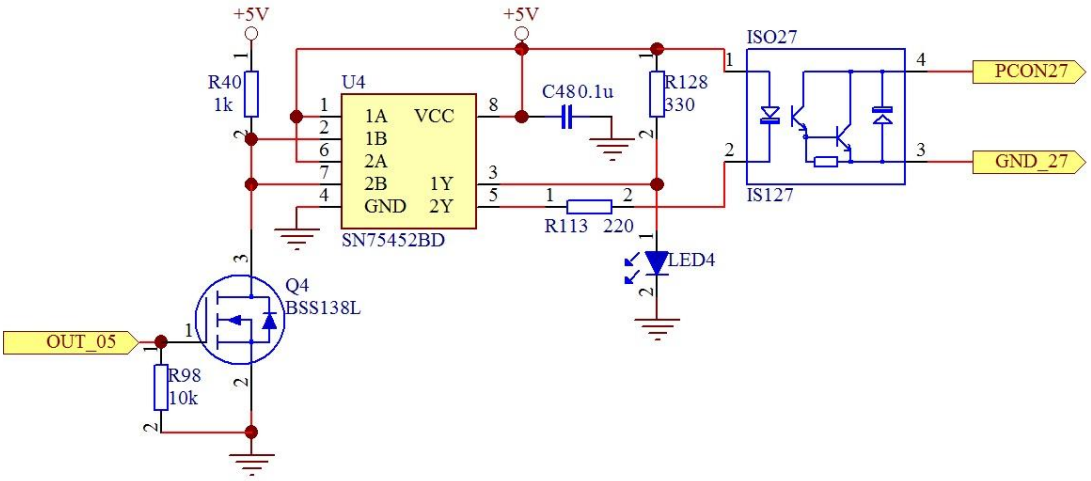

Figure 9 Output channel with high voltage darlington optically coupled isolator.

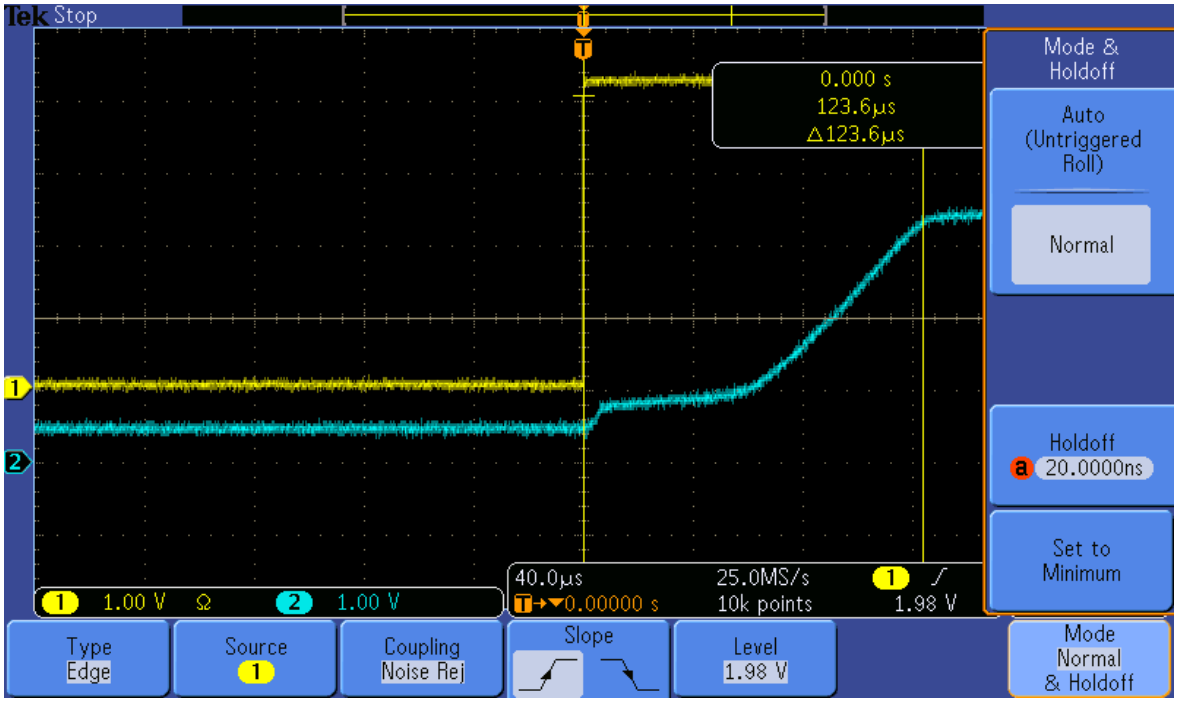

Figure 10 Delay at transient from Low to High.

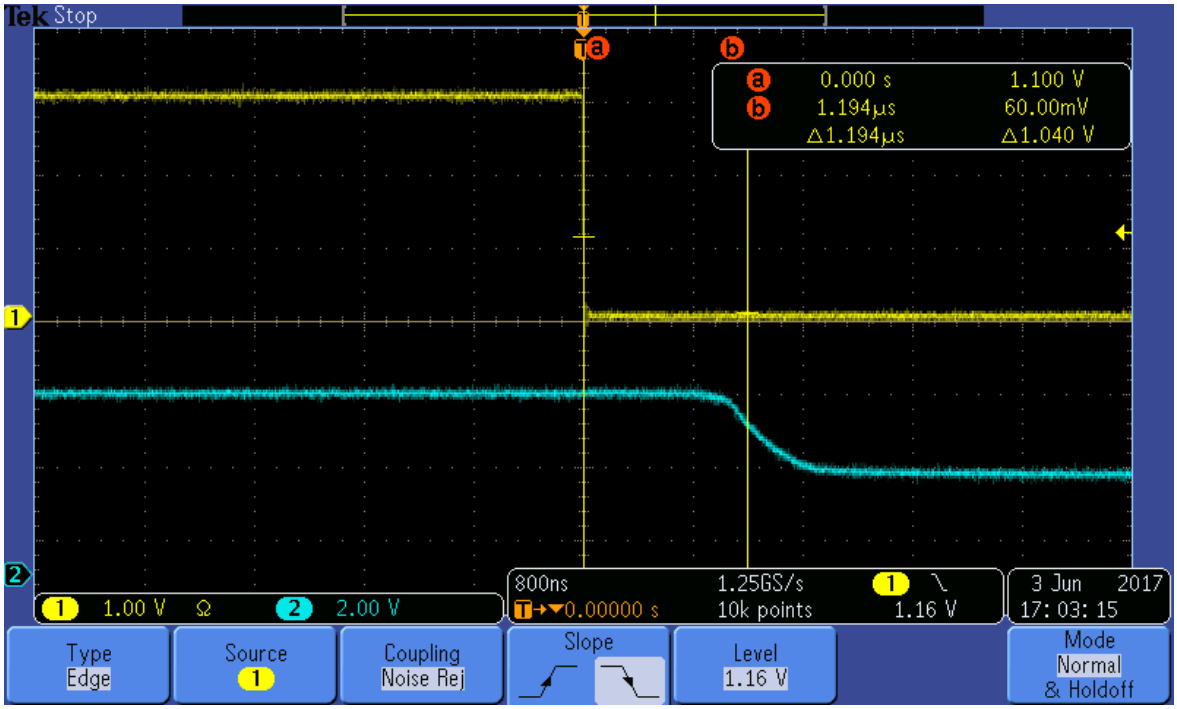

Figure 11 Delay at transient from High to Low 1.568 microsec.

The output channel is dedicated to drive any kind of fibre optic devices having the phase lined control protocol in input and output. The current can be varied by changing the value of the resistor in R141 position. Current flow calculated on the fibre transmitter one can take into account the forward voltage on LED and the power supply. The indicative LED also mounted on the PCB.

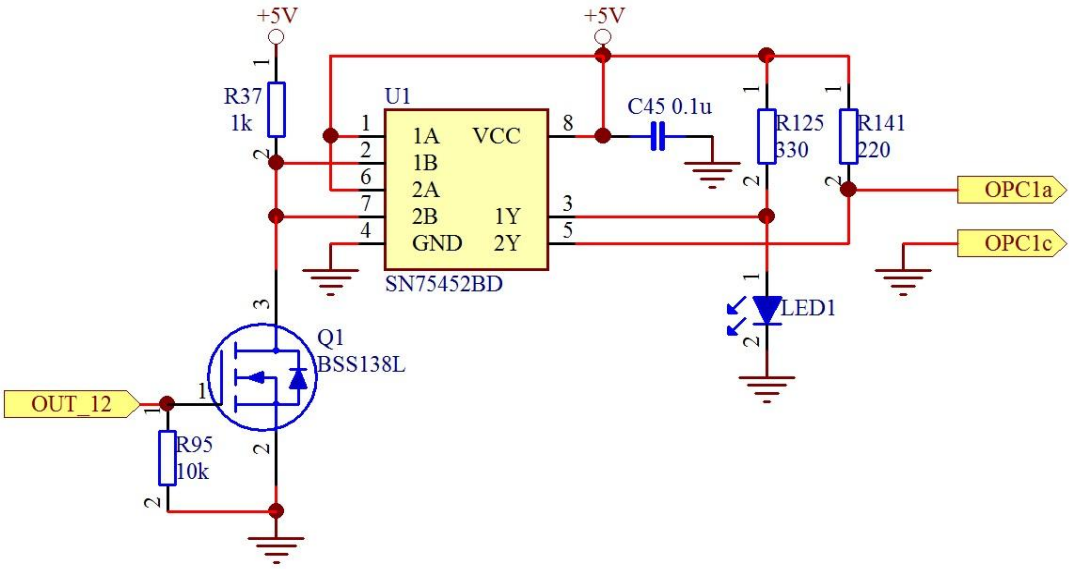

Figure 12 Typical output channel for fibres.

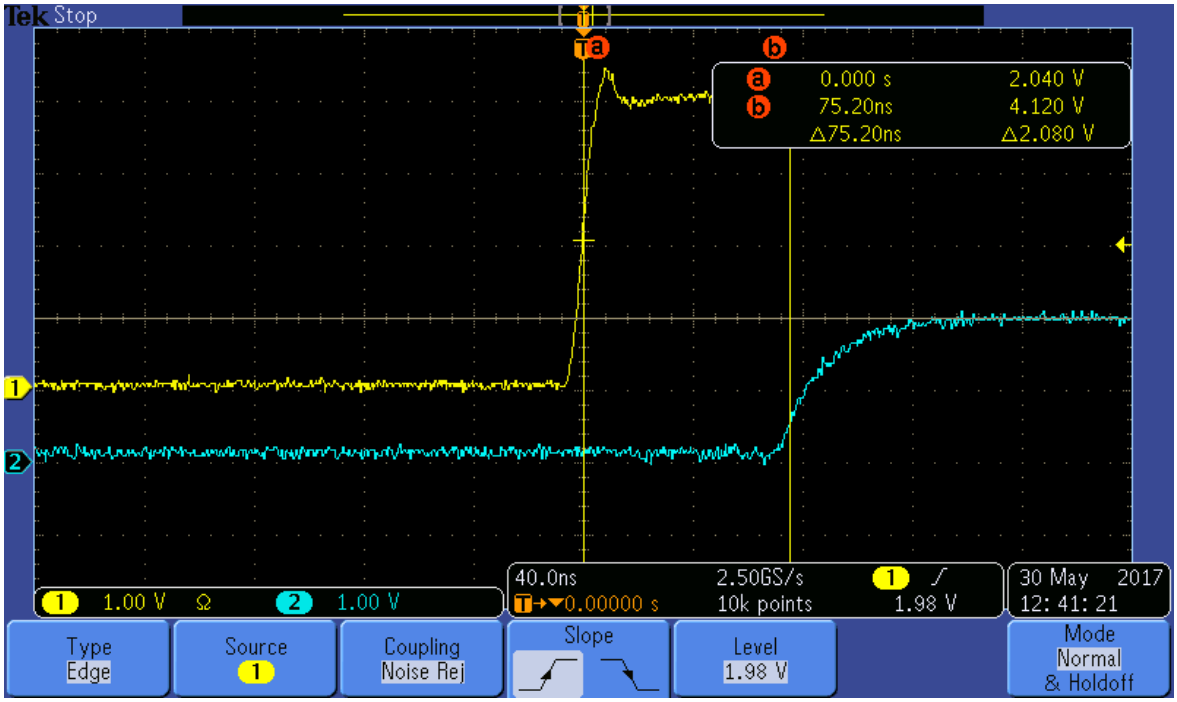

Figure 13 Delay on Low to High transient.

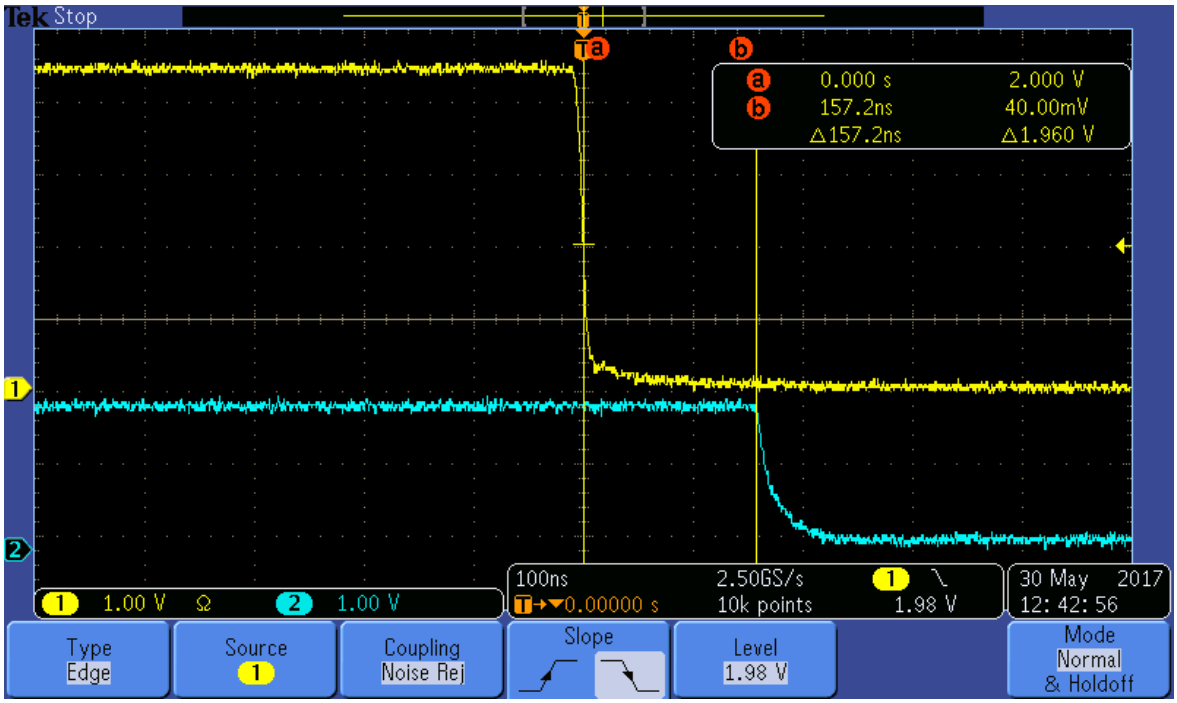

Figure 14 Delay on High to Low transient.

9.3. Electronics for analogue channels

Analogue Conditioning Board is to be used for treating the analogue signals coming from the field devices where the signals monitor the regime of the electronics. Generally, the output signals generated by the sensors of the field devices represent physical values (temperature, pressure, forward and reflected power, voltage, current etc.) with certain levels of analogue voltages and have to be connected to the inputs of Multichannel Analogue Digital Converters (ADC). The ADC inputs should be protected against the electromagnetic noise and also insensitive to the over-voltages coming from the environment, and low pass filtered matching the Shannon law.

At the MicroTCA interface, ADC_3117 is a single with FMC ANCI/VITA57.1 providing twenty (20) DC coupled ADC channels with 16-bit resolution at a sampling rate up to 5 Msps. The conversion signalling can be controlled from the FPGA user application or/and from the front panel connector signalling. The digital back-end interface to the FPGA is implemented with differential LVDS providing optimal noise protection.

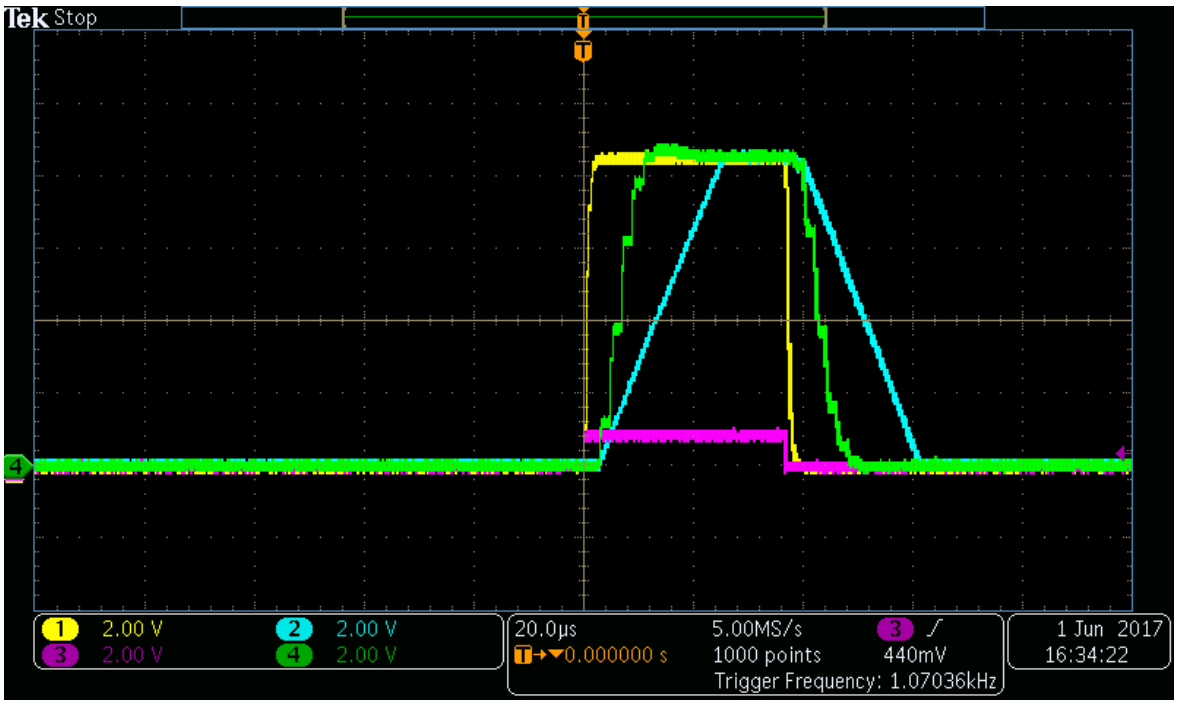

Figure 15 Typical signals extracted from one of the analogue channels at 10 amplification factor.

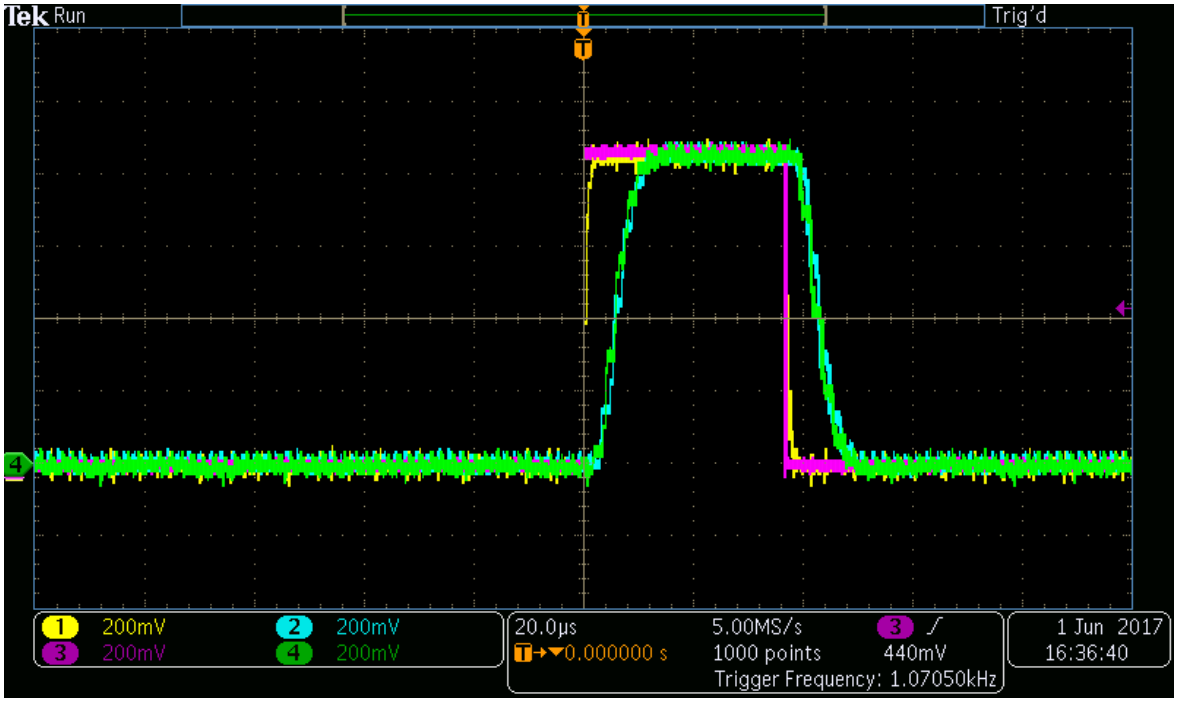

Figure 16 Typical signals extracted from one of the analogue channels at 1 amplification unit.

10. PLAN FOR SUSTAINABLE SELECTION OF MATERIALS

The mechanical and electronic components should be procured from responsible qualified companies to reduce environmental impacts, conserve resources and reduce costs.

When choosing the materials and components, ESS Procedure for Sustainable Selection of Materials [3] will be taken into account.

11. DOCUMENTATION TO INITIATE A COMPETITIVE TENDER

As a basic documentation to initiate a competitive tender for the procurement of the Signal Conditioning Boxes (36 pieces), see

- **Annex 17 Tender document in Hungarian**

12. COMPLETE DOCUMENTATION PACKAGE FOR THE PROCUREMENT OF THE FACILITY ELEMENT

For Medium Beta section of the Linac, 36 pieces of RF-LPS units are needed. Each unit contains SIM, FIM interlocks and SCB. The SCB is detailed below.

12.1. Digital Conditioning Board

The Digital Conditioning Board involves:

- 16-channel LVTTL inputs equipped with protection circuits against sparks, overvoltage, electromagnetic noise
- 1-channel LVDS input for interconnection to LLRF unit
- 10-channel opto-isolated output with TTL driver
- 4-channel opto-isolated output with transistor driver
- 2-channel driver for fibre optic transmission
- 1-channel LVDS output for interconnection to LLRF unit

For detailed schematics of the Digital Conditioning Board, see

- **Annex 18 Digital Conditioning Board**
- **Annex 19 16 Ch LVTTL Input**
- **Annex 20 14 Ch LVTTL Output & 2 Ch Fiber**

Figure 17 Assembled PCB of Digital Conditioning Board.

12.2. Analogue Conditioning Board

The Analogue Conditioning Board involves:

- 10-channel mother board with isolated units including programmable instrumentation amplifier, high precision isolation amplifier and output drivers for monitoring purpose
- 10 pieces of protection daughter card including transient suppressor, low pass filter, protection diodes against overvoltage
- 10 pieces of RF power detector including high precision RF demodulator plus level shifter operational amplifier, resettable peak detector and output driver

For detailed schematics of the Analogue Conditioning Board, see

- **Annex 21 Digital Filter Wall Board - RF daughter**
- **Annex 22 Digital Filter Wall Board - RF mother**
- **Annex 23 Digital Filter Wall Board - Analogue daughter**

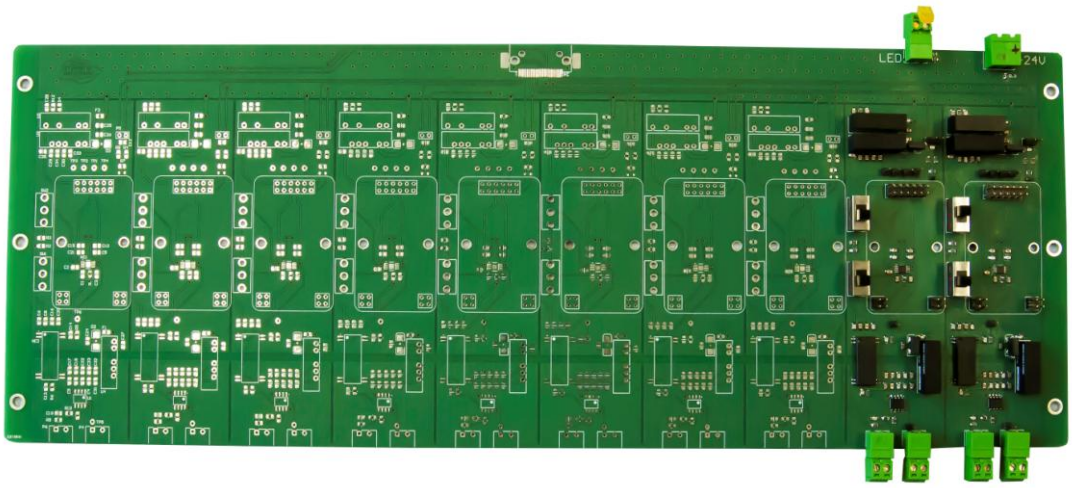

Figure 18 Analogue Conditioning Board with 10 channels.

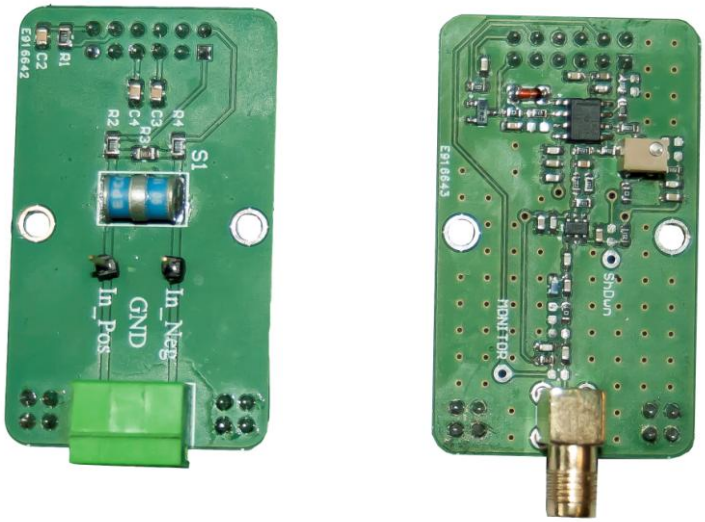

Figure 19 Typical daughter cards (protection and RF power detector) for Analogue Conditioning Board.

12.3. Conditioning Box

The mechanical dimensions of the Conditioning Box: standard 19” rack mounted box with 4U height, housing all of the necessary connectors required by the field devices like klystron, PLC, modulator, RF forward and reflected power detectors, fibre connectors for the pin diodes and the LLRF LVDS connectors. Both digital and analogue signal conditioning circuits are included.

The Conditioning Box involves

- 1 piece of Digital Conditioning Board
- 2 pieces of Analogue Conditioning Board
- +24 V and +5 V switch-mode power supply with low noise, low ripple and high efficiency

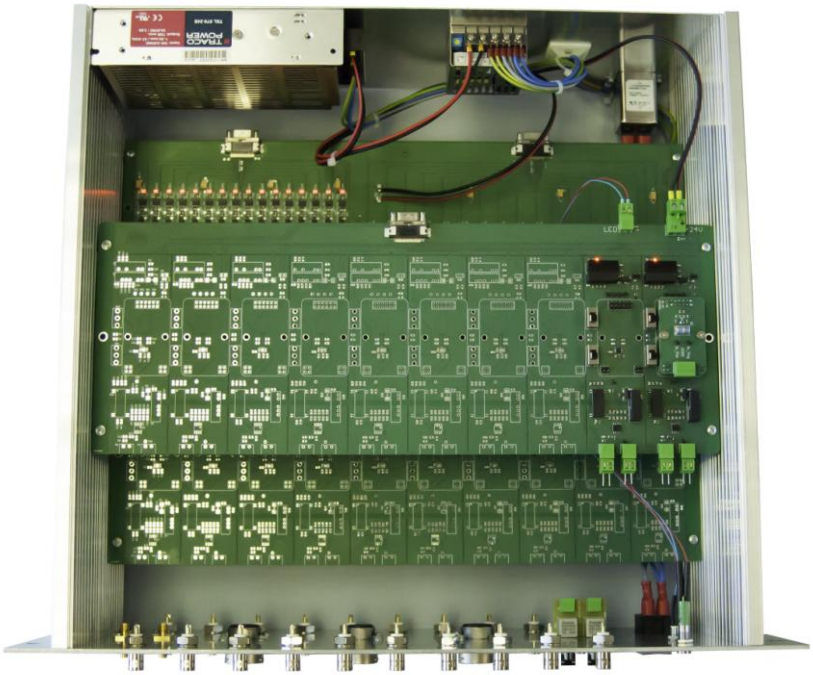

Figure 20 Internal view of the Conditioning Box.

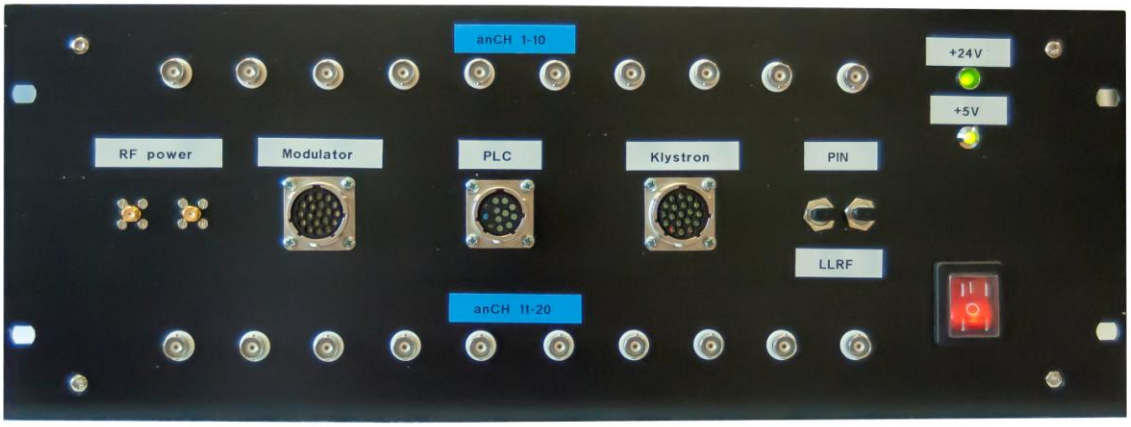

Figure 21 Real panel of the Conditioning Box with connectors.

For the list of components of the Conditioning Box, see

- **Annex 24 Conditioning Box components**

Please note that the prices given in the table can change depending on the customer, the total amount ordered and the date of the order (as it was experienced). In addition, the exchange rate between EUR and HUF can cause an uncertainty.

13. PROJECT SCHEDULE FOR CONSTRUCTION

See Table 1 (page 6) for project schedule of Signal Conditioning Board (SCB) including

- CDR (Critical Design Review),
- FAT 1-4 (Factory Acceptance Test) and
- SAR (System Acceptance Test).

A more detailed project schedule for Medium Beta section including SIM, FIM and SCB is shown in Table 2.

Table 2 Project schedule for Medium Beta section.

Activity	2015				2016				2017				2018				2019				2020			
	Q 1	Q 2	Q 3	Q 4	Q 1	Q 2	Q 3	Q 4	Q 1	Q 2	Q 3	Q 4	Q 1	Q 2	Q 3	Q 4	Q 1	Q 2	Q 3	Q 4	Q 1	Q 2	Q 3	Q 4
Kick-off meeting				■																				
Medium Beta																								
Design and prototype				■	■	■	■	■	■	■														
CDR 2017-06-28										x														
Industrialization start										x														
Procurement components											■	■												
Assembly of subsystems											■	■												
FAT of SIM, FIM and SCB											■	■												
Batch 1-8 systems delivery 01/12/2017												x												
Procurement components												■	■											
Assembly of subsystems												■	■											
FAT of SIM, FIM and SCB												■	■											
Batch 9-16 systems delivery 01/03/2018													x											
Procurement components													■	■										
Assembly of subsystems													■	■										
FAT of SIM, FIM and SCB													■	■										
Batch 17-24 systems delivery 01/06/2018														x										
Procurement components														■	■									
Assembly of subsystems														■	■									
FAT of SIM, FIM and SCB														■	■									
Batch 25-36 systems delivery 01/09/2018															x									
SAR MB Sep 2018															x									

14. RISK REGISTER

1	Event	Tendering process and serial production starts with relevant delay
	Cause	Modification is needed after the CDR and waiting for missing information
	Impact	Delay of deliveries
	Treatment plan	Increase the number of units per batch and decrease the number of batches

2	Event	Signal conditioning procedure implemented in the CB does not match the real field devices
	Cause	At the time of design and development of CB, the parameters of the real field devices are not fully available therefore the initial design is very complex with few redundancy between options
	Impact	Delay of completion and delivery, cost increase
	Treatment plan	Re-design or modification of the circuit already implemented in CB

3	Event	During engineering run high failure rate of the system
	Cause	MTCA.4 is a very new technology without long-term verification, experts are not available
	Impact	Damage of expensive devices
	Treatment plan	Before final installation of the MTCA.4 based system, standard checking tests should be carefully performed

4	Event	Field experts do not accept the systems
	Cause	The design concept of the system differs from the requirements expected by the field experts
	Impact	Delay of delivery
	Treatment plan	Re-design of the systems based on the requirements suggested by the field experts

15. OPINION ABOUT THE INTERLOCK SYSTEM

15.1. Strategic solution of ESS

The Signal Conditioning Box is to be used for proper matching of the analogue/digital signals between the inputs/outputs of the accelerator field devices and Interlock Systems. SIM part of the Interlock System is constructed based on Siemens automation standard PLC platform, while the FIM part uses MicroTCA.4 standard. These standards represent excellent environment and flexibility for establish the platforms used for realization of processing power both the slow and the fast signals. The most important issues regarding the noise immunity of the platforms must be taken into consideration to ensure the required reliability and stability.

From the mentioned point of view the Siemens platform is applied with the features having the grade satisfying the demands, but not the MicroTCA.4 environment. With respect to the hardware specification of the MicroTCA.4 system a detailed measurements and discussions of the results have to be considered.

A Programmable Logic Controller (PLC) is the best choice for most systems that do not require tight synchronisation with the ESS accelerator cycles:

- needs to have built-in-logic that ensures safe autonomous operation of the device under control even if the connection to upper layer, EPICS is broken;
- has a rate of I/O that is relatively slow (in 10 Hz range) and not bound to the 14 Hz beam rate;
- cooling systems, vacuum control, slow interlock etc.

The PLCs are foreseen to be connected to EPICS IOCs that run on virtual machines on robust server infrastructure maintained by the ICS infrastructure team.

During development, in cases when the infrastructure is not available, it is possible to have the EPICS controllers running on industrial or even regular off-the-shelf PCs. However, this hardware will be removed when the system will be taken in production.

The ESS standard platform for most demanding tasks in terms of data acquisition and online handling is the MicroTCA.4 standard. These tasks are characterized by:

- need for synchronized actions and processing in real-time, processing of one beam pulse must be finished before start of the next, in 71 msec corresponding the 14 Hz operation;
- high-speed processing that requires use of FPGAs or similar technology;
- capability to handle large data rates and volumes.

MicroTCA.4 technology shall be used when the protected system requires:

- acquisition of analogue signals faster than 100 kSPS,
- precise time synchronisation that requires access to ESS timing system,
- clock signals that are synchronised to the main RF source,
- generation of waveform data in range of megabytes or more per second,
- actions on the data need to happen within milliseconds or faster.

This technology tends to be expensive and requires special expertise so its use shall be limited to cases where the above requirements apply. Typical examples are beam instrumentation and low-level RF (LLRF) control.

Concluding the above mentioned features of slow and fast platforms as ESS candidates for realising the interlock functions have to declare that any of the consolidating actions of the platforms can create impacts on the Signal Conditioning systems.

On the other end the real field devices should be specified in terms of signal lists, definition of the connectors, pin assignments of cables, timing and logic of the signals connecting in or out. In case

of missing any data, timing information describing the operation of the field devices can strongly impact on the Conditioning Boards, both analogue and digital.

15.2. Simple solution

The interlock systems can be implemented in different ways. One of the possible solutions of the electronics for the klystron amplifier and related electronics is implemented in hardware on printed circuit boards. Indeed, the timing specifications and the need of a reliable system forbid any software solution, including real-time platforms. Moreover, even if implementation based on Field Programmable Gate Arrays (FPGA) could be considered, the klystron provider suggested the use non-volatile, non-programmable hardware. This type of interlock can be considered as a hard wired unit dedicated to prevent the field devices connected directly to the system. The system flexibility is minimal built into this kind of solutions, and not even satisfying when the technical parameters of the field devices have been changed slightly.

Regarding the Signal Conditioning Boards the solution has to be realised in a way to fulfil all the system requirements with the maximal flexibility versus minimal complexity. In this field of business by law, the simplest solution is the best one.

The optimal solution is if the interlock system can tolerate directly the signals from-to field devices, that is can be connected directly to them. The Signal Conditioning electronics should be a small part of the interlock unit or electronics placed inside the field devices instead of a standalone Signal Condition Board with serious drawbacks like

- consumption of high power,
- heat dissipation, extra cooling with ventilation,
- big weight and size,
- expensive standard mechanics,
- expensive operation and
- sophisticated maintenance.

15.3. Value engineering

Value engineering is a crucial aspect of the construction phase of the ESS ERIC spallation neutron source. In case of a simple specific solution matching the real field equipment instead of a general solution ready to handle lots of yet unknown parameters, value engineering task would also be completed.

16. GLOSSARY

Term	Definition
aCB	Analogue Conditioning Board
CB	Conditioning Box
CDR	Critical Design Review
dCB	Digital Conditioning Board

EPICS	Experimental Physics and Industrial Control System
ESS	European Spallation Source
ESS ERIC	European Spallation Source, European Research Infrastructure Consortium
FAT	Factory Acceptance Test
FIM	Fast Interlock Module
FPGA	Field-Programmable Gate Array
ICS	Integrated Control System of ESS ERIC
IGBT	Insulated-Gate Bipolar Transistor
IKC	In-Kind Contribution
IKC Agreement	In-Kind Contribution Agreement
IOCs	Input Output Controllers
ISO	International Organization for Standardization
kSPS	kiloSample Per Second
LED	Light-Emitting Diode
LLRF	Low Level RadioFrequency
LVDS	Low-Voltage Differential Signalling
LVTTL	Low Voltage Transistor Transistor Logic
MTA Atomki	Short name of Institute for Nuclear Research, Hungarian Academy of Sciences from its Hungarian name Magyar Tudományos Akadémia, Atommagkutató Intézet
MTCA	Micro Telecommunications Computing Architecture
P&ID	Piping and Instrumentation Drawing
PC	Personal Computer
PCB	Printed Circuit Board
PLC	Programmable Logic Controller
RC	Resistor-Capacitor
RF	Radiofrequency
RF Group	Radiofrequency Group in Accelerator Division of ESS ERIC
RF-LPS	Radiofrequency Local Protection System
SAR	System Acceptance Review
SCB	Signal Conditioning Board
SIM	Slow Interlock Module
TTL	Transistor-Transistor Logic

17. REFERENCES

[1] In-Kind Contribution Agreement (IKC Agreement) AIK 8.4, ESS-0061938 with the Schedule and Framework, ESS-0061939
[2] RF-LPS Project Baseline, ESS-0061940
[3] [SUM] ESS Procedure for Sustainable Selection of Materials, ESS-0011452

18. LIST OF ANNEXES

Annex 01 FIM conditioning board requirements

Annex 02 Technical report for linear technology RF detector LTC5530 and ADL5513

Annex 03 ESS DIO Conditioning Board Hardware Manual

Annex 04 RF detector - Interface between coupler and interlock

Annex 05 DIO_3118 Digital-IO Generic FMC

Annex 06 DIO_3118 Proposal for Digital-IO Generic FMC

Annex 07 DIO3118 SDR Input Connector

Annex 08 DIO3118 SDR Output Connector

Annex 09 External connectivity of the Klystron Modulator

Annex 10 ADC_3117 High-Density ADC FMC Technical Specification

Annex 11 Toshiba State Machine FIM

Annex 12 Digital isolation test report

Annex 13 Technical report of the mother board plus daughter board

Annex 14 Fast Interlock Module LEP Klystron

Annex 15 ICS Handbook

Annex 16 Slow Interlock Module CERN

Annex 17 Tender document in Hungarian

Annex 18 Digital Conditioning Board

Annex 19 16 Ch LVTTL Input

Annex 20 14 Ch LVTTL Output & 2 Ch Fiber

Annex 21 Digital Filter Wall Board - RF daughter

Annex 22 Digital Filter Wall Board - RF mother

Annex 23 Digital Filter Wall Board - Analogue daughter

Annex 24 Conditioning Box components

DOCUMENT REVISION HISTORY

Revision	Reason for and description of change	Author	Date
1	First issue	MTA Atomki	2017-06-20