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| http://demon.ise.pw.edu.pl/images/headers/iselogo.gif https://europeanspallationsource.se/sites/default/files/ess_logo_frugal_blue_cmyk_1.jpg |
| Description: | This document describes the requirements of the LO RTM designed for ESS LLRF |
| Title: | **LO RTM Specification** |
|  |
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| Date: | 10.02.2017 |

1. **General description**

The LO RTM module will be responsible for generation and distribution of LO and clock signals based on an externally fed reference signal.

The module will be designed as an RTM module compliant with the MTCA.4 standard. It shall work together with the "RTM carrier" AMC module designed by PEG. If necessary, the module will be full-size.

1. **Functional specification**

The LO RTM module should fulfill the following functional requirements:

* the module must be compliant with the MTCA.4 RTM specification,
* the module can be mid-size or full-size,
* the module shall provide 4 LO outputs,
* the module shall synthesis the LO signal using direct analog synthesis scheme,
* the module shall provide 4 clock outputs,
* the module shall provide 1 reference output,
* the configuration of the module should be performed remotely by the AMC module,
* a monitoring output for clock and LO signal shall be provided.
	1. **Block diagram**

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* 1. **MTCA.4 Diagnostics**

Following diagnostics information shall be provided to the MTCA.4 management:

* power supply voltages,
* temperature.
	1. **LLRF System Diagnostics**

Following diagnostics signals should be delivered to the AMC module:

* output power level (one detector for each group),
* input power level.
	1. **Interfaces**

There should be three groups of connectors on the LO RTM module:

* front panel connectors,
* zone 3 connector to AMC module,
* debugging connectors.
	+ 1. **Front panel connectors**

All front panel connectors are presented in table 1.

**Table 1: Front Panel Connections**

|  |  |  |  |
| --- | --- | --- | --- |
| **Name** | **Connector Type** | **Level** | **Description** |
| REF in | SMA (50Ω) | 3 dBm ± 2 dB  | Main Reference input |
| REF out | SMA (50Ω) | +13 dBm ± 1 dB | Reference output |
| 4 x LO out  | SMA (50Ω) | +15 dBm ± 1 dB | LO signal outputs |
| 4 x CLK out  | SMA (50Ω) | +15 dBm ± 1 dB | CLK signal outputs |
| LO mon | MMCX (50Ω) | > -20 dBm | LO signal monitoring output |
| CLK mon | MMCX (50Ω) | > -20 dBm | CLK monitoring output |

* + 1. **Zone 3 Connector**

Pinout of the ZONE 3 connector should be compliant with the DESY digital class D.1.0[[1]](#footnote-1) and "RTM carrier" AMC module. The detailed pinout of ZONE 3 connectors is presented in table 2. LVDS signaling will be used for bidirectional communication between the AMC and the RTM.

The RTM module will not make use of the AMC\_CLK, AMC\_TCLK, OUT0, OUT1, OUT2 signals. Those signals will be terminated. The RTM will source the RTM\_CLK1 signal.

**Table 2: ZONE 3 Connectors Pinout**

|  |  |  |  |  |
| --- | --- | --- | --- | --- |
| **Signal name** | **Pins** | **Electrical Type** | **Level** | **Description** |
| RTM+12V | 1a, 1b, 2a, 2b (J30) | DC +12 V | +12 V | AMC power supply voltage (+12 V) |
| RTM\_MP | 2c (J30) | DC +3.3 V | +3.3 V | Management power supply voltage (+3.3 V) |
| RTM\_PS# | 1c (J30) | DC GND | +3.3 V | Management present pin |
| RTM\_SDA | 1d (J30) | I2C | +3.3 V | Management I2C data line |
| RTM\_SCL | 2d (J30) | I2C | +3.3 V | Management I2C clock line |
| TCK | 1e | LVCMOS | +3.3 V | JTAG |
| TDO | 1f | LVCMOS | +3.3 V |
| TDI | 2e | LVCMOS | +3.3 V |
| TMS | 2f | LVCMOS | +3.3 V |
| RTM\_CLK1 | 3c, 3d | LVDS |  | High speed clock |
| DIFF\_IO\_0 | 5a, 5b | LVDS |  | Data lines |
| DIFF\_IO\_1 | 5c, 5d | LVDS |  |
| DIFF\_IO\_2 | 5e, 5f | LVDS |  |
| DIFF\_IO\_3 | 6a, 6b | LVDS |  |

* + 1. **Debugging connectors**

The debugging connectors are presented in table 3.

**Table 3: Debugging Connectors**

|  |  |  |  |
| --- | --- | --- | --- |
| **Signal name** | **Connector Type** | **Level** | **Description** |
| RTM+12V | PHOENIX CONTACT 1803439 | +12V | AMC power supply voltage (+12 V) |
| RTM\_MP | PHOENIX CONTACT 1803439 | +3.3 | Management power supply voltage (+3.3 V) |
| IPMI BUS | Gold Pin | +3.3V | Management I2C  |

1. **Electrical requirements**
	1. **Operating frequency**

Reference input: 704.42 MHz

Supported intermediate frequencies:

23.481, 25.158, 27.093, 29.351, 32.019, and 35.221 MHz

LO outputs frequency: 704.42 MHz + IF

CLK frequency: 117.403(3) MHz

* 1. **LO signal output phase noise**

Phase noise of the output signal should fulfill requirements presented in table 4 (assuming the sufficient quality of the reference signal).

**Table 4: LO signal absolute phase noise requirements**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Frequency offset | 10 Hz | 100 Hz | 1 kHz | 10 kHz | 100 kHz | 1 MHz | 10 MHz |
| Max. Phase Noise SPD [dBc/Hz] | -88 | -100 | -115 | -125 | -140 | -150 | -155 |

* 1. **CLK signal output phase noise**

Phase noise of the output signal should fulfill requirements presented in table 5 (assuming the sufficient quality of the reference signal).

**Table 5: CLK signal phase noise requirements**

|  |  |  |  |  |  |  |  |
| --- | --- | --- | --- | --- | --- | --- | --- |
| Frequency offset | 10 Hz | 100 Hz | 1 kHz | 10 kHz | 100 kHz | 1 MHz | 10 MHz |
| Max. Phase Noise SPD [dBc/Hz] | -104 | -120 | -130 | -140 | -145 | -150 | -153 |

* 1. **CLK signal spurious**

Maximum harmonic spurious level: -60 dBc

Maximum non-harmonic spurious level: -60 dBc

* 1. **LO signal spurious**

Maximum harmonic spurious level: -60 dBc

Maximum non-harmonic spurious level: -50 dB

1. http://mtca.desy.de/resources/zone\_3\_recommendation/index\_eng.html [↑](#footnote-ref-1)