EUROPEAN SPALLATION SOURCE

ESS BPM Firmware

Status of BPM firmware

ESS FPGA development framework

- ESS platform
- ESS DEVENV for IKCs
- BPM Status

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Beam Diagnostics

The Beam Diagnostics work package includes the development of all beam instrumentation for the ESS linac:

- BLM (Beam Loss Monitor)
- BCM (Beam Current Monitor)
- BPM (Beam Position Monitor)
- FC (Faraday Cup)
- WS (Wire Scanner)
- NPM (Non-Invasive Profile Monitor)
- EMU (Emittance Measurement Unit)
- LBM (Longitudinal Bunch Profile Monitor)

etc.....

Integrated Control System (ICS)

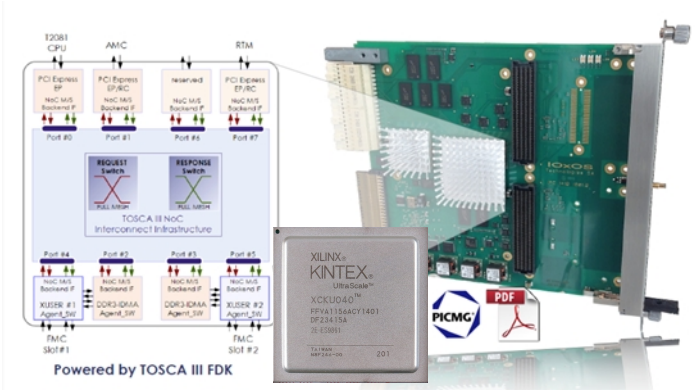
The ESS Control System is a complex network of hardware, software and configuration databases that integrates the operations of all the various parts of the Accelerator, Target, Instrument and Conventional Facility infrastructures.

ESS has a large network of laboratories to exchange knowledge, personnel and experience with, and that in many cases will contribute directly to the project through **In-Kind Contributions (IKCs)**

MTCA.4 AMC

BEAM DIAGNOSTIC
PLATFORM
STRUCK
SIS8300KU/L2
+
DWC8300

MIGRATION



ICS
PLATFORM
IOxOS
IFC1420 (??)

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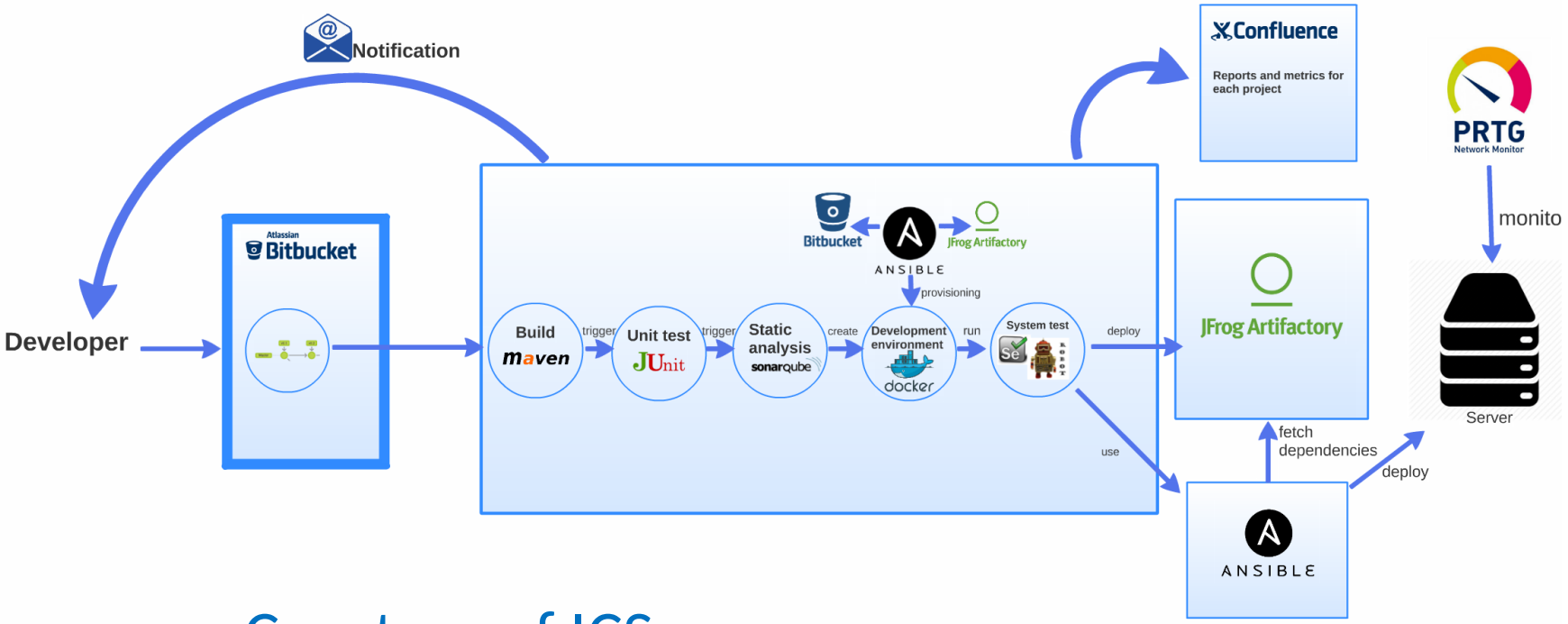
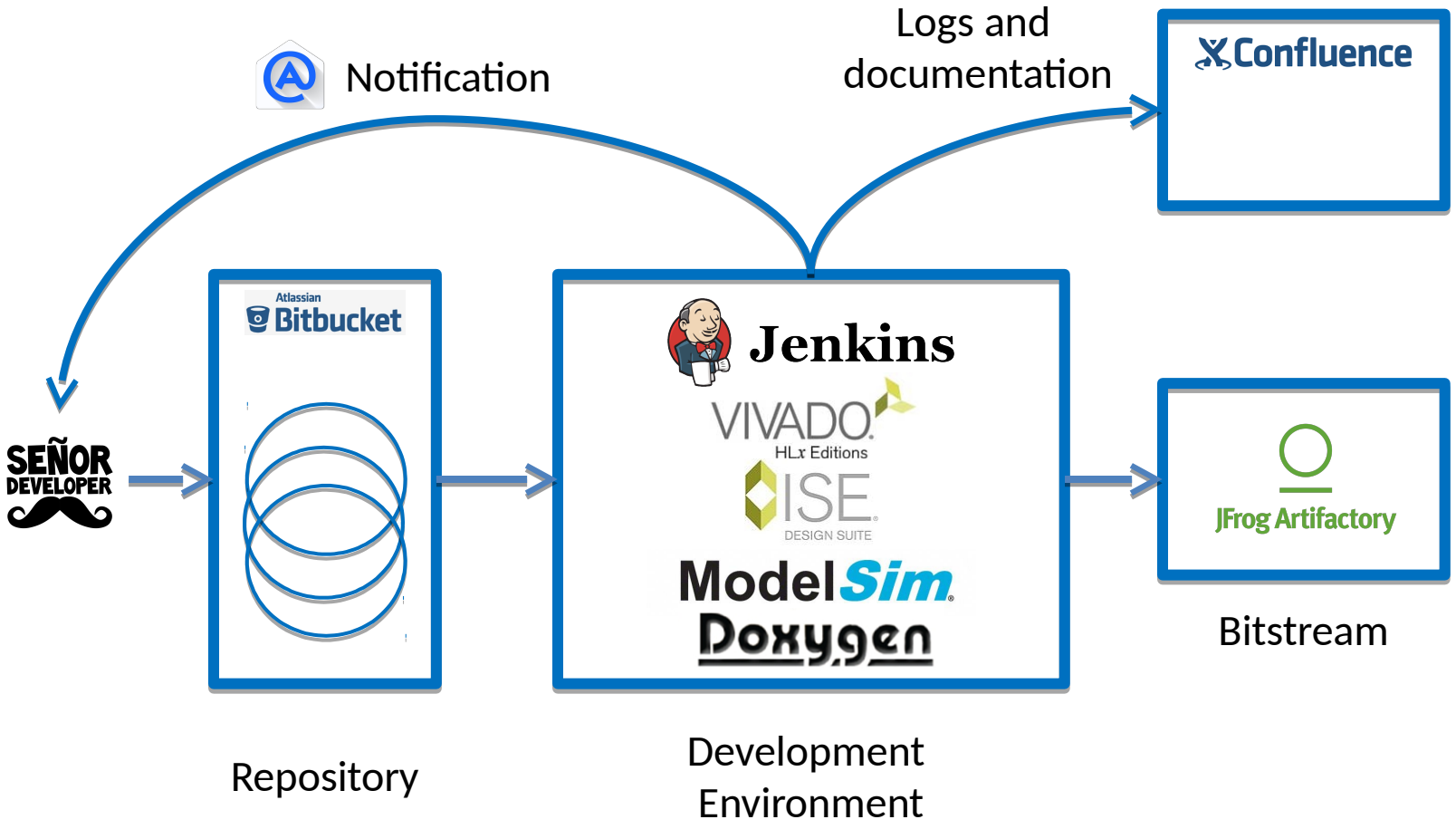
ICS Continuous Integration/Delivery

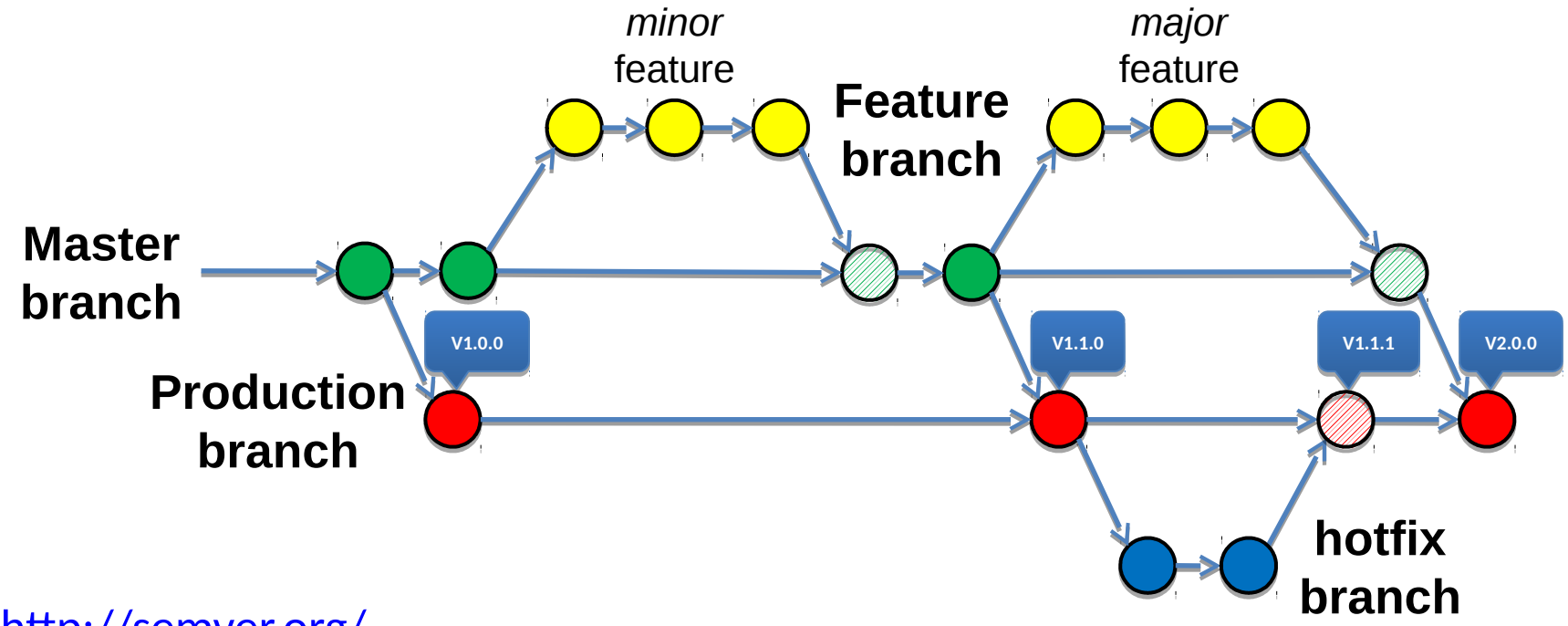


Courtesy of ICS JAVA flow

FPGA design/delivery



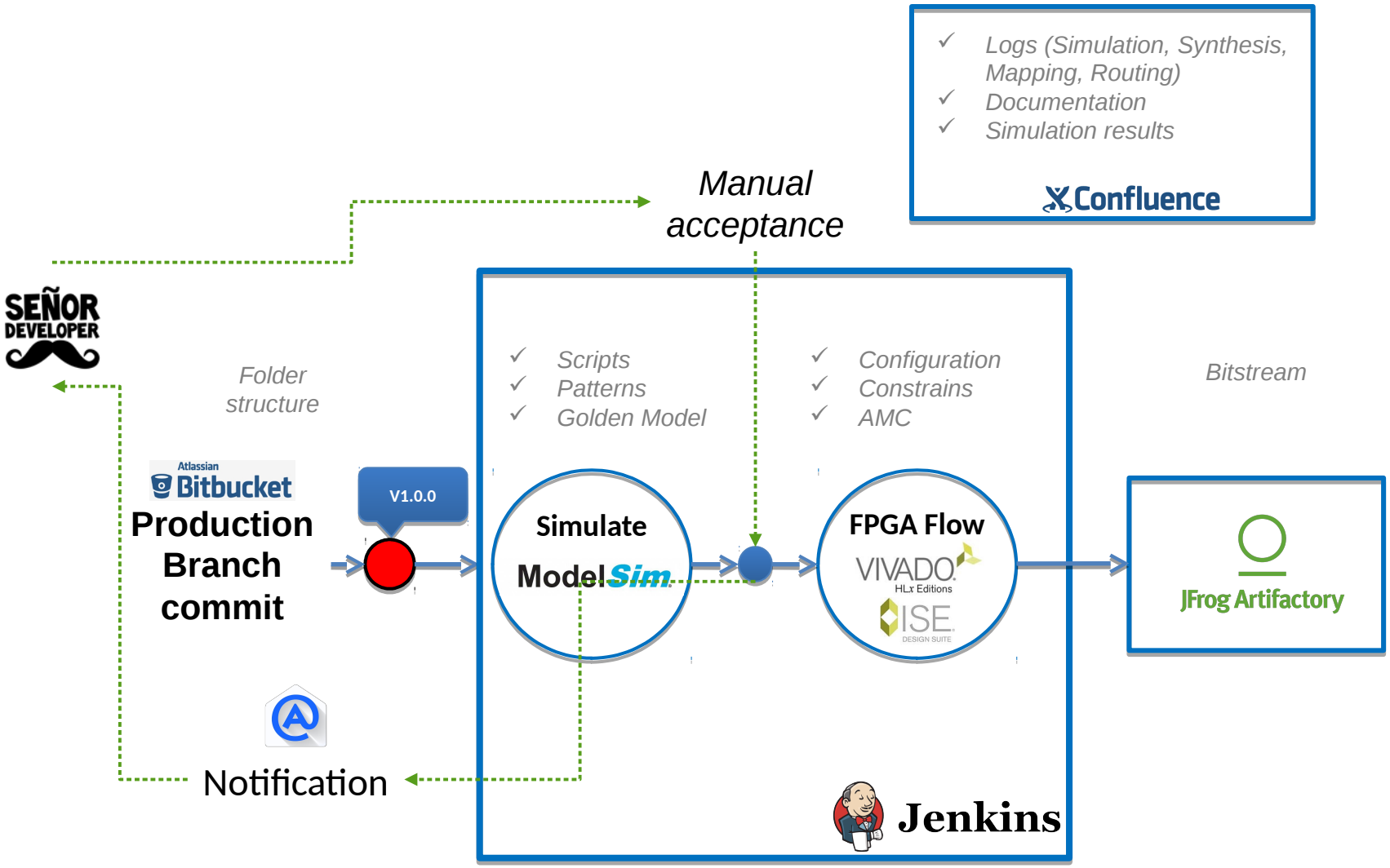
Atlassian Bitbucket



http://semver.org/

MAJOR.MINOR.PATCH

- MAJOR version when you make incompatible API changes
- MINOR version when you add functionality in a backwards-compatible manner
- PATCH version when you make backwards-compatible bug fixes


✓ Logs (Simulation, Synthesis, Mapping, Routing)
✓ Documentation
✓ Simulation results
Confluence
Manual acceptance
SEÑOR DEVELOPER
Folder structure
✓ Scripts
✓ Patterns
✓ Golden Model
✓ Configuration
✓ Constrains
✓ AMC
Bitstream
Atlassian Bitbucket
Production Branch commit
V1.0.0
Simulate
ModelSim
FPGA Flow
VIVADO HLx Editions
ISE DESIGN SUITE
JFrog Artifactory
Notification
Jenkins

Frameworks on bitbucket

- STRUCK project contains different repository for FW and SW for the SIS8300L/L2/KU, each of it has 2 branch for the 2 RTM used:
  - for BCM (SIS8900 RTM);
  - for BPM (DWC8300 downconverter RTM);
  -
- IOxOS project contains the TOSCA III firmware for IFC1410 that support streaming of data from a ADC 3110/3111 - FMC Mezzanine Card

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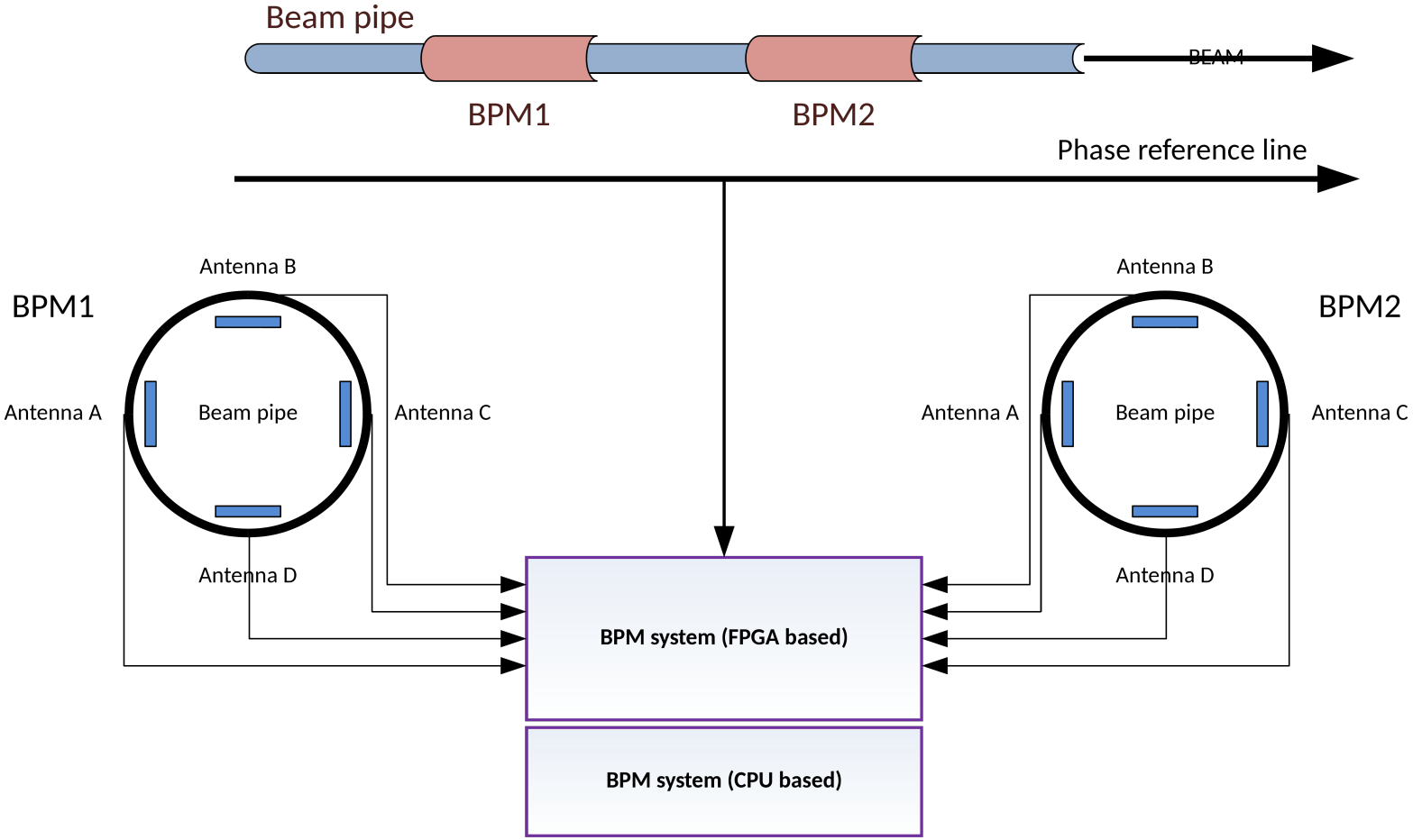
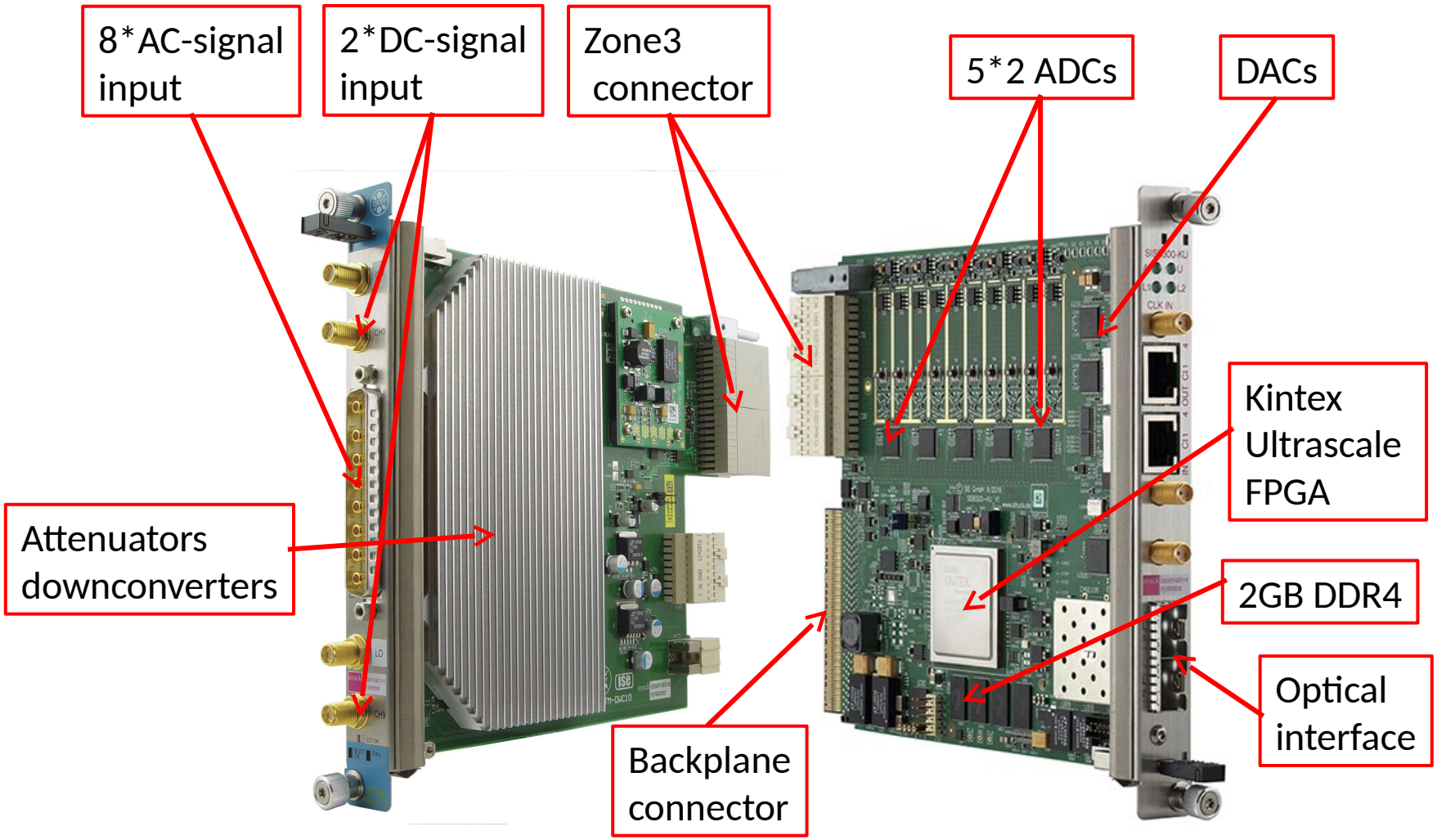
BPM

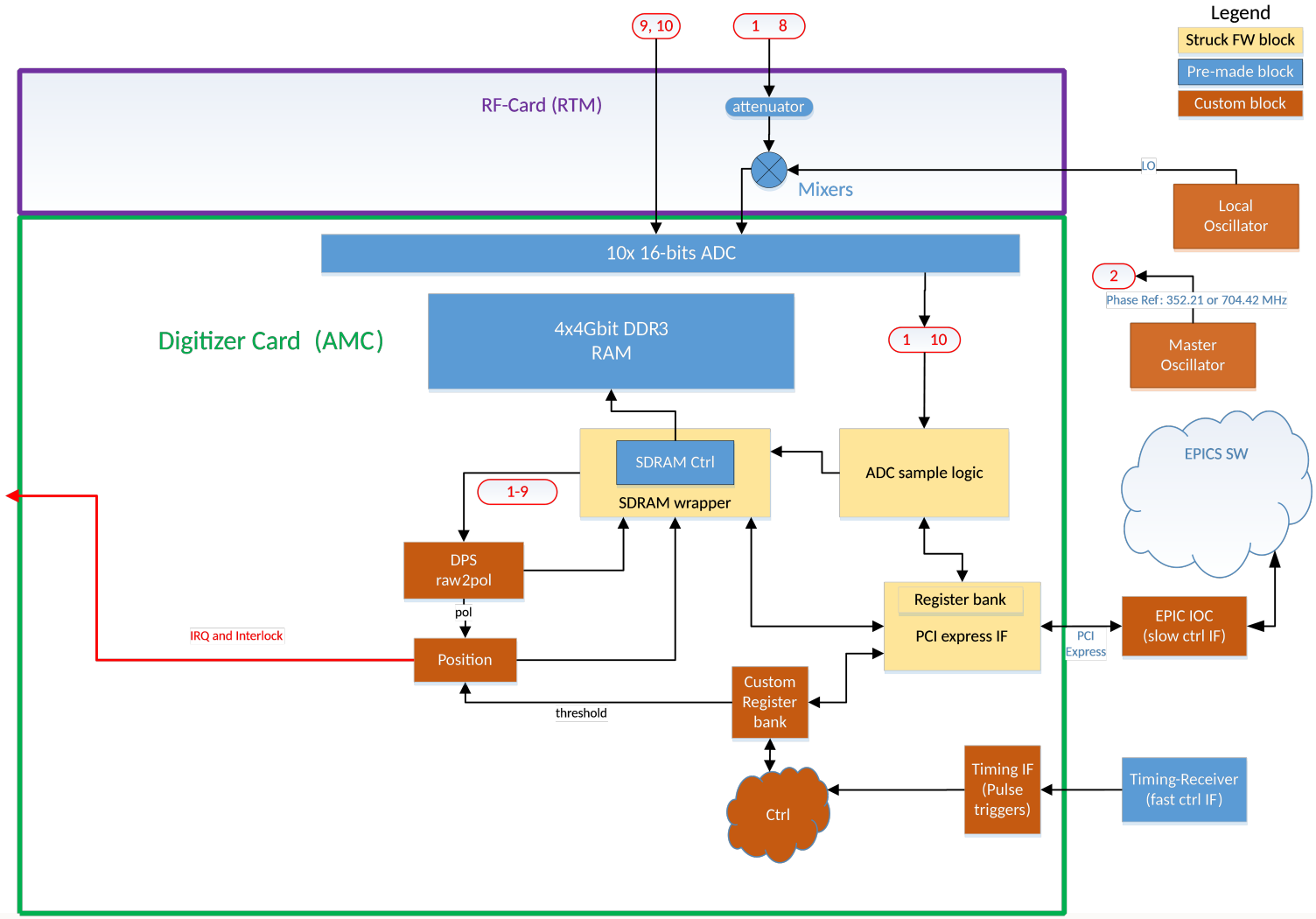
What does it include?



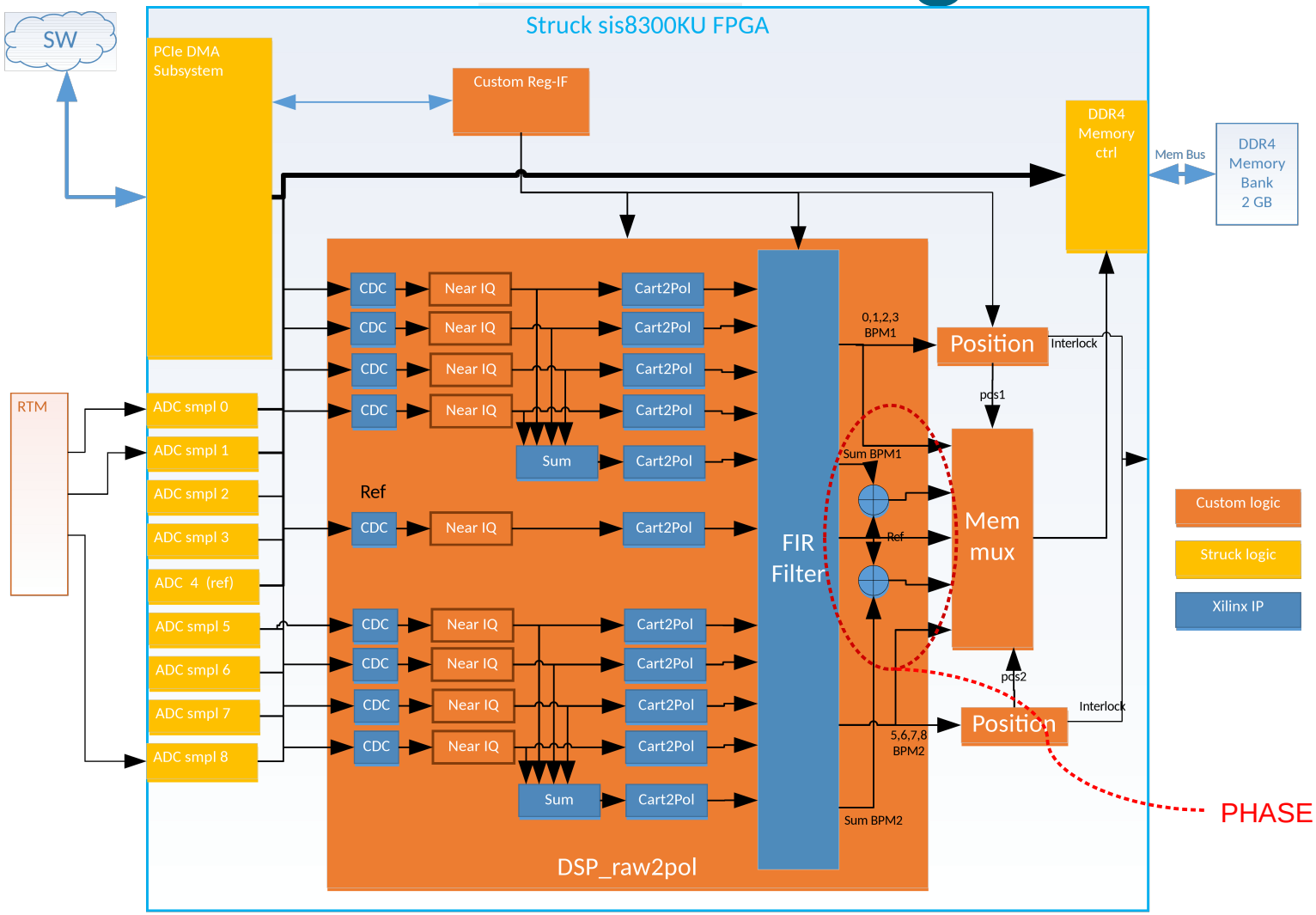
HW: RTM-Digitizer



Overview RTM-Digitizer



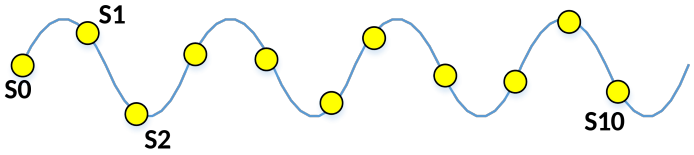
Overview RTM-Digitizer



Supported FW functionality:

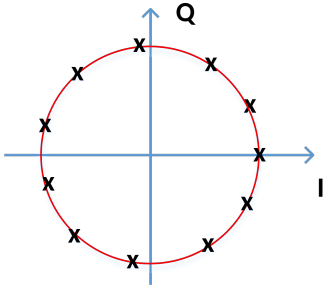
- Supports both pulsed and CW operation;
- Operation modes:
  - ADC raw data
  - Near-IQ sampling
  - FIR filtering
  - Single channel phases and amplitudes
  - BPM phases relative to Phase reference line
  - BPM positions calculations
  - Self trigger
  - Position interlock

Near or Non IQ Sampling



N = 11 and M=4

$$S_i = I \cdot \sin(\varphi_i) + Q \cdot \cos(\varphi_i$$

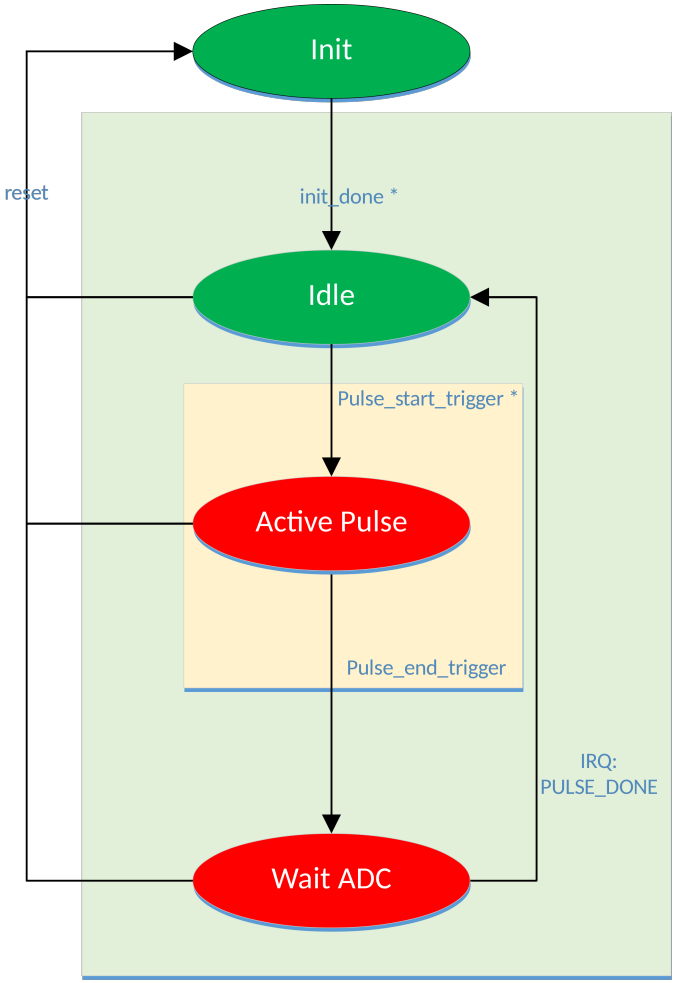


$$I = \frac{2}{N} \sum_{i=0}^{N-1} s_i \cdot \sin\left(i \cdot 2\pi \cdot \frac{M}{N} \right)$$

$$Q = \frac{2}{N} \sum_{i=0}^{N-1} s_i \cdot \cos\left(i \cdot 2\pi \cdot \frac{M}{N} \right)$$

- Less sensitive to:
  - Nonlinearities
  - DC-offset
  - Noise
- Will cost in delay

Operation



XXX_trigger : commes from timing control system.

BPM operationell

BPM active

SW: R/W memory not allowed

SW: All memory accesses allowed

* At these transitions all visible new parameters are taken into use.

** At this transition interrupt PULSE_DONE is raised

Operations

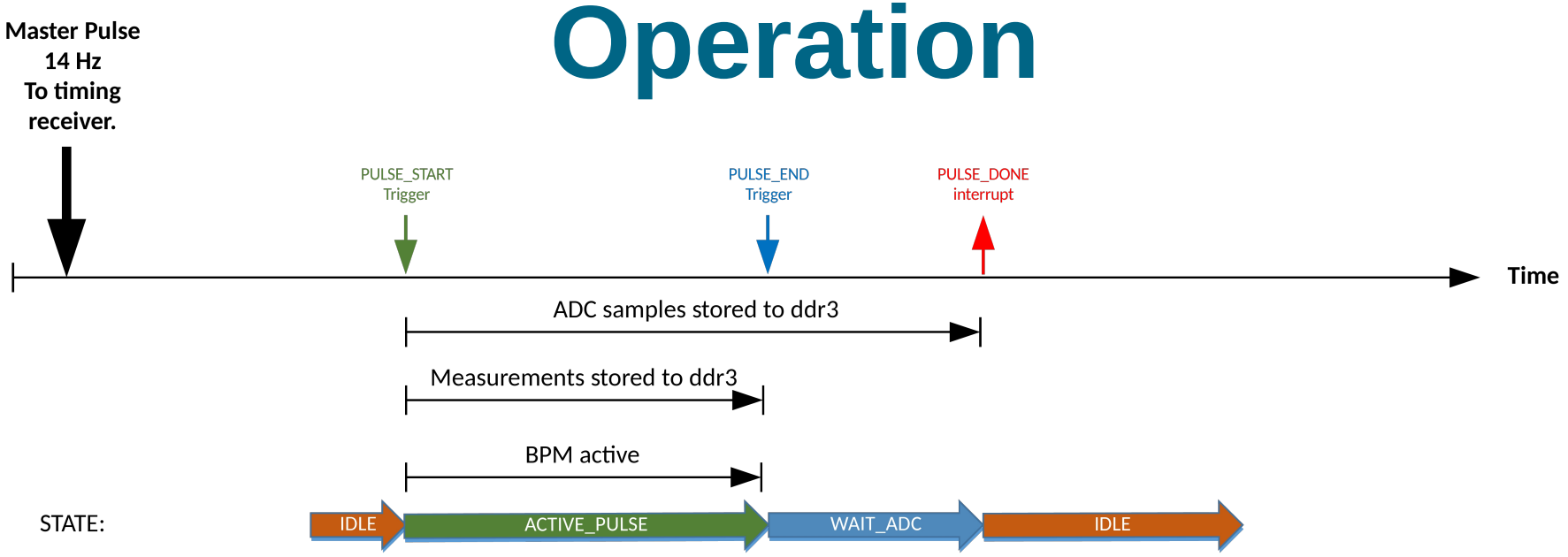
Init:
- **SW:** R/W registers.
- **FPGA:** Nothing.

Idle:
- **SW:** Read data, R/W registers.
- **FPGA:** Nothing.

Active pulse:
- **SW:** R/W registers.
- **FPGA:** Store external and internal signals.

Wait ADC:
- **SW:** R/W registers.
- **FPGA:** Wait ADC store done.

Operation

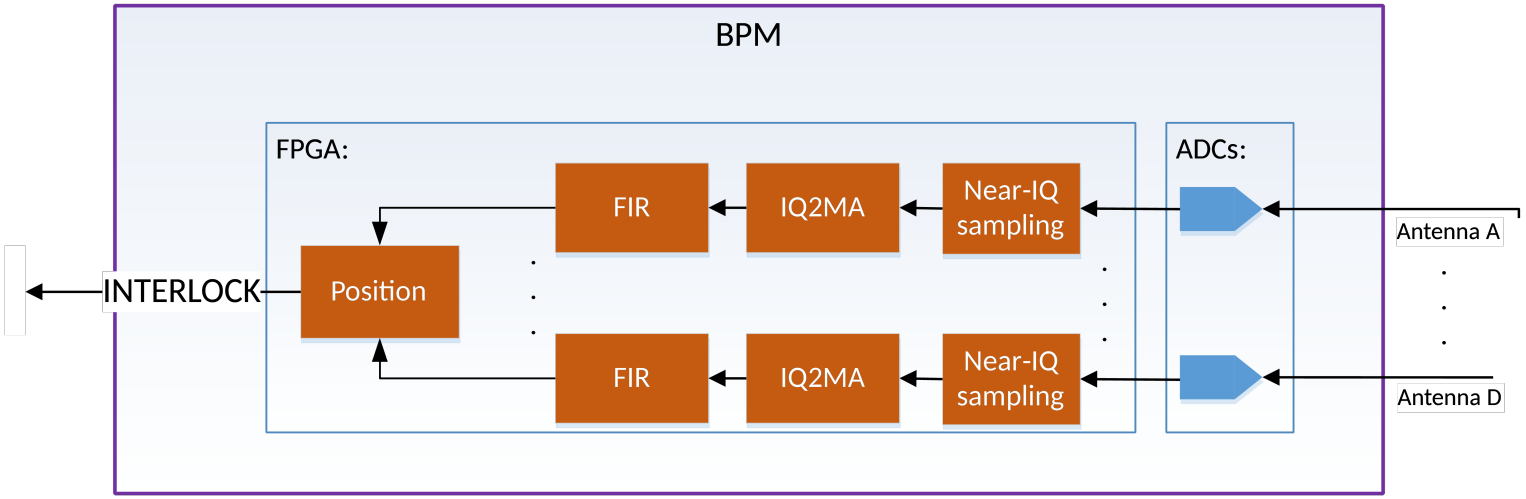


After PULSE_DONE IRQ is received, SW has access to:

- From memory:
  - Raw samples of all 9 input channels, plus one measurement channel or
  - Raw samples from 1 BPM, plus all measurement channels.
- From registers (for fast GUI displaying)
  - Amplitude and phase of Phase-ref, position and antenna-sum at PULSE_END.

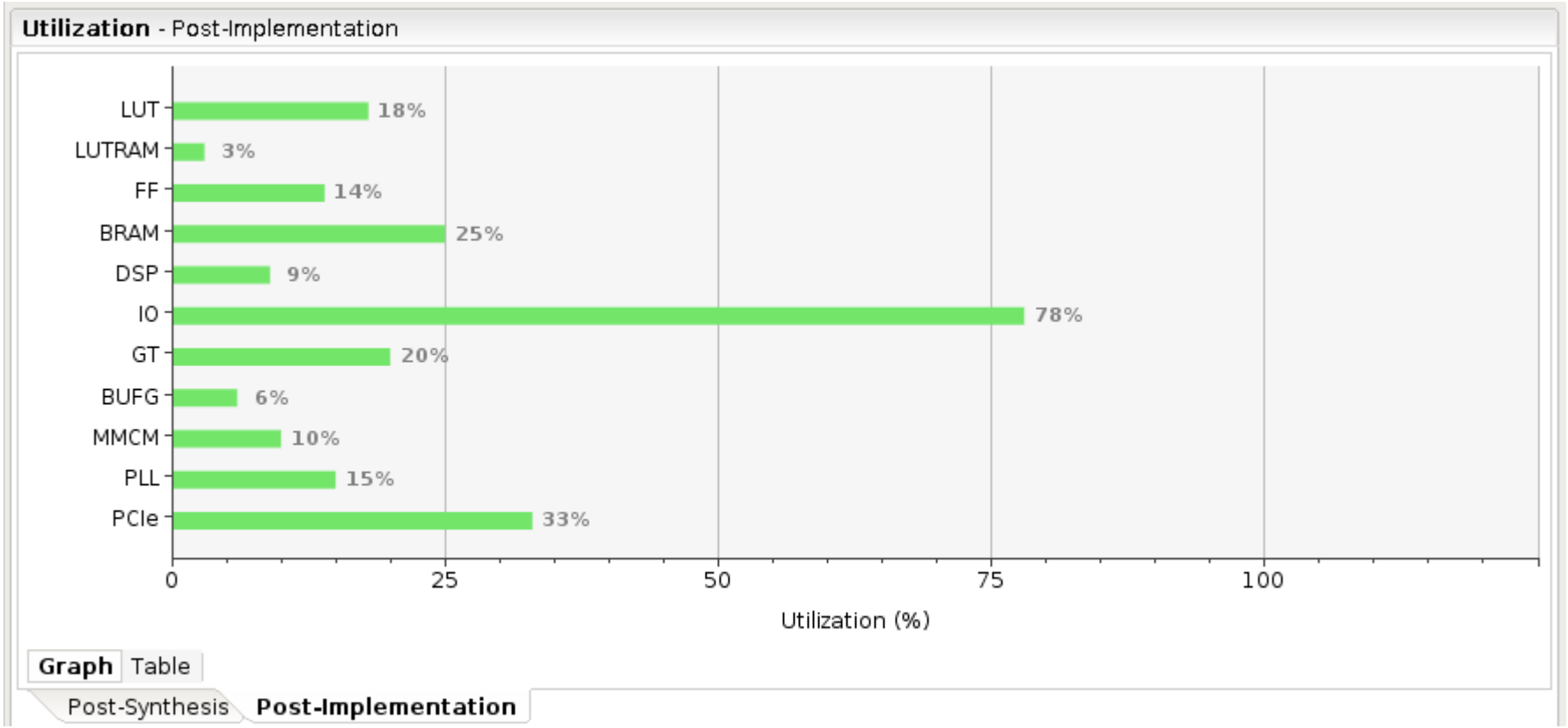
PDR's implementation numbers

- Utilization of FPGA: 75% slices
- Max Clk period ~10 ns (100 MHz)
- Delay: FW 97cc, ADC 13cc



- Input to interlock delay ~1.1 us

Today's implemetation number



PDR's Next step

- Use and test the design as much as possible 
- Optimizations, if required. 
- Move to the next generation of digitizers 
  - Reduce latency.
  - Get access to all internal data at all times.
  - Get space to add new functionality.
- Test 
- Test
- And some more testing

Next step

- Firmware has been tested on the STRUCK SIS8300L (Xilinx Virtex 6 FPGA) and successfully ported with same performance to STRUCK SIS8300KU (Xilinx Kintex Ultrascale);
- We plan to migrate from the Struck framework (not AXI based) to a more reliable and maintainable AXI based framework;
- When IOxOS IFC1420 (with same FPGA mounted) it will replace the SIS8300KU (we wish…) easily;

Questions


Thanks!