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| |  | | --- | | **Background** | | Background    The ESS LEBT will include one ACCT toroid that will be integrated into the LEBT-RFQ interface. The LEBT will be commissioned in 2017 in Catania-Italy. The ACCT will be used to measure the pulsed beam current at the LEBT output.  The ESS ACCT system will include custom hardware, firmware and software. It is planned to test and verify the critical parts of the system during the LEBT tests in Catania before final installation in the ESS linac tunnel.  The LEBT ACCT toroid will be of Bergoz type. The ACCT front-end electronics will be of Bergoz ACCT-E type with full-scale current range of +/- 100 mA and bandwidth of 3 Hz – 1 MHz.  The ACCT readout electronics will be based on the uTCA.4 standard. It is planned to use a Struck SIS8900 RTM in combination with a Struck SIS8300-L2D AMC for the early LEBT test in Catania.  A custom interface module will be used to match the ACCT-E voltage and impedance to those of the RTM.  The ACCT firmware will consist of two parts being: 1) A custom firmware including the algorithms relevant to the ACCT signal processing such as baseline level correction, droop compensation and interlock signal generation for machine protection. 2) An integration firmware based on the original SIS8300-L2D firmware and tailored to the ESS BCM requirements in terms of clock multiplexing, register and memory maps, data decimation etc.  The readout electronics need to be integrated into EPICS. Display of the ACCT output data and control of the settings will be through a dedicated user screen. | | |
| Purpose of the document:   * Functional description of the LEBT ACCT system for the Catania tests * Definition of the ACCT requirements for the early LEBT tests * Short- and mid-term BCM planning * Starting with the development of the custom- and integration- firmware as well as software * Project coordination with other groups and external partners   Concept:  The BCM system that is planned for the LEBT tests in Catania-Italy in 2017 is based on a Bergoz ACCT toroid and uTCA.4 electronics. The toroid will include calibration winding but no automatic calibration is planned for the early tests in Catania. The ACCT output signal will be first buffered by a Bergoz ACCT-E module and then sent to a custom interface module that will match the signal to the input of the uTCA.4 electronics. The ACCT acquisition electronics will be based on a SIS8900 RTM and SIS8300-L2D AMC from Struck. The ACCT signal will be sampled at 88.0525 MHz and then FPGA processed on the AMC for droop compensation, baseline level correction, V-to-I scale factor and machine protection. A “check shape” block in the ACCT firmware will measure the amplitude, width and frequency of the beam pulse for machine protection and consistency check. A timing receiver board that is synched with the LEBT pulse shall be used to provide pulse trigger and ADC clock for the readout electronics. The electronics will automatically trigger on the edge of the beam pulse, but the external trigger will still be needed for consistency check purposes. The readout electronics will be integrated into EPICS and the beam pulse information including pulse shape, current, charge, width and frequency will be shown on a user screen.  Main objectives:  The system that is described in this document requires new developments for software, firmware and hardware that will be partly done in-house and partly through external collaborations. It is planned to use the LEBT as a test bench to check the performance of the critical parts of the system, thus making sure that they will meet the ESS requirements. The early LEBT tests in Catania are considered “a good opportunity” to test the ACCT system under real beam conditions, and identity/fix bugs well ahead of the final installation in the ESS linac.  Scope:  The scope of the current document is limited to the definition of the ACCT firmware (both custom and integration parts), software as well as custom hardware requirements for the LEBT tests in Catania. Future modifications for the downstream sections are out of the scope of this document.  Acceptance tests:  The BCM system needs to successfully pass acceptance tests against the current requirements before an official delivery takes place.  The foreseen methods of check and verifications are described below:   * Inspection: carefully checking the system thus making sure that it fulfils a certain requirement. * Test: verification by making tests. When applicable, this will be done using a test bench specific to the test as well as some lab. equipment. * Measurement: verification by measuring a physical quantity * Simulation: verification by simulating the code functionality without porting it to another software other than the one used for development   The foreseen verification method for each requirement item is mentioned in the following requirements table.  As the firmware/software developer will have in-depth knowledge about these parts, the intent should that he delivers a bug-free, tested and verified piece of firmware/software thus avoiding potential delays. Therefore, the acceptance tests that are foreseen within this document are not intended to verify that all the FW/SW blocks work as expected (these tests should have already been done by the developers ex. through simulations before delivery) but rather to focus on the system performance and the requirements as described in this document. The FW/SW developer shall still provide support to fix any bugs that may be detected later on such as those that may not be captured during the foreseen acceptance tests. | |

| **ID** | **Title** | **Description** | **Author** | **Date** | **Stake Holder** | **Approval**  **Status** |
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| LEBT-BCMpre-FD-001 | Measurement type | The ACCT system will be used to measure the LEBT beam current including pulse and no-pulse periods. The beam current data will then be further processed for machine protection purposes including pulse width, amplitude and frequency measurements.  Verification method: inspection  Verification result: verified -> no of samples should be divisible by 16 | Hooman Hassanzadegan | Feb. 24th 2016 | Matthias Werner |  |
| LEBT-BCMpre-FD-002 | Measurement range | The ACCT system needs to satisfy the requirements that are described in this document with the beam current ranging from 1 mA to 90 mA, pulse width ranging from 5 us to 6 ms and pulse rate ranging from 1/30 Hz to 14 Hz.    Verification result: FW was successfully tested with the RTM input voltage ranging from 10 mV to 1V (emulating current from 1 mA to 100 mA) and pulse width from 1us to 2.86 ms.  Also, current measurement and interlocks (lower, upper and errant thresholds) were successfully tested under two extreme conditions: 1) 2.86 ms pulse with repetition rate of 1/30 Hz, and 2) 5 us pulse with repetition rate of 14 Hz | Hooman Hassanzadegan | Feb. 24th 2016 | Matthias Werner |  |
| LEBT-BCMpre-FD-003 | Data display | The information on the user screen shall include (but not necessarily be limited to):  - Graphical display of the beam pulse with zoom-in possibility: the time window shall as minimum start shortly before the rising edge of the pulse, and end after the falling edge.  - Numerical display of the average current over the pulse flat-top (compliant with LEBT-BCMpre-FD-008 and LEBT-BCMpre-FD-032)  - Numerical display of the per-pulse charge (compliant with LEBT-BCMpre-FD-032)  - Numerical display of the cumulative charge from the time of a manual reset from the user screen (compliant with LEBT-BCMpre-FD-032)  - Numerical display of the pulse width (compliant with LEBT-BCMpre-FD-020)  - Numerical display of the external trigger frequency (compliant with LEBT-BCMpre-FD-020 and LEBT-BCMpre-FD-032)  - Access to settings through a separate tab    Verification method: inspection  Verification result: depends on OPI | Hooman Hassanzadegan | Feb. 24th 2016 | Hinko Kocevar |  |
| LEBT-BCMpre-FD-004 | Mode of operation | The ACCT system shall work in pulsed mode.  Verification method: inspection  Verification result: verified | Hooman Hassanzadegan | Feb. 24th 2016 | Matthias Werner | MW: approved |
| LEBT-BCMpre-FD-005 | Screen update rate | The ACCT data on the user screen shall be updated at a rate not lower than 1 Hz.  Verification method: measurement  Verification result: depends on OPI | Hooman Hassanzadegan | Feb. 24th 2016 | Hinko Kocevar | MW: Ok, will not be limited by firmware |
| LEBT-BCMpre-FD-006 | Custom firmware time resolution | The ACCT custom firmware shall output the ACCT data at the ADC clock rate.  Verification method: simulation  Verification result: verified | Hooman Hassanzadegan | Mar. 3rd 2016 | Matthias Werner | MW: approved |
| LEBT-BCMpre-FD-007 | Integration firmware time resolution | The ACCT integration firmware shall decimate the custom firmware output data at 8-to-1 rate. This data shall then be sent to software for post-processing and display on the user screen.  Verification method: inspection and simulation (if needed)  Verification result: verified. Raw data is available through the control system at the full ADC clock rate and processed data at 1/8 of the ADC clock rate. | Hooman Hassanzadegan | Mar. 3rd 2016 | Klemen Erjavec |  |
| LEBT-BCMpre-FD-008 | Display time resolution | The pulse data on the user screen shall be displayed with the integration firmware time resolution (i.e. LEBT-BCMpre-FD-007)  Verification method: inspection  Verification result: depends on OPI | Hooman Hassanzadegan | Mar. 3rd 2016 | Hinko Kocevar |  |
| LEBT-BCMpre-FD-009 | ACCT number | Only one ACCT is foreseen for this implementation.  Verification result: verified | Hooman Hassanzadegan | Feb. 24th 2016 | Hooman Hassanzadegan |  |
| LEBT-BCMpre-FD-010 | ADC clock | Three clock sources are foreseen  - An external 88.0525 MHz clock from the MRF timing receiver module through the crate backplane (default option)  - An external clock through the SMA or the Harlink connector on the AMC front-panel  - The free-running AMC clock  Clock multiplexing shall be done in the integration firmware. The custom firmware shall get only one clock (88.0525 MHz). All inputs and outputs shall be in the clock domain of this clock.  Verification result: FW works as expected with 1) AMC internal clock with clock frequency of 250 MHz/3 = 83.333 MHz. and 2) external clock connected to the SMA on the AMC with frequency of 88.0525 MHz  **CH0 got stuck after switching OFF and ON the external 88 MHz clock. The same problem happened on CH1 after a crate power cycle. ‘ALAArr\_ADC\_STUCK’ bit (in the PKG\_TYPES.vhd) is occasionally set during normal operation without making any changes in the clock configuration.**  Cosylab delivered a modified FW on March 15th 2017. The issue of ADC data getting stuck still exits. | Hooman Hassanzadegan | Feb. 24th 2016 | Klemen Erjavec |  |
| LEBT-BCMpre-FD-011 | External trigger specifications | An external trigger that is synched with the LEBT pulse shall be provided for the ACCT readout electronics.  The rising edge of the external trigger shall be received by the AMC at minimum 99 us and at maximum 101 us before the rising edge of the beam pulse.  The falling edge of the external trigger shall be received by the AMC at minimum 99 us and at maximum 101 us before the falling edge of the beam pulse.  Verification method: measurement  Verification result: external trigger with above-mentioned specifications depends on timing. No bugs were discovered using a lab setup with the timing intervals being as close as possible to the ideal case. | Hooman Hassanzadegan | Oct. 10th 2016 | Hinko Kocevar |  |
| LEBT-BCMpre-FD-012 | External trigger source | Two external trigger sources are foreseen:  - A trigger from the MRF timing receiver module through the crate backplane  - An external trigger through the Harlink connector on the AMC front-panel  Trigger multiplexing shall be done in the integration firmware. The custom firmware shall only have one trigger input.  Verification result: option 1 (external trigger from the timing receiver through the crate backplane) works as expected. Option 2 was not tested. | Hooman Hassanzadegan | Feb. 24th 2016 | Klemen Erjavec |  |
| LEBT-BCMpre-FD-013 | Interlock on external trigger | An interlock signal shall be sent out if the beam pulse does not arrive shortly after the external trigger (compliant with the “lower\_MPS\_threshold” under LEBT-BCMpre-FD-020)  Verification method: test with a waveform generator  Verification result: verified | Hooman Hassanzadegan | Oct. 10th 2016 | Matthias Werner |  |
| LEBT-BCMpre-FD-014 | Toroid type | The ACCT toroid will be of Bergoz wideband type with a bandwidth of 3 Hz to 1 MHz.  Verification method: inspection  Verification result: verified | Hooman Hassanzadegan | Feb. 24th 2016 | Hooman Hassanzadegan |  |
| LEBT-BCMpre-FD-015 | ACCT front-end electronics | The ACCT front-end electronics shall be of Bergoz ACCT-E type. The output voltage range of the ACCT-E shall be +/- 10 V for a full-scale current range of +/- 100 mA.  Verification method: inspection  Verification result: verified | Hooman Hassanzadegan | Feb. 24th 2016 | Hooman Hassanzadegan |  |
| LEBT-BCMpre-FD-016 | RTM type | The readout electronics shall use a Struck SIS8900 RTM.  Verification method: inspection  Verification result: verified | Hooman Hassanzadegan | Feb. 24th 2016 | Hooman Hassanzadegan |  |
| LEBT-BCMpre-FD-017 | ACCT Interface Unit | A custom ACCT Interface Module (AIM) shall be used for the interconnection of the ACCT-E output to the RTM input. This interface module will match the ACCT-E output voltage and impedance to those required by the RTM. Both the input and the output of the interface module will be single-ended.  The AIM shall have high-impedance input (that will be seen by the ACCT-E output) and 50 Ohm output (that will be seen by the RTM input).  The AIM shall have two identical output ports so that the ACCT signal can be measured simultaneously by two sets of readout electronics.  Verification method: inspection  Verification result: verified  The AIM shall have a gain of 0.1 thus giving an output voltage of -1 V to +1V with the input voltage ranging from -10 V to +10 V (corresponding to an ACCT current of -100 mA to +100 mA).  A custom ACCT Calibration Module (ACM) shall be used to generate a current pulse with a fixed amplitude of 50 mA for the ACCT calibration.  Verification method: measurement  Verification result: verified. The calibrator current drifts due to temperature variations was negligible.  The calibration pulse shall be enabled/disabled using an LVDS signal through the Harlink-OUT connector on the SIS8300-L2D front-panel.  Verification method: inspection  Verification result: verified. Two LVDS signals on the Harlink port are used to control a transistor and a relay on the calibrator module. | Hooman Hassanzadegan | May. 16th 2016 | Hooman Hassanzadegan |  |
| LEBT-BCMpre-FD-018 | AMC type | The readout electronics shall use a Struck SIS8300-L2D AMC  Verification method: inspection  Verification result: verified | Hooman Hassanzadegan | Feb. 24th 2016 | Matthias Werner, Hooman Hassanzadegan | MW: approved |
| LEBT-BCMpre-FD-019 | uTCA chassis and infrastructure | The following items shall be used for the chassis and the infrastructure modules:  - Schroff MicroTCA.4 system cube 5U-42HP with 6-slots.  - NAT MCH-PHYS Front module configured with: NAT-MCH-M4-Base12-GbE, SSCH + TCTCXO, PCIEx48 and FP1D. 128Gb 2.5” SSD  -NAT MCH-COMex Rear Module configured with: i7 COMex processor module, 1,7 GHz System Clock & 4Gb RAM  - NAT MicroTCA 600W Power Module. AC-DC Double Width Full Size (6 HP).  - MRF event-receiver timing module  Verification method: inspection  Verification result: verified. The 6-slot crate may be replaced with a compact 3U crate (provided by the ICS) for the Catania installation. | Hooman Hassanzadegan | Feb. 24th 2016 | Hinko Kocevar, Hooman Hassanzadegan |  |
| LEBT-BCMpre-FD-020 | ACCT custom firmware functionality | A custom firmware shall be developed for the LEBT ACCT system. The required functionality includes:  - Baseline level correction: when enabled, shifts the baseline level of the ACCT signal to zero Volt.  - Droop compensation: when enabled, compensates the droop to better than +/- 0.1% of the pulse current for the maximum pulse width and within the full current range.  Verification method: Verification result: verified  - Interlock signal generation on the pulse amplitude: when enabled, checks pulse current and generates an interlock if the current goes above a upper\_MPS\_threshold or below a lower\_MPS\_threshold. The upper\_MPS\_threshold check shall be done continuously. The time window for the lower\_MPS\_threshold shall start 103 us after the rising edge of the external trigger, and end 99 us after the falling edge of the external trigger.  - Errant beam detection: when enabled, generates an interlock if an errant beam is detected during the no-pulse period. The time window for the errant beam detection starts 104 us after the falling edge of the external trigger, and ends 98 us after the rising edge of the external trigger (next pulse). An MPS threshold shall be used for the errant beam detection.  Verification result: verified. Lower/upper and errant thresholds were checked. No error was found.  - A moving average filter shall be applied to the ACCT data. The time constant of this filter (assuming a step change at the input and 88.0525 MHz clk) shall be about 100 ns. When enabled, the filtered data shall be used for the pulse shape display as well as the two interlock signal generations that are mentioned above.  Verification result: Noise filter time constant is about 100 ns. Filtered data is used for the pulse shape display. | Hooman Hassanzadegan | Mar. 9th 2016 | Matthias Werner |  |
| LEBT-BCMpre-FD-021 | ACCT custom firmware functionality (cntd) | - ACCT calibration: the ACCT shall be calibrated in MANUAL and AUTO modes (compliant with LEBT-BCMpre-FD-032). A calibration current pulse with fixed amplitude (compliant with LEBT-BCMpre-FD-017) shall be sent to the calibration winding of the ACCT during the no-pulse period. The custom firmware shall make a small adjustment in the ACCT scale factor based on the read-back signal to calibrate the ACCT. Verification result: Cal pulse synchronization to the trigger still missing.  - Pulse width measurement: measures the total time within one pulse that the beam current is above a fixed level of 3 mA. This measurement shall be done within a time period that is complementary to the errant beam detection. Verification result: verified.  - Trigger frequency measurement: measures the repetition period of the external trigger with a time resolution of not more than 1 us (this number shall then be reversed in the software to give the trigger frequency, compliant with LEBT-BCMpre-FD-032). Verification result: verified.  - Pulse charge measurement: pulse current shall be integrated, thus giving per-pulse charge including rising and falling edges (compliant with: LEBT-BCMpre-FD-003). -> Verification result: It works, but the conversion factor is not clear (how does mA/64/88M converts into Coulomb? -> Matthias Werner reply on Feb. 27th 2017  - Average beam current measurement over the pulse flat top: the custom firmware shall integrate the pulse current from 104 us after the rising edge of the external trigger to 99 us after the falling edge of the external trigger. The integrated charge and the integration period shall then be sent to the software to calculate the average current by diving these two numbers (compliant with LEBT-BCMpre-FD-003 and LEBT-BCMpre-FD-032). -> Verification result: verified. flat-top time measurement verified; integrated charge over flat-top works, but conversion factor is not clear -> M. Werner’s email dated Feb. 27th 2017  - Common enable/disable input for the baseline-level correction and droop compensation. Verification result: verified.  - Enable/disable input for the interlock signal generations. Verification result: verified. | Hooman Hassanzadegan | Mar. 21st 2016 | Matthias Werner |  |
| LEBT-BCMpre-FD-022 | Latency | The total latency from the moment that the beam goes through the ACCT toroid until the moment that an interlock signal is generated on the AMC output pin shall not be more than 2 us. This includes toroid response time, cables, ACCT front-end electronics and digital processing.  Verification method: measurement  Out of the total delay budget mentioned above, the digital processing delay from ADC data in the FPGA to FPGA output alarm pin shall be 400 ns (MAX).  Verification method: simulation  Verification result: latency was not measured. | Hooman Hassanzadegan | Feb. 24th 2016 | Matthias Werner, Hooman Hassanzadegan |  |
| LEBT-BCMpre-FD-023 | Custom firmware deliverables | The custom ACCT firmware shall be delivered as a collection of files - with a designated top level file which will be the interface to the surrounding code designed by ESS or other parties. Three deliverables are foreseen:  - Signal port list of the VHDL top module -> verified  - Complete VHDL code, tested by simulation -> verified  - Documentation -> Complete documentation still missing  Technical details shall be based on discussions (emails, skype meetings etc) between the DESY and the ESS contact persons. | Hooman Hassanzadegan | Feb. 24th 2016 | Matthias Werner | Approved |
| LEBT-BCMpre-FD-024 | Custom firmware acceptance tests | The custom firmware performance shall be tested and verified against the requirements described in this document before an official delivery takes place. When applicable, firmware functionality shall be tested on a BCM test bench at ESS using a waveform generator with external trigger.  The ACCT code developer shall be responsible for bug fixings and modifications if the code does not satisfy any of the requirements.  Verification result: FW functionality is consistent with this document and sufficient for the Catania tests. ADC stuck data remains to be checked in more details. | Hooman Hassanzadegan | Mar. 4th 2016 | Hooman Hassanzadegan |  |
| LEBT-BCMpre-FD-025 | Integration firmware | The ACCT custom firmware shall be integrated into the generic Struck SIS8300-L2D firmware provided by Struck. The integration firmware shall be tailored to the ESS BCM requirements in terms of clock multiplexing, register and memory maps, data decimation etc.  Verification result: verified. | Hooman Hassanzadegan | Feb. 24th 2016 | Klemen Erjavec |  |
| LEBT-BCMpre-FD-026 | ACCT firmware acceptance tests | The integration firmware shall be tested and verified against the requirements described in this document before an official delivery takes place.  The code integrator shall be responsible for bug fixings and modifications if the code does not satisfy any of the requirements that are relevant to the integration of the ACCT custom code into the generic firmware.  Verification result: FW functionality is consistent with this document and sufficient for the Catania tests. ADC stuck data remains to be checked in more details. | Hooman Hassanzadegan | Feb. 24th 2016 | Hooman Hassanzadegan |  |
| LEBT-BCMpre-FD-027 | Custom firmware milestones and schedule | A very simple "Integration Test Version" (ITV) of the ACCT custom code shall be delivered by DESY ahead of the Catania (i.e. “Cat” as shown below) version. The “ITV” version shall be used for defining interfaces (including ADC, DDR, parameters, MPS alarm output) and integration tests well ahead of the delivery of the “CAT” version.  Custom firmware deliverables (by DESY) shall be according to the following schedule:  - Port def.  ITV:   2 months after “start”  - Code ready ITV:   4   "      "     "  - Port def.  Cat:   3   "      "     "  - Code ready Cat:   9   "      "     "  - Port def.  LEBT:  6   "      "     "  - Code ready LEBT: 16   "      "     "  - Docum. complete: 19   "      "     "  \* Here, “start” refers to the start of the custom code development by DESY that shall happen right after a contract agreement between DESY and ESS.  Verification result: the above-mentioned items except complete documentation have already been provided by DESY | H. Hassanzadegan | Mar. 4th 2016 | M. Werner |  |
| LEBT-BCMpre-FD-028 | Integration firmware milestone | ACCT firmware with integrated custom code shall be delivered by cosylab not later than 1.5 months after the “Code ready Cat”.  Verification result: verified. | H. Hassanzadegan | Oct. 10th 2016 | Klemen Erjavec |  |
| LEBT-BCMpre-FD-029 | BCM software milestone | ACCT software by ESS-BI shall be available not later than 1.5 months after the delivery of the “Code ready Cat”.  Verification method: inspection | H. Hassanzadegan | Oct. 10th 2016 | Hinko Kocevar |  |
| LEBT-BCMpre-FD-030 | Custom-code interface | Parameters relevant to the custom-code interface including bit sizes and data rates shall be provided by the ACCT custom code developer based on the foreseen application that is described in this document.  Verification result: verified. | Hooman Hassanzadegan | Mar. 3rd 2016 | Matthias Werner | Approved |
| LEBT-BCMpre-FD-031 | Firmware-software interface | The code integrator shall use both the LEBT-BCMpre-FD-030 interface definition and this functional description to define a custom register array memory map for the firmware-software interface. This interface definition shall include register addresses, definition of functions as well as register types and lengths.  Verification result: verified. | Hooman Hassanzadegan | Mar. 3rd 2016 | Klemen Erjavec |  |
| LEBT-BCMpre-FD-032 | Software functionality | The signal processing that will be performed on the ACCT signal in software shall include (but not necessarily be limited to):  - Average current over the pulse flat-top shall be calculated by dividing the integrated charge by the integration period (compliant with LEBT-BCMpre-FD-003 and LEBT-BCMpre-FD-021)  - Cumulative beam charge shall be measured by adding up the charge of consecutive pulses. The user shall be able to reset the cumulative charge value by pressing a reset button on the user screen (compliant with: LEBT-BCMpre-FD-003).  - Repetition period of the external trigger shall be reversed to give the trigger frequency (compliant with: LEBT-BCMpre-FD-003 and LEBT-BCMpre-FD-021).  The controls on the user screen shall include (but not necessarily be limited to):  - ADC clock source (compliant with LEBT-BCMpre-FD-010)  - Trigger source (compliant with LEBT-BCMpre-FD-012)  - MANUAL/AUTO/OFF switch for the ACCT calibration mode. With the MANUAL mode, calibration shall be done during the next no-pulse period after pressing a button on the user screen. With the AUTO mode, calibration shall be done regularly and the calibration frequency (i.e. no of calibrations per 24 hours) will be set by the user.  - Upper and lower MPS thresholds for the pulse current (compliant with LEBT-BCMpre-FD-021)  - MPS threshold for errant beam detection (compliant with LEBT-BCMpre-FD-021)  - Enable/disable switch for the moving average filter (compliant with LEBT-BCMpre-FD-021)  - Common enable/disable switch for the baseline level correction and droop compensation (compliant with LEBT-BCMpre-FD-021)  - Enable/disable switch for interlock signal generation (compliant with LEBT-BCMpre-FD-021)  The user shall be able to see the MPS-related error/threshold types on the user screen after a beam abort occurred (compliant with LEBT-BCMpre-FD-021).  Verification method: inspection | Hooman Hassanzadegan | Mar. 3rd 2016 | Hinko Kocevar |  |
| LEBT-BCMpre-FD-033 | EPICS support | The ACCT readout electronics shall be integrated into EPICS. The read-out data and control of settings shall be all available to the user on a user screen.  Verification method: inspection | Hooman Hassanzadegan | Feb. 24th 2016 | Hinko Kocevar |  |
| LEBT-BCMpre-FD-034 | ADC coding | The ADC shall be configured to output format “Offset Binary Output Mode” or “Twos Complement Mode” by the framework (TBC).  Verification result: verified. | M. Werner | Mar. 3rd 2016 | Klemen Erjavec |  |
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