

BCM verification plan

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Outline



- Naming convention
- Data management system: Insight
- Acceptance tests workflow
- BCM tests description
- After-installation tests

Naming convention



- Every Field Replaceable Unit (FRU) is named. A FRU can be a simple part or an assembly
 - Ex: FEB-050ROW:PBI-PPC-002 for a cabinet cable
- Naming convention:

Sec-Sub:Dis-Dev-Idx

Two major areas of FRU installation slots are identified:

- tunnel: including stub, tunnel wall and gallery wall,
- support: front end building (FEB), klystron gallery, gallery support area (GSA) in A2T
- → System name is not misused!

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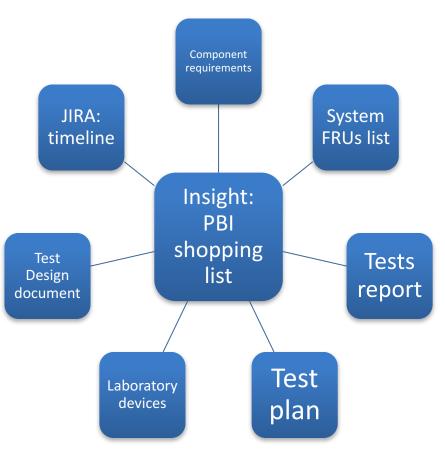
Data management system

- Data export / import with other software tools
- Systems and subsystems tests results coming from different locations (ESS, IK Partner, Industry partners...)
- We must be able to trace back acceptance tests results to laboratory measuring devices
- We need to be able to prepare an installation batch when an installation slot is ready: need for a dynamic tool
 - → Having a reliable Data management system is critical!



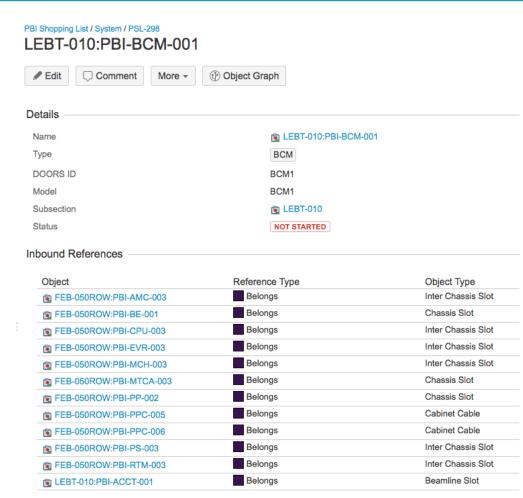
- Ensures traceability between tests and production data, system components and laboratory devices.
- Objects' attributes store all FRU info: responsible, current status (procured, received, RFI...) etc.
- Added value, current installation or production progress... can be automatically extracted for each system or FRU
- Timeline is managed in Jira, tasks are linked to Insight.

We do not want to replace CHESS!



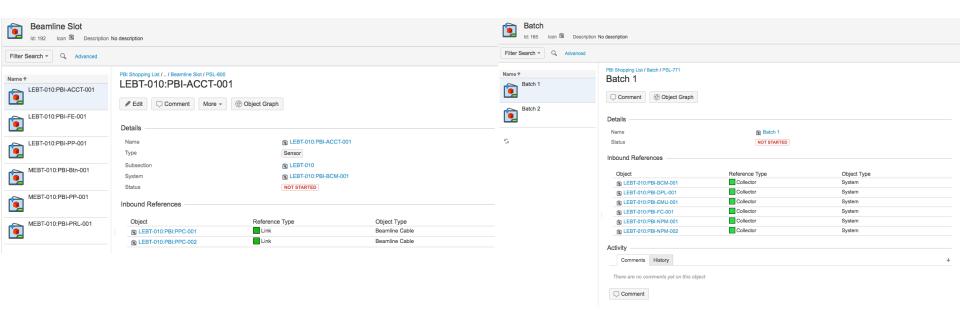


- Change of status are triggered when all required documents and conditions are met.
- ICS database requirements are being defined. It will be automatically populated from Insight when available.



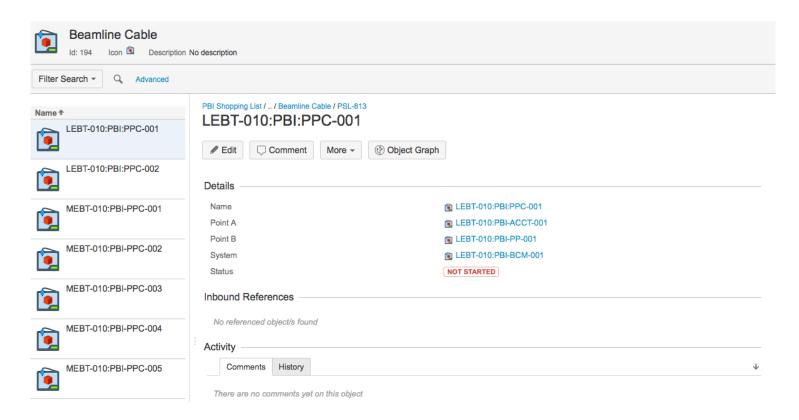


- No lost effort, as everything can be scripted to populate external tools and extract any needed information!
- Installation batch: installation status easily verified and prepared
- Data is uploaded by BD team. Training IK and industrial partners on that is possible.





- Hierarchy goes down to systems cables and their status and properties
- Example of a Beam line cable connecting an ACCT to a Patch Panel:





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Measurements files format

- Large amount of measurements parameters: Data logged in HDF5 and uploaded to Insight.
- Data files produced at ESS follow a fixed format: Files, groups and datasets mandatory attributes are defined.
- Existing data received from IK and industry partners is stored as is for now, adding the needed metadata. Reformatting to HDF5 is planned for each test results.





System tests requirements

• Tests requirements are defined for each subsystem

Test plan

- Describes subsystems' test setup and characterization procedures
- When not COTS: test plan is prepared/discussed and agreed with IK partner

Test Design Document

- Design document is validated by system lead: we make sure test requirements are correctly translated
- Test coverage is reviewed. Possible risk assessment if we do not reach 100% coverage
- Tests IDs defined for each measurements

testbench implementation • Test system implemented in python.

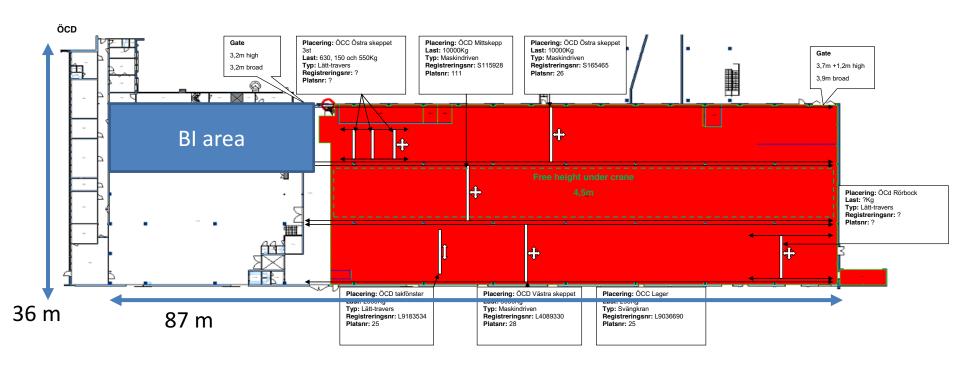
Run tests

- Acceptance tests performed in RATS
- Data logging in Insight



Where do we test our systems?

RATS preliminary layout



Acceptance tests workflow



- RATS: Component received.
- RATS: Component tested.
- RATS: Component stored.
- RATS: System assembly and test → RFI
- RATS: System stored
- Installation slot: System goes to ESS AT site.
 - Guideline: Install and test as much as possible, as early as possible
 - Learning curve will help us moving faster with installation work after the first systems are processed
- Last step: commissioning





When struck digitizer boards are received, acceptance tests are performed to characterize the ADC on all channels:

Parameter	Test description	Pass/Fail thresholds
ADC SNR	Using low noise & distortion Generator	65 dBc
ADC SFDR	Using low noise & distortion Generator	65 dBc
ADC SINAD	Using low noise & distortion Generator	60 dBc
ADC ENOB	Using low noise & distortion Generator	11.5 bits
RTM clock source	Test the ADC clock using the RTM input as source	





The next tests then include the complete system, from toroid +FE to digitizer card:

Parameter	Test description	Pass/Fail thresholds
Current measurement range	Measure non linearity on a full scale input waveform	Non linearity < 0.1 % FS
Pulse rise time	Measure pulse rise time, sweeping pulse amplitude until 80 mA.	< 300 ns (cable length < 20m)
latency	Measurement of response time from current through toroid to AMC/RTM digital output.	< 2 us (cable length < 20m)
Droop	Acquire a 6 ms pulse, measure droop value	< 2% per ms





Parameter	Test description	Pass/Fail thresholds
Noise	Measure noise in lab conditions. Adjust threshold after first tests.	< 1% (RMS) FS
Temperature induced drift	Measure signal drift vs temperature over a range of xx degC	< +/- 1% FS
Bandwidth	Measure data acquisition system's bandwidth: sweep sine input frequency until 3 MHz	> 1 MHz (cable length < 20m)
Overshoot	Sweep pulse amplitude until 80 mA, measure overshoot	Time and amplitude thresholds to define

Uploaded to database:

- ACCT-E calibration data
- Automated electronics tests results: output of the tests described in the table above.
- Production tests results from manufacturer (Bergoz)

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After-installation tests sequence

- After-installation tests sequence:
 - initial first-time commissioning: test_ID
 - cold check-out: test_ID
 - commissioning with beam: test_ID
 - quick self-check: test_ID
- Sequential testing is important (tests timestamps are checked automatically). Otherwise the statement: "the instrument is installed and working properly" has less confidence.
- During debugging:
 - Relevant tests in each architectural layer are repeated until satisfactory results are obtained.
 - If the problem is identified and can be isolated within its layer, there is normally no need to repeat all of the tests which are sequentially following. Depending on the situation, some test might become mandatory nevertheless (for instance a software recompilation might entail a standard interface check, and a repaired connector might entail a signal transmission check).



After-installation tests sequence

- Cold check out: Testing of the whole instrument on all architectural layers:
 - monitor, front-end electronics, cables, mTCA-electronics, timing, data treatment, publishing, network transmission and machine protection interface.
- Commissioning with beam: Aims at verifying the correctness of the integration for machine operations.
 - Includes initial comparisons and cross-calibrations in order to gain confidence in the instrument. Performance limiting factors are identified.
- Quick self test: The self-test procedure includes testing of calibration, machine protection and data transmission.



Thank you!

Questions?