Preliminary System Design		
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ESS icBLM Preliminary System Design

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1. INTRODUCTION

The BLM system is one of the primary diagnostic system of the ESS LINAC for beam tuning and equipment protection. The system is designed to prevent hardware destructions, to avoid cavity quenches and/or degradation, in SC section of LINAC and to provide quantitative loss values. icBLM stands for ionization chamber Beam Loss Monitor, which is sued for continuous surveillance of particle losses. Ionization chambers are a compromise among high dynamic range to able to detect fast and slow losses, time resolution, RAMI (reliability, availability, maintainability, inspectability), radiation hardness and cost.

The icBLM system is one component of a diverse and redundant suite of iinstrumentation to diagnose and protect against beam losses. The other systems include the neutron BLM (nBLM) system and the BCM system. Additions to this suite may be considered after commissioning. These potential additions include Cherenkov detectors, phase and position monitors, and other advanced techniques and systems.

The ESS LINAC is depicted in the diagram below:

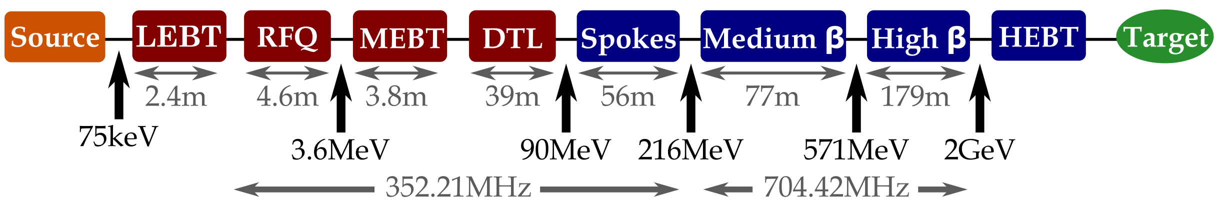

Figure 1: ESS LINAC

Particles deviating from the design orbit may eventually hit the aperture limit, these are beam losses. Their impact in the vacuum chamber produces "particles showers".

The charged particles ionise the nitrogen gas within the chamber. The liberated electrons and ions are collected at the electrodes due to an applied electrical field. The induced current is proportional to the particle flux. It is important to operate the detector in its linear region.

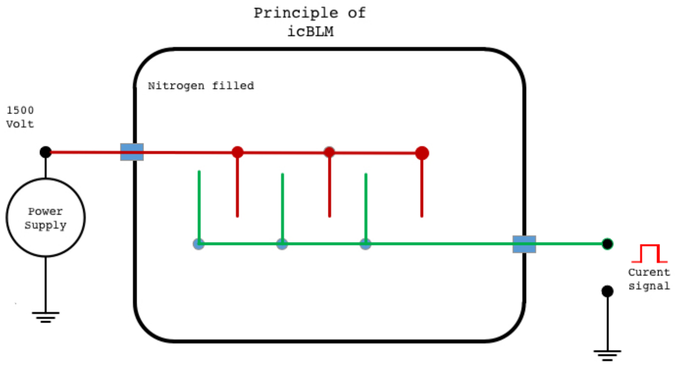

Figure 2: Ionization chamber working principle

icBLMs detectors are installed all along the LINAC from the DTL on up to the A2T section.

1.1 Detectors location

The number of ionization chambers deployed per LINAC section is summarized in the table below:

LINAC section	Number of ionization chambers	Comment
DTL	5	1 per Tank
Spokes	52	
Medium Beta	36	
High Beta	84	
HEBT	45	3 per q-pair
Dog leg	21 2	3 per q-pair 1 per dipole
A2T	15	
Dump line	6	

Total	266	

Detectors location is planned as follows: 4 devices are installed where there is a cryomodule, 3 in the transport section in the superconducting LINAC:

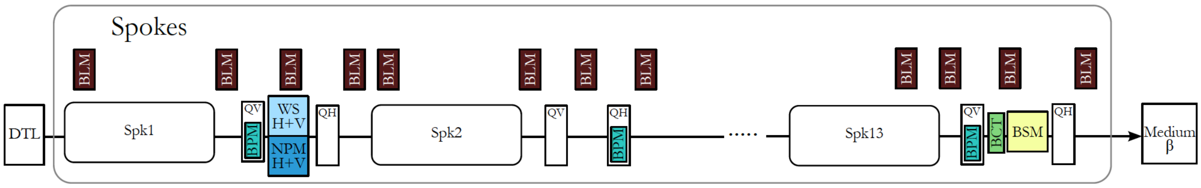

Figure 3: icBLM detectors locations

2. SYSTEM BLOCK DIAGRAM

The icBLM complete acquisition chain is composed of the Field Replaceable Units (FRU) listed in the table below. Support FRU are installed in a micro TCA crate in a 47U rack, as specified by Beam Diagnostics and provided by WP15.

Unit description	Installation area	Comment	Entity
Current readout	Support	FMC or custom acquisition crate	CAENels FMC-PICO. The unit is detailed in section 4
High voltage supply	Support	1 is needed per mTCA chassis	CAENels HV-PANDA. The unit is detailed in section 4
Timing Receiver	Support	Event receiver for triggers and clock	The unit is provided by ICS.
Power supply	Support	Power supply for mTCA chassis	The unit is provided by ICS.
Central Processing Unit	Support	CPU for mTCA chassis, Intel i7	The unit is provided by ICS.
Chassis	Support	The microTCA chassis	3U microTCA crate. The unit is provided by ICS.
MicroTCA Carrier Hub	Support	1 is needed per mTCA chassis	The unit is provided by ICS.
Rack	Support	Electronics rack	The unit is provided by WP15 and specified by BI.
Rack patch panel	Support	Installed on top of the rack	The patch panel will be designed by WUT
Sensor	Tunnel	Ionization chamber	The unit design is detailed in section 3

Beam Line Element Patch Panel	Tunnel		

Table 1: icBLM Field Replaceable Units

The design concept, based on 2 different architectures, is further detailed in the block diagrams below. A readout unit based on a Commercial Off The Shelf (COTS) solution is the baseline at this stage. An alternative solution using a custom acquisition crate will be evaluated.

The COTS current readout unit based solution is illustrated below:

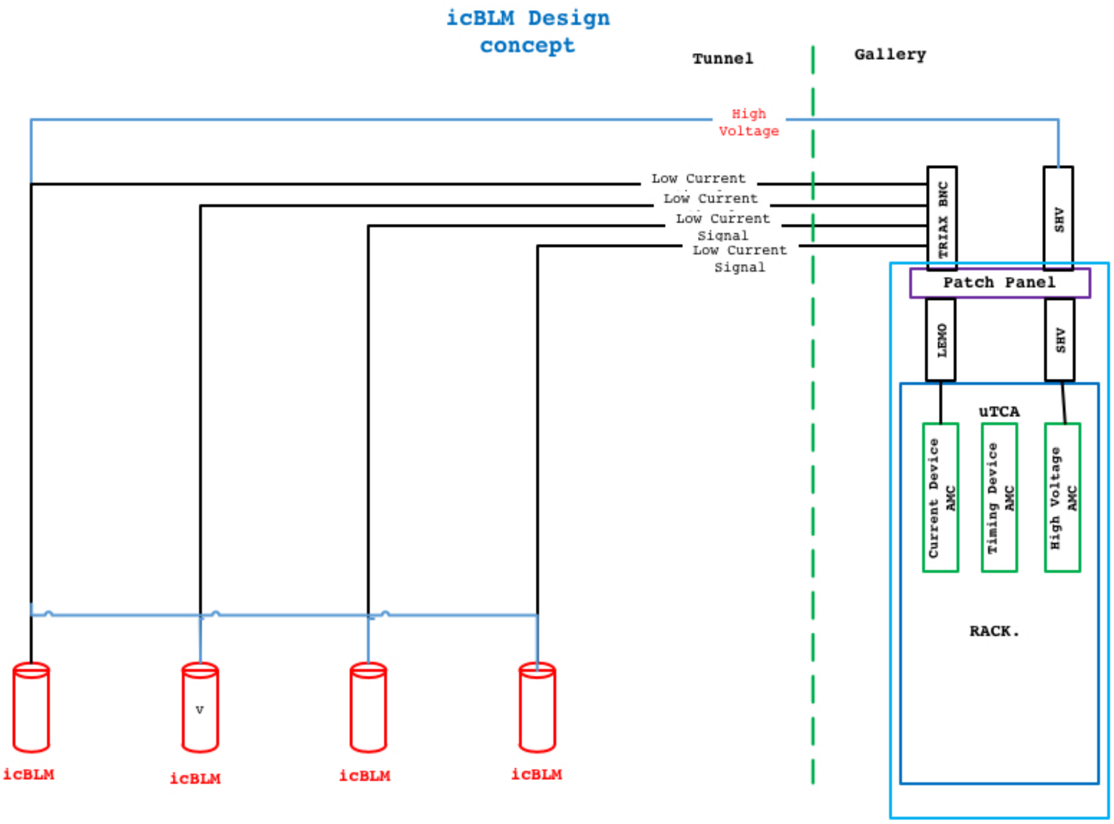

Figure 4: icBLM design concept - AMC COTS current readout

All electronics modules in the conceptual design above are hosted in a uTCA.4 crate. The crate interfaces to the global ESS control system include an EPICS IOC (Channel Access). The microTCA crate is placed in a rack installed in the Klystron Gallery. A patch panel on top of the rack is used to connect to a maximum of 8 ionization chambers per AMC current acquisition unit. Quality and availability aspects that have been driving this design are detailed in section 9.

No patch panel is planned to be installed next to the ionization chambers in the tunnel, except to support some additional temporary or movable detectors throughout the tunnel.

An alternative system design solution, based on a current to frequency custom acquisition crate added to the architecture is detailed in Figure 5:

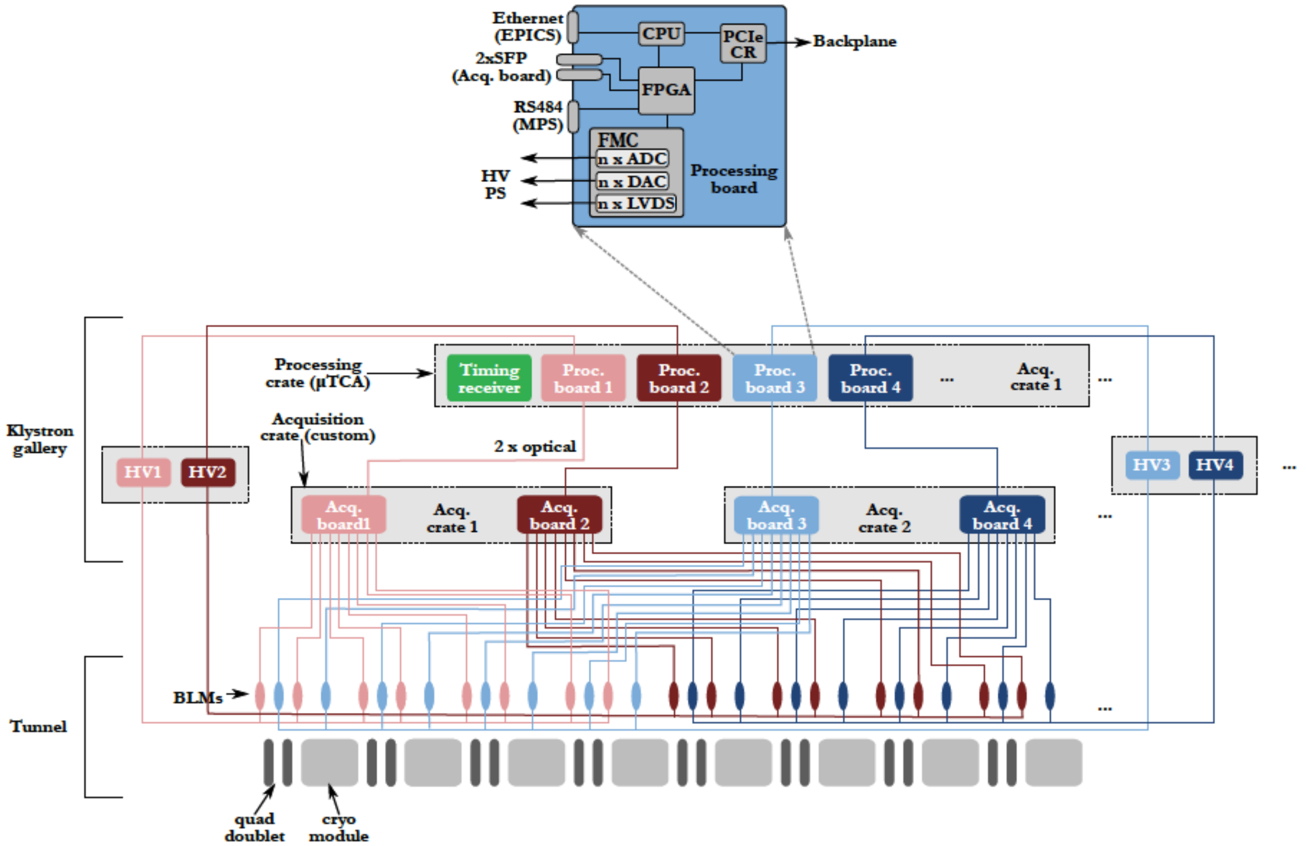

Figure 5: icBLM design concept – custom acquisition crate

These two solutions will be described in more detail in Section 4. In both design cases, the interface to the BIS shall be provided by ICS and include an FPGA module in the microTCA crate with an industry standard interface to the protection function. The protection function is provided by beam diagnostics.

Triggers are provided by the Event Receiver in both design choices. This Event receiver is provided by ICS, and listed in the system's Field Replaceable Units.

ICS division is responsible for delivering all the framework components that are required for icBLM specific application design and development.

3. IONIZATION CHAMBERS

3.1 Mechanical Design

Signal speed and robustness against ageing were the main design criteria. Each monitor is permanently sealed inside a stainless-steel cylinder. The quality of the welding was a critical aspect during production. To avoid radiation aging (up to 2.10^8 Gy in 20 years) the production of the chambers followed strict UHV requirements. Due to the required dynamic range of 10^8, the leakage current of the monitors has to stay below 2 pA.

Several tests during and after production were performed at IHEP (Protvino) and CERN. Consequently, no gain variations are expected on the icBLMs for 20 years of operation.

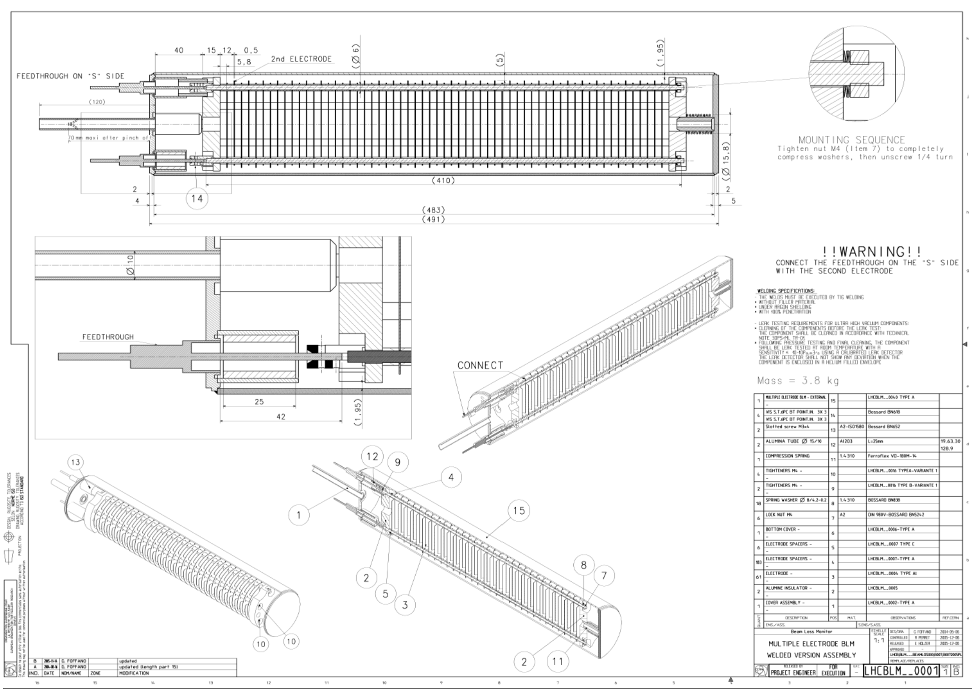

Figure 6: ionization chamber mechanical design

3.2 Production status, including tests overview

The ionization chambers have been tested at CERN and 285 monitors were shipped to ESS in June 2017.

The acceptance tests consist of 2 main tests:

- Leakage current measurement, which should be less 2 pA:

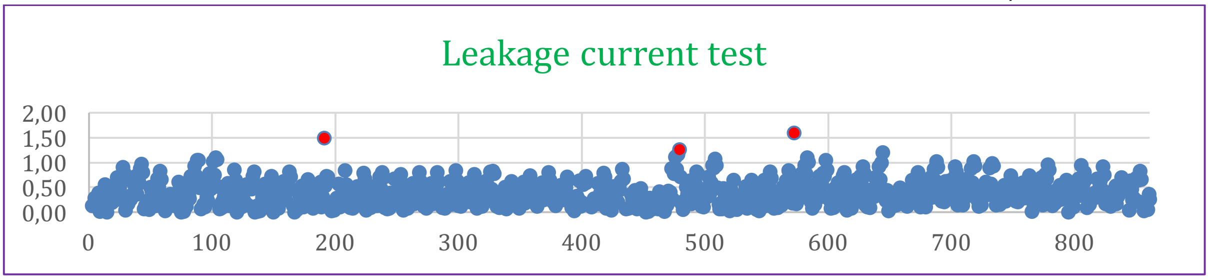

Figure 7: ionization chambers leakage current test

- The signal under irradiation versus a defined threshold:

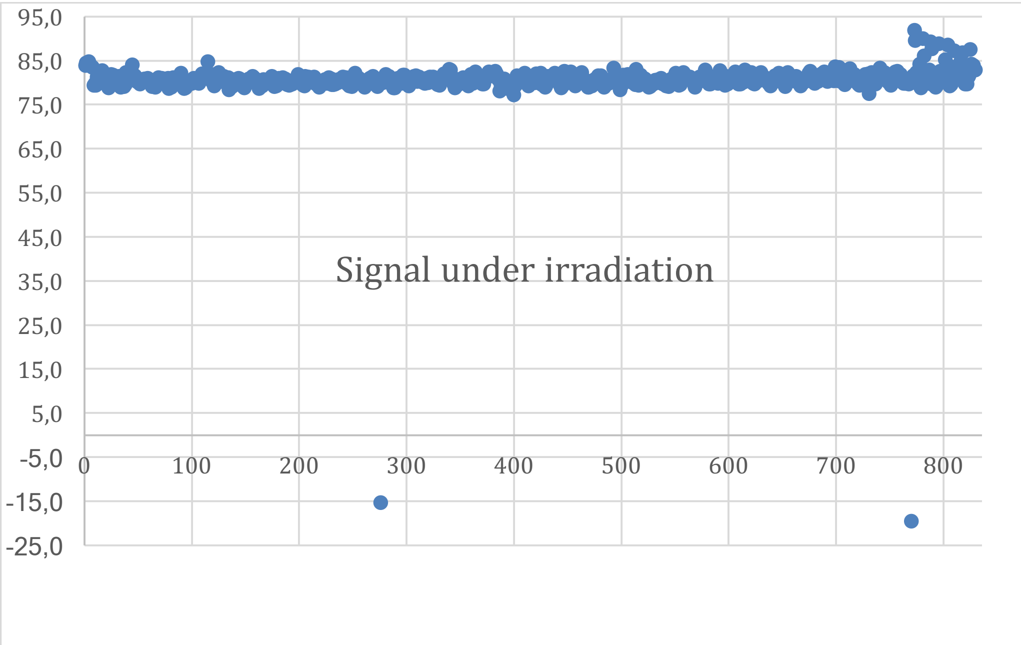

Figure 8: ionization chamber - irradiation test

3.2 Signal expectation

Name	Description
Leakage current	Less than 1-2 pA
Conversion factor	5.25 E-5 C/Gy
Energy Cut-off	*Protons, neutrons ~ 30 MeV *Electrons, photons ~ 2 MeV

Electron and Ion drift time	Electrons: 1/e fit of max is ~ 50 ns, all electrons collected is ~300ns Ions: 1/e fit of max is ~ 83 microsec, all ions collected is ~300 microsec
Dynamic range	**Chamber's current is 10^8, in range 50 pA to 0.5 mA**

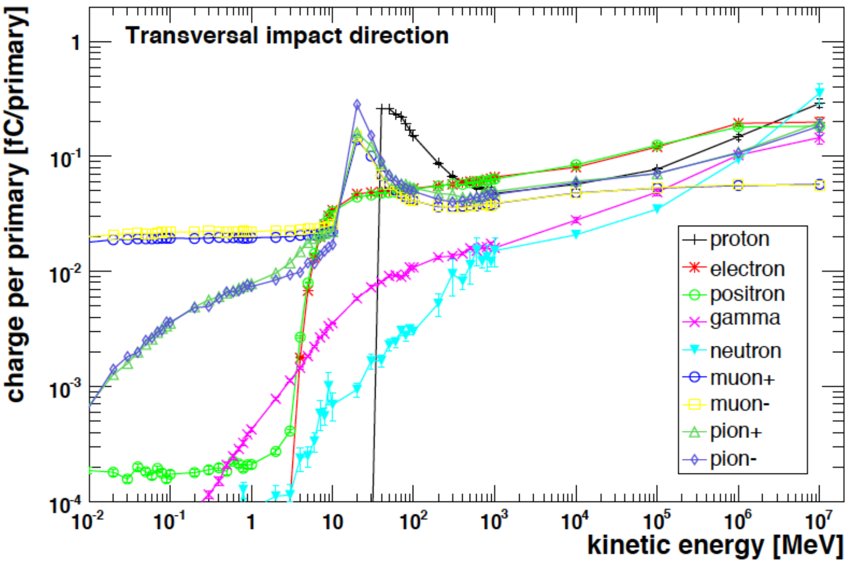

Figure 9: Ionization chamber response function (M.Stockner)

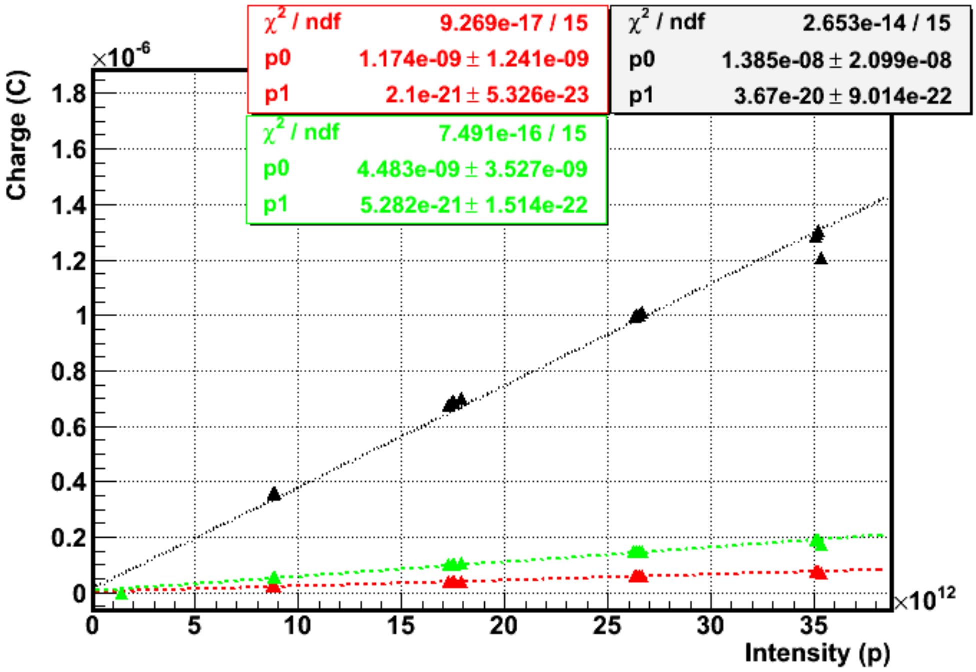

Figure 10: Plot of the integrated charge (over 40 us), Sep 2015 at HRM. Tests performed at CERN.

4. ELECTRONICS

4.1 High voltage power supply

The ionization chamber high voltage supply shall comply with the following requirements:

Name	Description
Modulation	Self-testing the ion chamber channels by modulating HV bias voltage shall be possible
Output voltage rating	The High voltage power supply providing the polarizing voltage to the ion chamber electrodes shall be able to provide a positive voltage of at least 3 kV
Output power	The High voltage power supply should feature a maximum output power of at least 5 W
Output voltage ripple	The High voltage power supply should feature an output voltage ripple below 4 ppm pk-pk/FS
Noise figure	The High voltage bias supply noise figure shall be compatible with that of the signal acquisition board. This includes temperature induced noise

Possible candidates for the high voltage power supply unit have been identified. Their noise performance fit the ones of the current acquisition devices described in the next section.

- CAENels HV-PANDA
- CAENels High Voltage unit used in the nBLM design

These possible power supplies will be evaluated, and the design choice will be made based on the results of these measurements.

The HV power supply test plan includes the following main tests: Modulation, output voltage range, output voltage ripple, noise figure.

4.2 Current acquisition

The signal readout unit supply shall comply with the following requirements:

Name	Description
Dynamic range	Input current dynamic range: 10 nA to 10 mA.

Response time	NC LINAC: Calculated melting time values of 3-4 us SC LINAC: 10 us The signal acquisition car shall therefore feature a bandwidth of at least 300 KHz and a minimum sampling rate of 1MSPS
Maximum input voltage	The signal acquisition card shall have an input protection of at least xx V
Crosstalk	The crosstalk between all channels on the signal acquisition board shall be below xx % FS
Resolution	The signal acquisition card shall have a resolution of at least 20 bits
Noise figure	The signal acquisition card shall have a typical noise better than 10 nA in its lowest range, including temperature induced noise

Table 2: Signal readout unit specifications

Possible candidates for this unit have been identified. The preliminary evaluation results of these devices are detailed in the next sections.

4.2.1 CAENels FMC-PICO

This picoammeter is a 20 bits 4 channels floating 1 MSPS ammeter. A CAENels DAMC-FMC25 full size standard AMC board hosts 2 PICO-8 FMC mezzanine cards.

The main digitizer specifications from the manufacturer are as follows:

- Full scale ranges of 10 mA and 500 uA
- Input bandwidth of 300 KHz

A testbench has been design in order to verify that this digitizer solution fits the system specifications.

A Keithley 6221 current source is used to generate pulses from ranging from 5 us to 2.86 ms, amplitude is changed from 500 nA to 8 mA. The testbench is depicted in the schematic below:

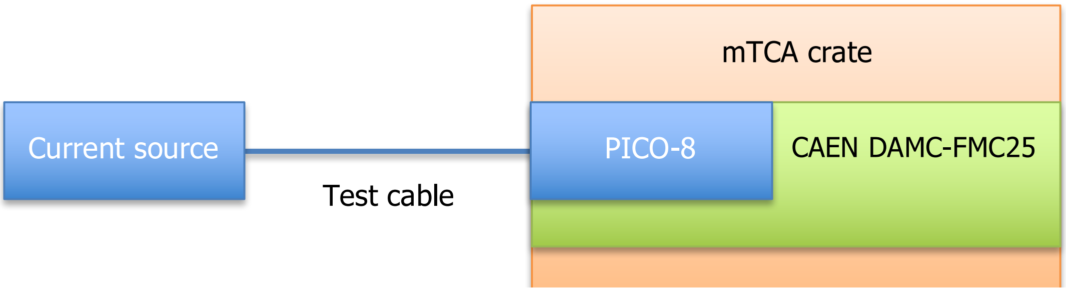

Figure 11: CAENels PICO-8 testbench block diagram

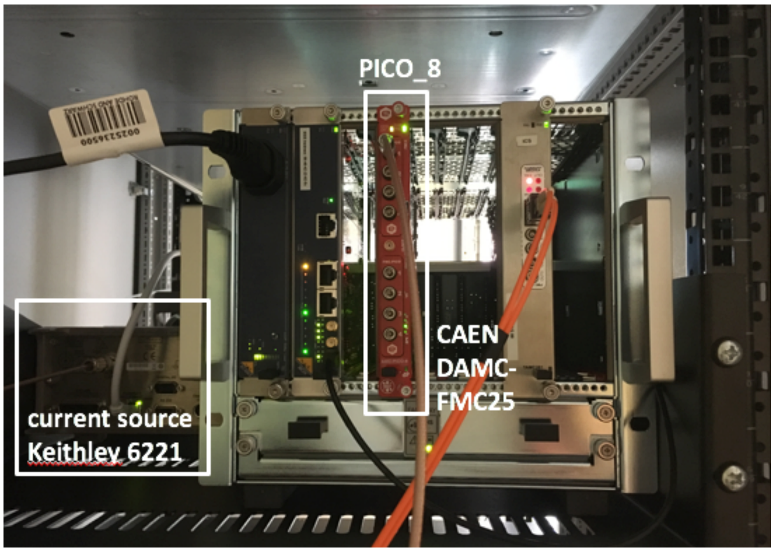

Figure 12: CAENels PICO-8 testbench

The test cable is a 1 m triaxial cable. The outer shield is grounded at the FMC side. The bloc diagram below describes a single channel:

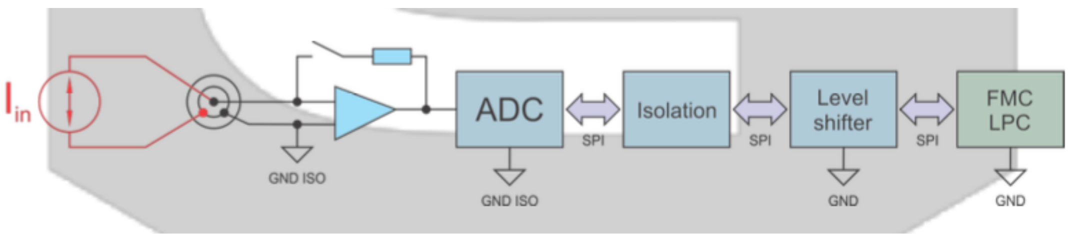

Figure 13: PICO-8 single channel bloc diagram

Current pulse test parameters are as follows:

Parameter	***Value***	***Comment***
Pulse width	5 us to 2.86 ms	2 us settling time on Keithley 6221

Pulse amplitude	800 nA to 8 mA	
Sampling frequency	1 MSPS	Max sampling frequency
Acquisition time	10 ms	10000 points acquired at 1 MSPS

- Noise levels, as measured by manufacturer vs measured at ESS:

PICO-8 Range	***CAENels***	***ESS testbench***
10 mA range	190 nA	195 nA
500uA range	10 nA	10 nA

Test conditions: 1σ,10000 points acquired at 1 MSPS.

- Bandwidth (3dB), as measured by manufacturer

PICO-8 Channel	***CAENels, 10mA range***	***CAENels, 500uA range***
Ch 0	301 kHz	300 kHz
Ch 1	294 kHz	292 kHz
Ch 2	299 kHz	299 kHz
Ch 3	303 kHz	391 kHz

- Shortest current pulse (5 us), at lowest and highest amplitudes:

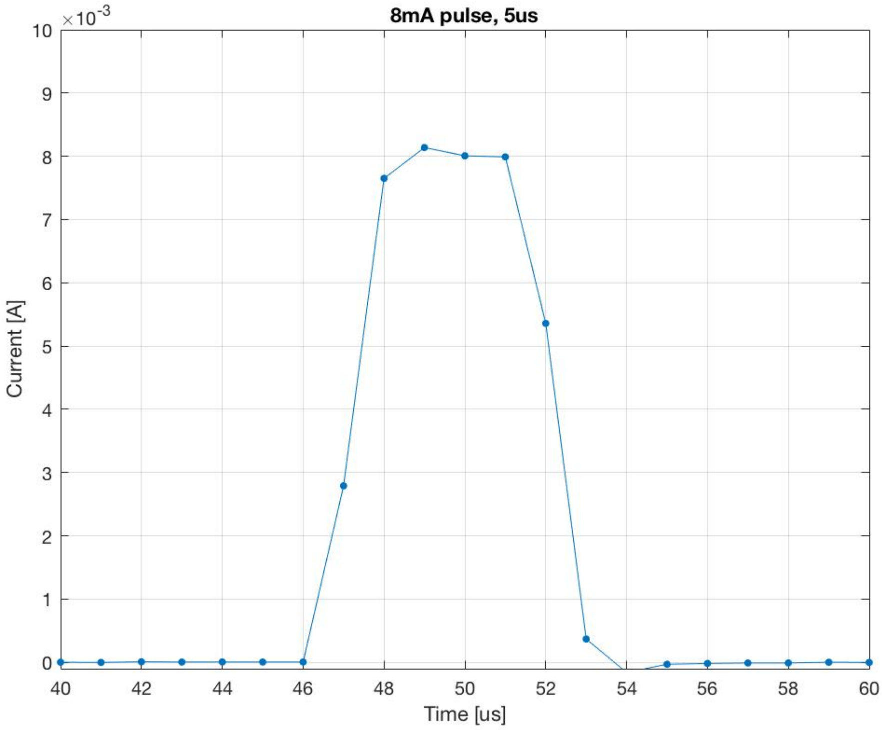

Figure 14: 5 us 8mA current pulse acquisition

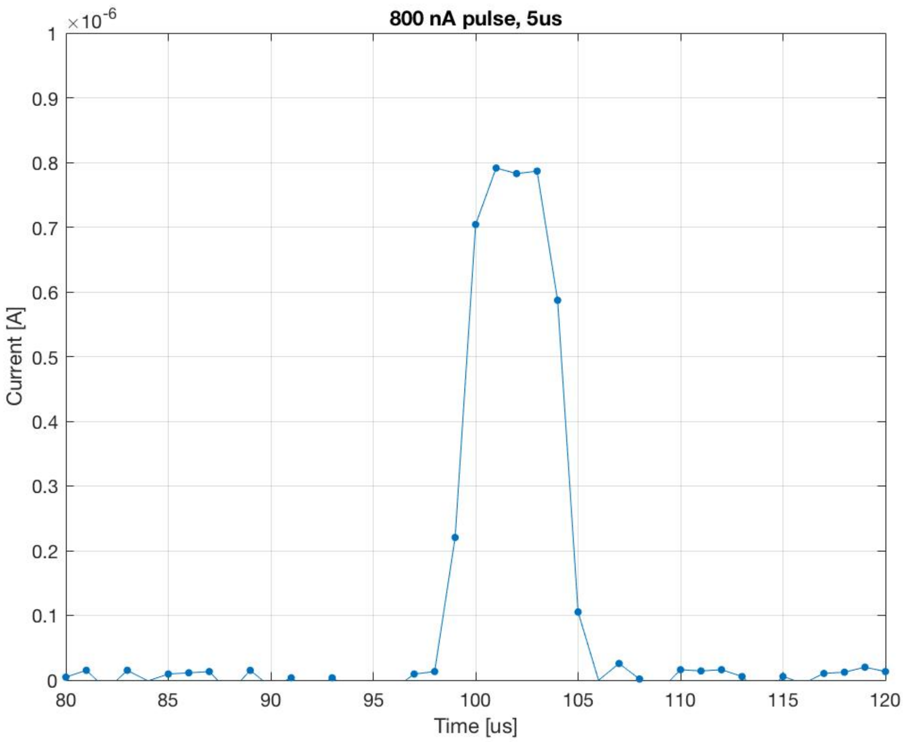

Figure 15: 5 us 800 nA current pulse acquistion

- Longest current pulse (2.86 ms) at shortest and highest amplitudes:

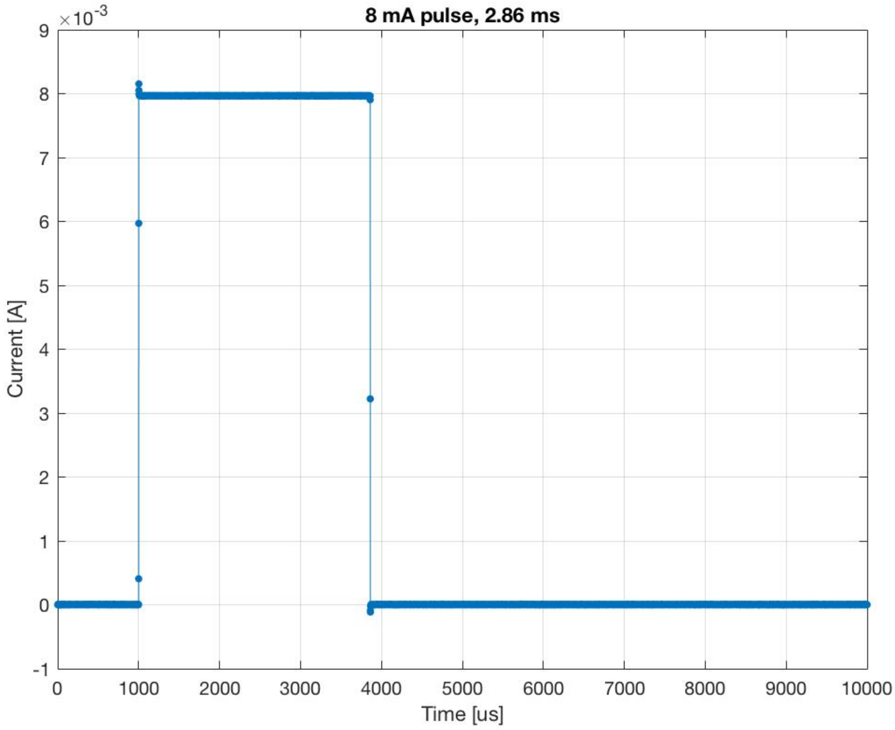

Figure 16: 2.86 ms, 8 mA current pulse acquisition

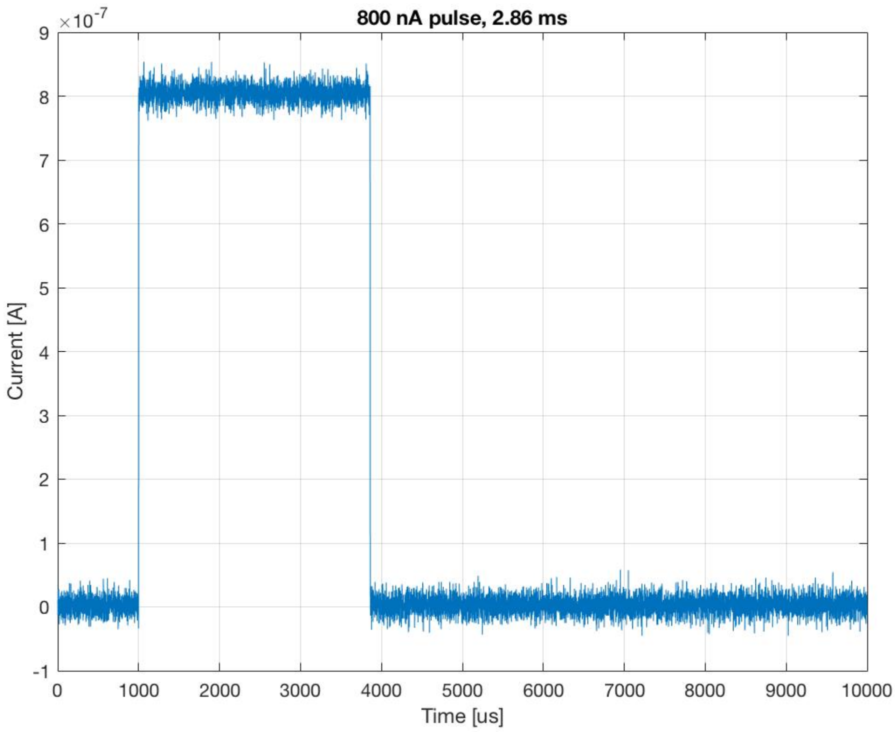

Figure 17: 2.86 ms, 800 nA current pulse acquisition

In the following tests, the triaxal test cable between the current source and the ammeter has been replaced with an off-the-shelf 50m coaxial cable. The effect of applying a basic moving average on measurement data has then been assessed.

- Longest current pulse (2.86 ms), 800 nA amplitude:

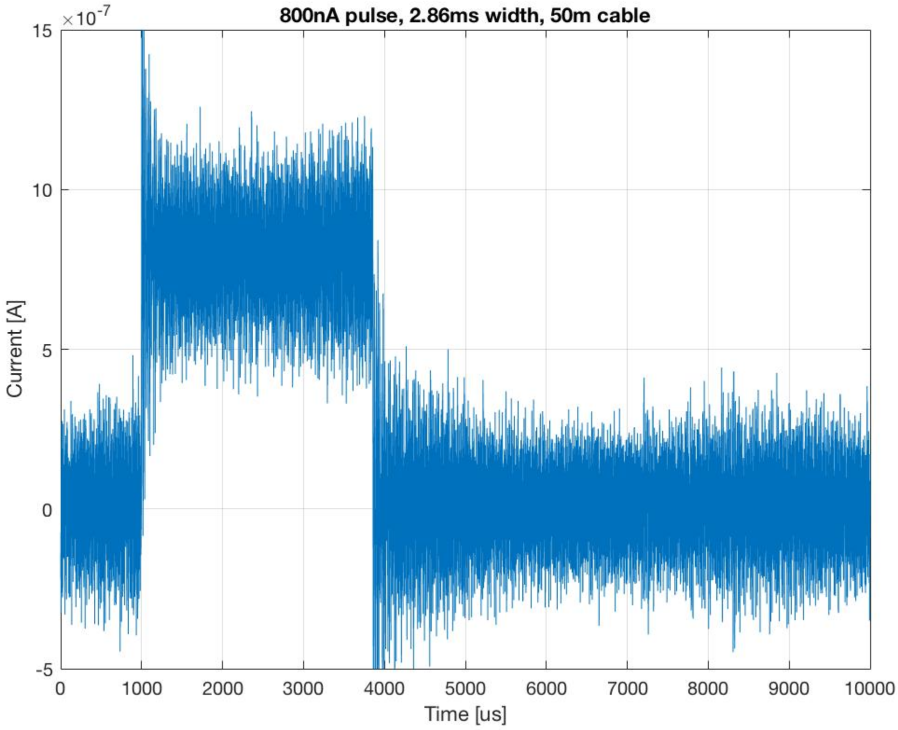

Figure 18: 2.86 ms, 800 nA current pulse acquisition (long cable)

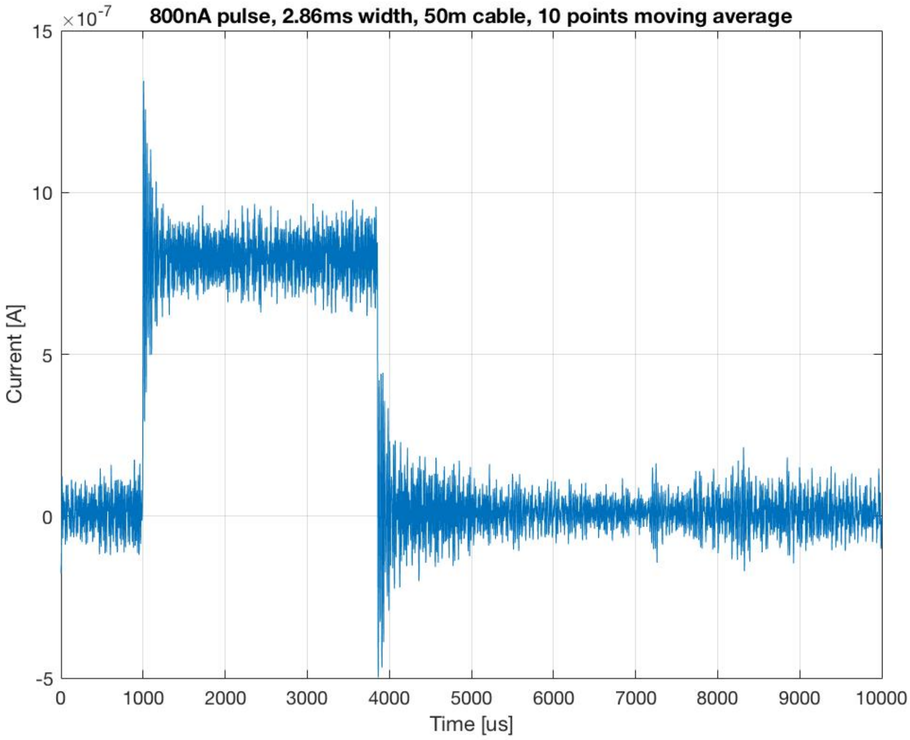

Figure 19: 2.86 ms, 800 nA current pulse acquisition (long cable, 10 points moving average)

- The electronics shall be tested with the ionization chamber itself: The current tests demonstrate the performances that can be reached by the signal acquisition unit, but additional tests shall be performed with a correct cap load.
- Crosstalk measurements need to be performed
- A "long term" measurement shall be performed to identify a possible signal drift, including temperature induced drift.

The table below summarizes the preliminary evaluation results. These are to be confirmed with the next tests, listed above.

icBLM specification	**Evaluation result**
Dynamic range	Fits specifications
Response time	Fits specifications
Maximum input voltage	Evaluation to be performed

Crosstalk	Evaluation to be performed
Resolution	Fits specifications
Noise figure	Fits specifications

Table 3: COTS signal readout unit evaluation results

4.2.2 Custom acquisition crate solution

The alternative unit ESS BI will evaluate as digitizer solution for the icBLM is the solution in use at CERN. Its detailed architecture and specifications are available at this link:

https://indico.cern.ch/event/527597/contributions/2159805/attachments/1338813/2016185/Christos_Zamantzas_.pdf

This signal acquisition unit will be evaluated following the same protocol as the COTS option. Evaluation results will then be compared.

Figure 20: Standalone custom acquisition crate

5. DIGITAL PLATFORM

5.1 The AMC

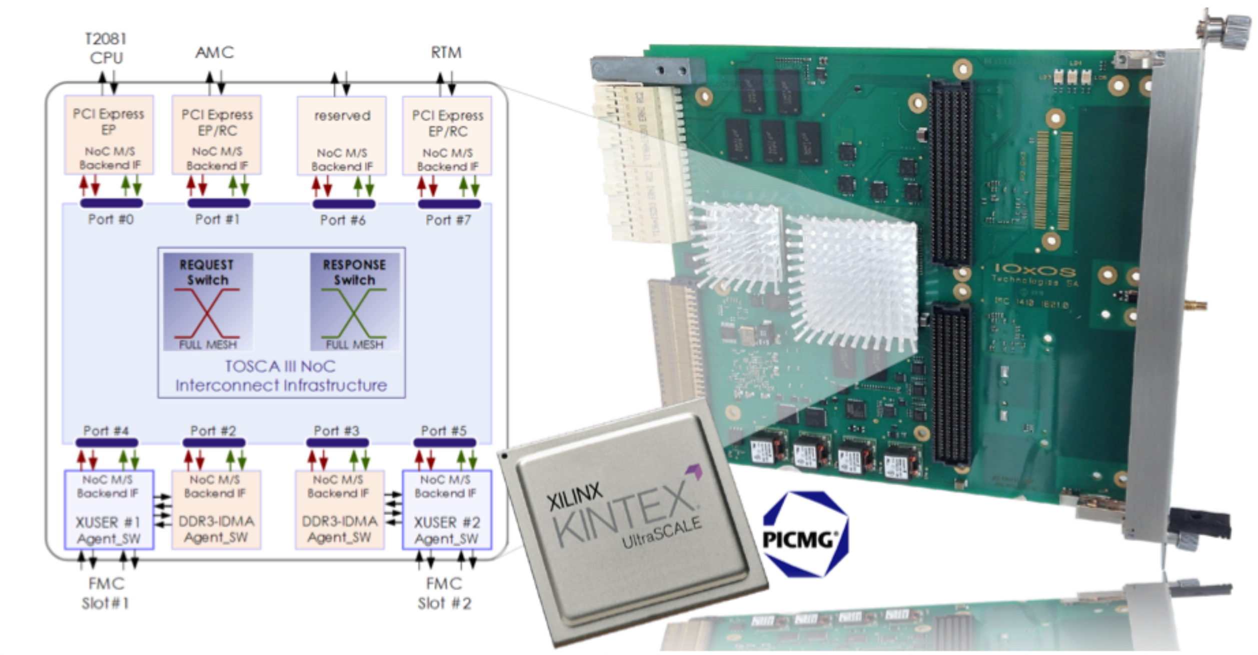

Figure 21: AMC IOxOS IFC1410

The AMC is an IOxOS IFC1410, FMC carrier with Xilinx Kintex Ultrascale FPGA (See producer website for more information: http://www.ioxos.ch/images/pdf/01_datasheet/IFC_1410_DS_A3.pdf).

5.2 The RTM

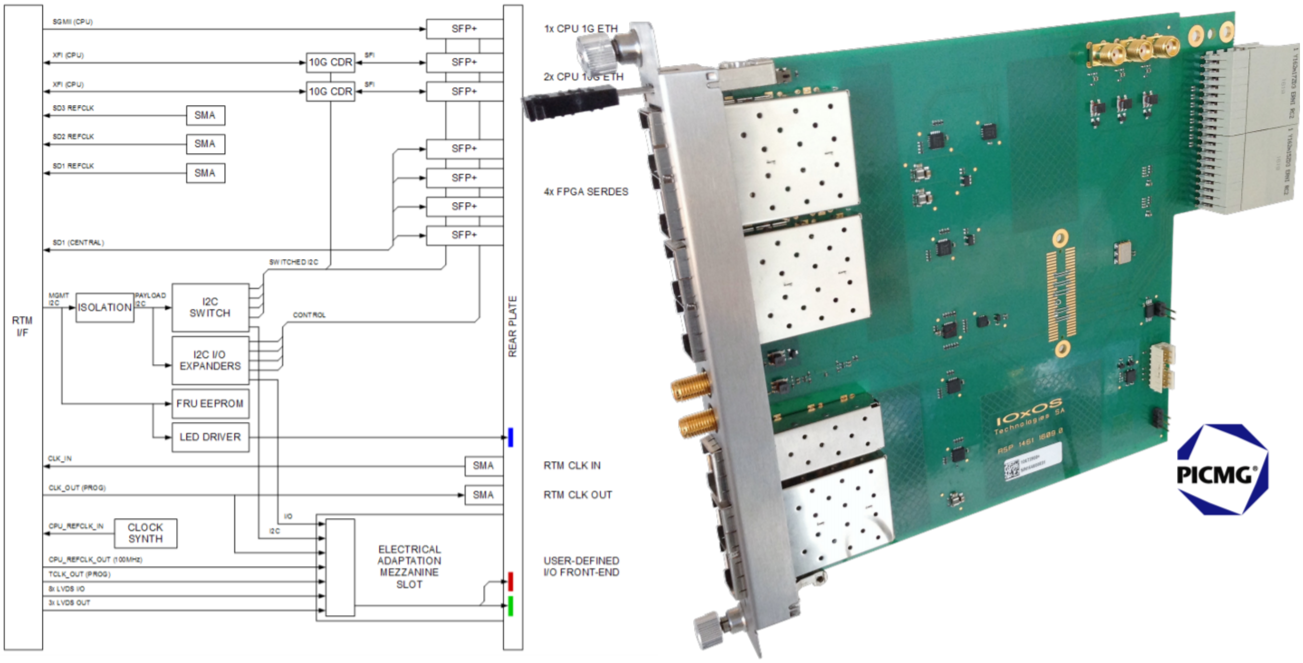

Figure 22: RTM IOxOS IFC1461

The RTM is an IOxOS IFC1461 Communication Extender μRTM, equipped with 7 SFP+ ports (See producer website for more information:

http://www.ioxos.ch/images/pdf/01_datasheet/RSP_1461_DS_A2.pdf).

This is mainly used to interconnect different AMC to share useful information: the only requirement is that the maximum latency is less than 1 μs (this only include all the delay related to the firmware ignoring the latency due to the time of flight on the fiber).

6. SOFTWARE AND EPICS INTEGRATION

ESS standard software framework and development environment, provided by ICS division, shall be used for software development purposes.

ICS division is responsible for delivering all the framework components that are required for icBLM specific application design and development. icBLM system specific application software development is planned to be carried out by the PBI section.

The main EPICS PVs to answer software specifications have been identified and are listed in Table 4: main icBLM EPICS PVs. Assumptions have been made to produce this list:

- It is assumed that the timing system provided timestamps are set for all EPICS records
- DOD (data-on-demand) is available for any EPICS record to provide post-mortem data or data at 'interesting' event
- location of the PVs is not yet specified (IOC, service layer, ..)
- all PVs may be archived (depends on the archiver configuration)
- PVs providing integrated beam loss should have record alarm field set to some threshold in order to signal excess beam loss
- MPS interfacing is not part of this list

Name	Input or output	Scalar or waveform	Number of elements	Update rate	Comment
Beam loss over 1 pulse	output	waveform	3 000	14 Hz	1 us / sample
	output	waveform	3 000	1 Hz	1 us / sample
	output	waveform	3 000	on demand	1 us / sample
	output	waveform	300	14 Hz	10 us / sample
Beam loss over 1 period	output	waveform	72 000	14 Hz	1 us / sample, complete period ~72 ms

Name	Input or output	Scalar or waveform	Number of elements	Update rate	Comment
Background over 1 period	output	waveform	72 000	0.01 Hz	1 us / sample, complete period ~72 ms acquired when there is no beam in the pulse
Uncorrected beam loss data over 1 period	output	waveform	72 000	on demand	1 us / sample, complete period ~72 ms before background is subtracted
Raw beam loss data over 1 period	output	waveform	7 000 000	on demand	at ADC rate (1 MHz) complete period ~72 ms
Maximum peak loss	output	scalar	-	on change	using data from Beam loss over 1 pulse (1 us / sample) persistent over 60 seconds
Peak loss rate over 1 pulse	output	scalar	-	14 Hz	maximum loss detected from data in Beam loss over 1 pulse (1 us / sample)

Name	Input or output	Scalar or waveform	Number of elements	Update rate	Comment
Peak loss rate over 1 pulse	output	scalar	-	1 Hz	maximum loss detected from data in Beam loss over 1 pulse (1 us / sample)
Integrated beam loss over 1 pulse	output	scalar	-	14 Hz	data from Beam loss over 1 pulse waveform
Integrated beam loss over 1 pulse history	output	waveform	100	14 Hz	data from Integrated beam loss over 1 pulse scalar
Integrated beam loss over 1 second	output	scalar	-	1 Hz	data from Beam loss over 1 period waveform
Integrated beam loss over 1 second history	output	waveform	100	1 Hz	data from Integrated beam loss over 1 second scalar
Integrated beam loss over 10 seconds	output	scalar	-	0,1 Hz	data from Beam loss over 1 period waveform
Integrated beam loss over 10 seconds history	output	waveform	100	0,1 Hz	data from Integrated beam loss over 10 seconds scalar
Integrated beam loss over 1 minute	output	scalar	-	0,1 Hz	data from Beam loss over 1 period waveform

Name	Input or output	Scalar or waveform	Number of elements	Update rate	Comment
Integrated beam loss over 1 minute history	output	waveform	100	0,1 Hz	data from Integrated beam loss over 1 minute scalar
Integrated beam loss over 10 minutes	output	scalar	-	0,1 Hz	data from Beam loss over 1 period waveform
Integrated beam loss over 10 minutes history	output	waveform	100	0,1 Hz	data from Integrated beam loss over 10 minutes scalar
High voltage PS control	input	scalar	-	on demand	on, off, standby
High voltage PS status	output	scalar	-	on event	on, off, standby, fault, over voltage, over current, ..
High voltage PS voltage	input	scalar	-	on demand	set voltage
High voltage PS voltage	output	scalar	-	1 Hz	actual voltage
High voltage PS current	output	scalar	-	1 Hz	actual current
High voltage PS temperature	output	scalar	-	1 Hz	temperature readout

Name	Input or output	Scalar or waveform	Number of elements	Update rate	Comment
Instrument enable control	input	scalar	-	on demand	enabled, disabled
Instrument enable status	output	scalar	-	on demand	enabled, disabled
Temperature	output	scalar	-	10 Hz	temperature of the instrument?
Gain	input	scalar	-	on demand	
Filter parameters	input	?	?	on demand	?
Self test	input	scalar	-	on demand	?
Self test status	output	scalar	-	on event	was self test successful?
Mode	input	scalar	-	on demand	normal, calibration
Heartbeat	output	scalar	-	on event	?
Protection Parameters for FPGA algorithm	input	scalars	-	on demand	To be defined during detailed design phase.

Name	Input or output	Scalar or waveform	Number of elements	Update rate	Comment
Activation limits	input	scalars	-	on demand	Nominally 1 W/m (see ACC.SYR-20 Beam Loss Limit), but will be expanded to support dose and activation management

Table 4: main icBLM EPICS PVs

7. CABLING CONCEPT

7.1 Number of cables

In brief, each detector needs:

- One High Voltages cable
- One signal cable

Additional cables form the signal acquisition card to the detectors are foreseen in order to be able to scale up the number of deployed detectors in the future.

7.2 EMC interference

- Static & Dynamic EMC
- Cable picking up noise interference.
- Instruments causing noise/harmonics etc.
- Environment radiation e.g. RF power signals

The overall system cabling concept is depicted on Figure 23.

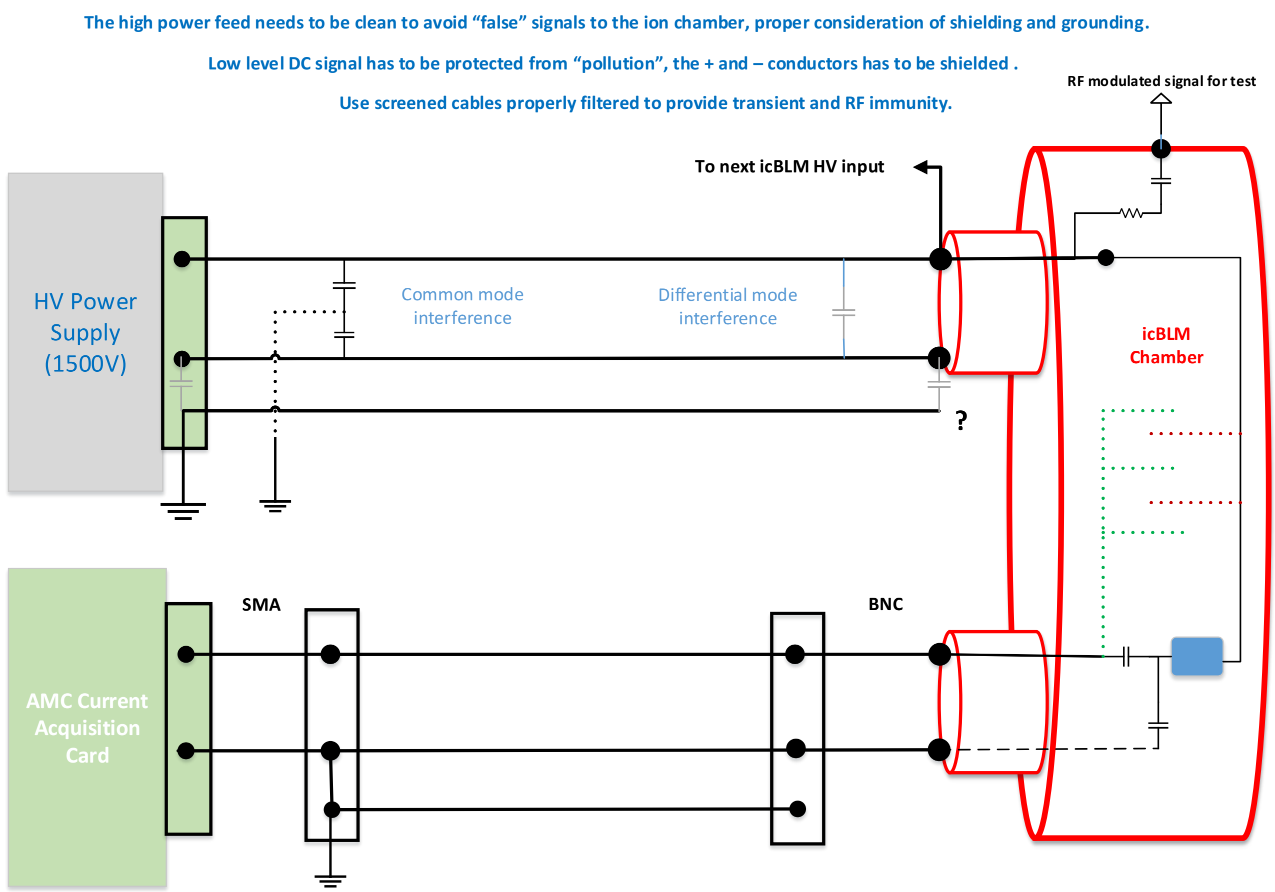

Figure 23: ionization chamber cabling concept

7.3 Cables specifications

7.3.1 High Voltage Cables, SHV connector

SHV Cable that can handle up to 8kV. For example,

1C20RG-58HV (already approved by ESS; HV-Coax, Working voltage > 7kV, RG58 size,

XPE Insulation, Red Jacket)

7.3.2 Signal Cables, LEMO connectors (PP-uTCA), TRIAX-BNC connectors.

Need to use low loss triaxial cables.

For example, cable:

- 1CRG-174HF, (already approved by ESS; 1 conductor RG-174 A/U, 50ohm)

7.4 Rack instruments to consider for EMC cable layout

- Attenuate low harmonics from switching power supply (<1MHz)
- One major source is the voltage developed within the circuit´s ground reference. This is why it is good practice to couple the circuit to ground at the interfaces, which will minimize noise voltage.
- Differential mode current is the current that flows in one direction along one cable conductor and in the reverse direction along another. It is normally equal to the signal or power current, and with shielded cable, is not present the shield. It contributes little to the net radiation because the total loop area formed by the two conductors is small, the two currents tends to cancel each other, depending cable length.
- Common mode current, ICM, Flows equally in the same direction along all conductors in the cable, including the shield if this is present, and may or may not be related to the signal currents. That part of the signal current which does not return via the cable but leaks through stray coupling, does appear as a common mode component; this aspect is related to the longitudinal conversion loss of the cable.

8. SAFETY

8.1 Hazards identification

- **Radioactive source:** Although not a permanent part of the system, calibration with encapsulated radiation sources is envisioned. These sources will be handled and the systems and techniques that utilize them will meet all applicable ESS, EU, and Swedish safety requirements.
- **High voltage bias integrated in the system:** A bias supply of up to 3 kV will be part of the system. This will be addressed during the design phase according to ESS internal regulations and the relevant laws of Sweden. Even for the low currents anticipated, finger-safe SHV connectors will be used, and high voltage cables will be red and run in dedicated tray partitions.

9. QUALITY AND AVAILABILITY

Assets management tools are in place at ESS to ensure documents tracking and a proper planning of the deployment & installation phase. This includes a barcode system, standards for measurement files formats.

Data integrity, portability and longevity are addressed as follows:

1. The repository that holds all of the data supports programmatic access such that entry, extraction and migration (to other repositories in the future) can be automated. This increases the efficiency of these operations and reduces the likelihood of human error.
2. All quantitative data will be in a portable, machine-readable format based on HDF5 and will include metadata that describes to the context in which the data was taken.

During the detailed design phase, a detailed acceptance test plan at system level will be produced. The table below summarizes the high level tests that shall be performed on the system FRUs:

	Detector	**Data acquisition units**	**HV unit**	**Complete acquisition chain**
Functional test	x	x	x	x
Barcode check	x	x	x	
Source test	x			
Radiation source test (before startup)	x	x	x	
Signal offset		x	x	x
Beam Inhibit tests		x	x	x
Thresholds and channels assignment software checks		x	x	x
HV modulation tests		x	x	x

The system will have to be reliable enough to support the availability goals of ESS.

The icBLM preliminary design has been built around the following main points to ensure ESS reliability requirements are met:

- The number of detector channels allows redundancy
- HV supply topology supports redundancy
- MTCA supports redundant PS, MCH, hotswap
- Low-latency communication links allow rapid reconfiguration in case of failures or new operational needs.

In addition, the verification program highlighted above reduces the possibility of latent, undetected errors in the system. A small subset of these tests will be incorporated into the deployed system to provide a built-in self test capability. System status will also be available to the Beam Interlock System and to the higher layers of the control system.

10. CONCLUSION AND OUTLOOK

To cover all system specifications in the design, further steps have been identified:

10.1 FRU tests

- Tests are planned to evaluate the performances of the high voltage supply versus ESS specifications.
- Tests are planned to evaluate the performances of the custom acquisition crate versus ESS specifications.
- Further tests including all system's constituting FRUs are planned

10.2 System design choices

A decision on the system architecture will be done based on evaluation results between the custom acquisition crate and the COTS solution.

10.3 Software and Firmware

- A Firmware meeting all icBLM specific functionalities as described in the specifications document should be designed
- A software meeting all icBLM specific functionalities as described in the specifications document should be designed