Description:	This document describes the LO RTM conceptual design proposed by the Polish Electronic Group (PEG) for the 704 MHz LLRF system at ESS.
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Introduction

The ESS LLRF control system detects the amplitudes and phases of the input RF signals by down-converting them to an intermediate frequency (IF) and digitizing. The architecture necessitates synthesis of a low phase noise heterodyne/local oscillator (LO) and clock signals.

A MTCA.4-complaiant chassis was selected by the ESS ERIC as the platform housing the main part of the LLRF control system electronics. The remote diagnostic functionality is considered one of the main benefits of the platform. Polish Electronic Group is responsible for the design, manufacturing, testing, and delivery of the LO and clock generation devices for the 704.42 MHz LLRF systems as a part of Polish In-Kind Contribution. The device will be a Rear Transition Module (RTM), controlled via digital interface over the Zone3 connector by an AMC module. One RTM will feed one system located in the same crate and three other neighboring systems.

A list of performance and functional requirements is given. Three LO frequency synthesis schemes are compared focusing on the phase noise performance in LLRF field detection application. For the clock signal two frequency division schemes are discussed. The measured characteristics of components used in the selected schemes are analyzed. The conceptual design of diagnostic, monitoring, communication, and power conditioning circuits is presented.

Requirements

The performance and functional requirements set before the LO RTM are presented in Table 1.

Table 1. LO and clock requirements.

Reference frequency	704.42 MHz							
Clock frequency	117.403(3) MHz							
Clock Signal Phase noise	Offset	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
	Phase noise (dBc/Hz)	-106	-120	-134	-145	-151	-151	-153
Number of Clock Outputs	4							
Clock Output Power (each)	+15 dBm							
Clock signal shape	Sine-wave							
Maximum spurious level for clock signal	-60 dBc							
Intermediate Frequency	25.158 MHz 32.019 MHz							
LO Signal Phase noise	Offset	10 Hz	100 Hz	1 kHz	10 kHz	100 kHz	1 MHz	10 MHz
	Phase noise (dBc/Hz)	-90	-110	-125	-140	-149	-152	-154
Number of LO Outputs	4							
LO Output Power (each)	+15 dBm							
Maximum spurious level for LO signal	-50 dBc (non-harmonic) -60 dBc (harmonic)							

Frequency Synthesis Schemes

The clock signal can be generated by frequency division of the reference signal (divide by 6). The LO to reference frequency ratio is $\frac{29}{28}$ or $\frac{23}{22}$. The output frequency cannot be generated by frequency division of the input signal and must be synthesized.

Frequency synthesizers may be classified into three types:

- Direct Analog
- Direct Digital
- Indirect Digital

The first approach uses frequency dividers, mixers, and band-pass filters. It closely follows the phase noise of the reference signal, with additional noise induced by the frequency divider. Far from carrier, the noise can be improved by using a narrow band-pass filter. Such filters increase the cost of the device and are sensitive to mechanical vibrations and temperature.

A Direct Digital Synthesizer (DDS) uses a numerically controlled oscillator feeding a DAC, both being synchronized by a reference clock. State of the art integrated DDS ICs accept a high frequency reference clock (3 GHz and above) and can generated output frequencies up to 1.5 GHz. The intermediate to reference frequency ratio is 1/28 or 1/22 and the clock to reference frequency ratio is 1/6, therefore systemic frequency error will be introduced by using a binary frequency tuning word. Additionally high-speed DDSs have a significant residual phase-noise floor at the considered LO frequency (-153 dBc/Hz @1 MHz and above offset), which makes them unsuitable for the application.

An Indirect Digital Synthesizer utilizes a PLL with an integer or fractional frequency divider. For offset frequencies within the loop bandwidth the phase noise is determined by the reference signal's characteristics distorted by the phase detector's noise. Outside the loop bandwidth the noise is dominated by the VCO used and optional output frequency dividers.

The DDS solution was rejected due to reasons explained above, leaving Direct Analog and Indirect Digital schemes for consideration. The phase-noise performance of both schemes was evaluated against each other.

LO Generation

The mechanical vibrations present in the crate may induce spurious in the spectra of the VCO output signal. The physical dimension constraints imposed by the MTCA standard limit the selection of VCOs. Integrated silicon VCOs are preferred due to their higher immunity to such vibrations and small size.

In the next sections details of the PLL-based design are discussed. Later the simulations and measurements of the design are presented.

PLL Configurations

For the performance evaluation LMX2592 chip made by Texas Instruments was selected. The IC contains both a PLL and a VCO. The integrated wideband VCO offers one of the best performance on the market (based on normalized noise floor). The dividers for the reference signal and the VCO support fractional division ratios.

The manufacturer provides two equations for optimization of the phase noise of the PLL output signal.

$$PLL_{flat} = PLL_{FOM} + 20 * log\left(\frac{F_{VCO}}{F_{pd}}\right) + 10 * \log(\frac{F_{pd}}{1\ Hz})$$

$$PLL_{flicker}(f_{offset}) = PLL_{flicker\ norm} + 20 * \log\left(\frac{F_{VCO}}{1\ GHz}\right) - 10 * \log(\frac{f_{offset}}{10\ kHz})$$

The close-to-carrier noise is dominated by frequency-converted reference noise and additive flicker (1/f) noise. The latter can be optimized by increasing the VCO frequency. Far from carrier the noise floor is dependent on the phase detector and VCO frequencies. Higher phase detector frequency should be selected to decrease the noise.

The selection of the VCO frequency is limited by the list of settings of the output frequency divider. To optimize the phase noise the maximum VCO frequency was selected (5808 MHz). Two configurations of the PLL were selected, simulated, and later measured (see Figures 1 and 2). Due to constraints of the VCO predivider using the higher phase detector frequency (176 MHz) is only possible with fractional division of the VCO frequency. The selected fraction (1/2) introduces new spurs in the phase noise spectrum at 88 MHz offset and above, hence it was considered acceptable.

The evaluation board is equipped with an 3rd order analog loop filter designed by the manufacturer. Increasing the charge pump current changes the loop gain and the effective loop characteristics.

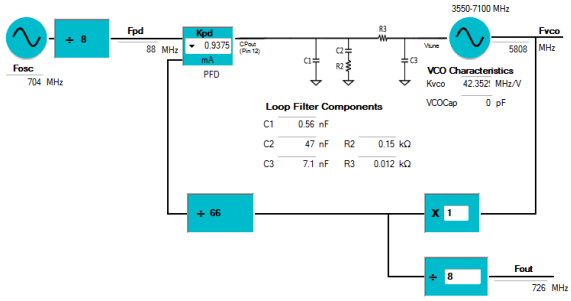

Figure 1. PLL configuration using lower phase detector frequency.

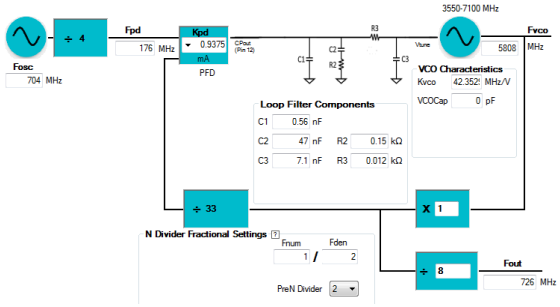

Figure 2. PLL configuration using higher phase detector frequency.

PLL Simulations

Texas Instruments provides a software package, named PLLatinum Sim, which can simulate the output phase noise of the device. The simulations were performed for the same reference signal as used for measurements (described in the next section) and for various charge pump currents. The current changes the effective loop filter bandwidth. The integrated jitter for various configurations is provided in Table 2 (current values selected for minimal total jitter) and phase noise spectra are compared in Figures 3 and 4.

According to simulations the proposed solution adds significant 1/f noise above the 20 Hz offset for both lower and higher phase detector frequencies. Varying the charge pump current affects the phase noise bump's position and height. Above 300 kHz offset (above the loop's bandwidth) the phase noise at the output is better than at the input.

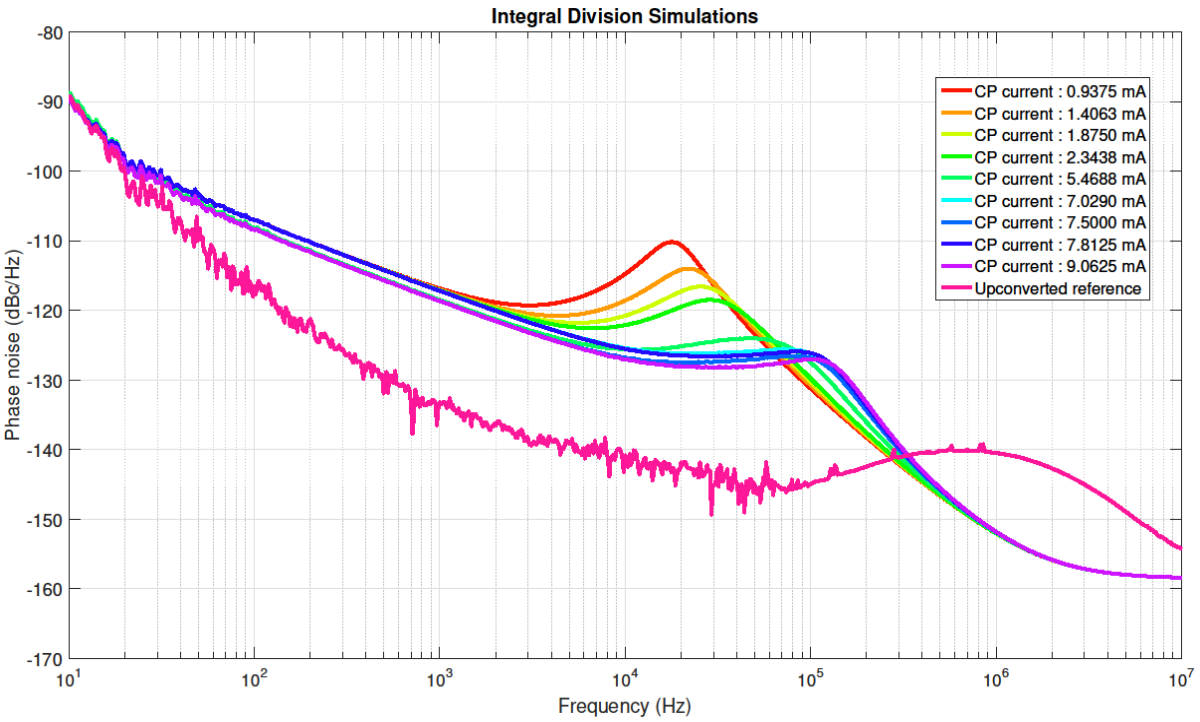

Figure 3. Simulated phase noise spectra of the PLL operating with lower phase detector frequency (88 MHz) for various charge pump currents. Integral VCO divider is used.

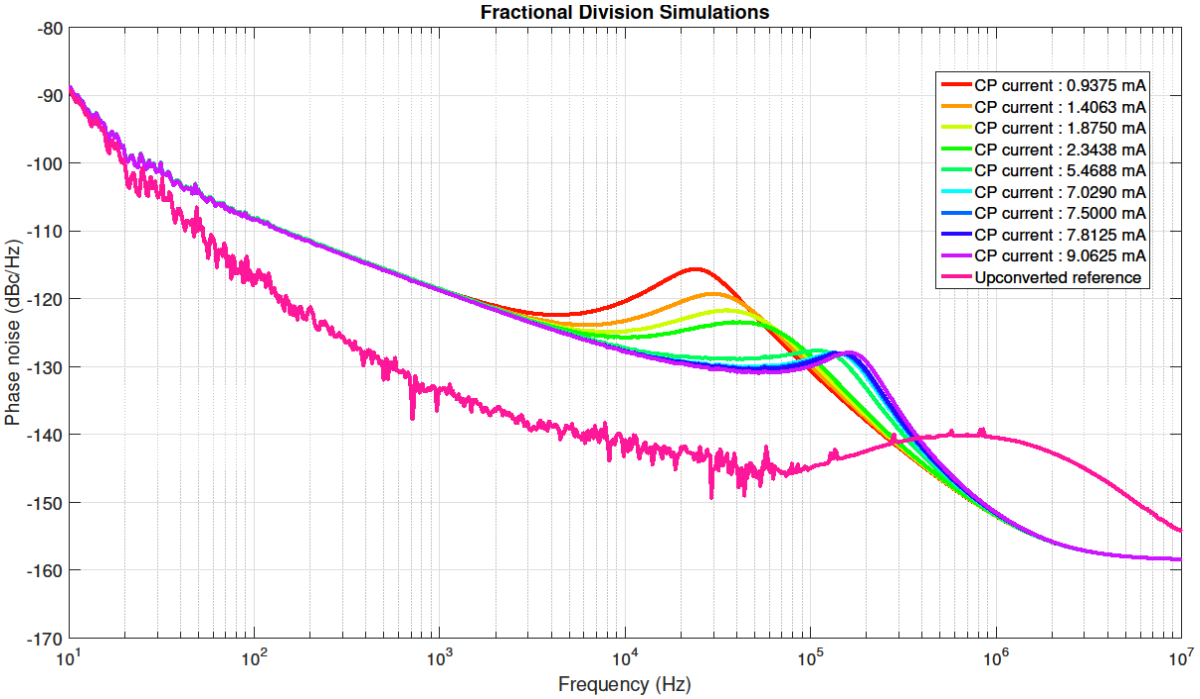

Figure 4. Simulated phase noise spectra of the PLL operating with higher phase detector frequency (176 MHz) for various charge pump currents. Fractional VCO divider is used.

Table 2. Simulated absolute jitter of two PLL configurations in each frequency decade. The charge pump current was select to minimize the total jitter (in the 10 Hz – 10 MHz band).

	Start offset	10	100	1 k	10 k	100 k	1 M	10
PLL Configuration	End offset	100	1 k	10 k	100 k	1 M	10 M	10 M
	Current							
Integer Division	9.0625 mA	25.7	17.5	18.4	38.5	40.1	12.8	67.5
Fractional Division	7.029 mA	27.7	17.4	17.8	31.3	42.4	12.8	65.8

PLL Measurement Setup

The block diagram of the setup used for the PLL's performance evaluation is shown in Figure 5. Holzworth HSX9004A is a low phase noise reference source, generating a 704 MHz reference signal for the PLL. The reference signal's power was set to +10 dBm and the PLL's output frequency was 726 MHz. Agilent E5052B is a signal source analyzer (SSA) measuring the PLL's output signal. Software written in Python and running on a PC acquired the data from the instrumentation. The PLL chip was configured using a hardware adaptor and software provided by the manufacturer with the evaluation module.

The phase noise of the reference signal was measured and used for simulations and as a comparison for the measurements' results.

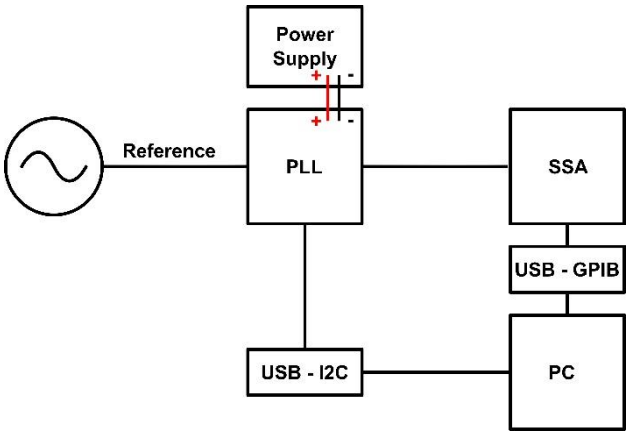

Figure 5. Block diagram of the measurement setup.

PLL Measurements

The proposed and simulated configurations were measured using the aforementioned setup. The integrated jitter for various configurations in summarized in Table 3 (current values selected for minimal total jitter) and phase noise spectra are presented in Figures 6 and 7.

The measured performance is similar to the results of simulations. The 1/f noise is few dB higher while the phase noise floor is few dB lower than simulated.

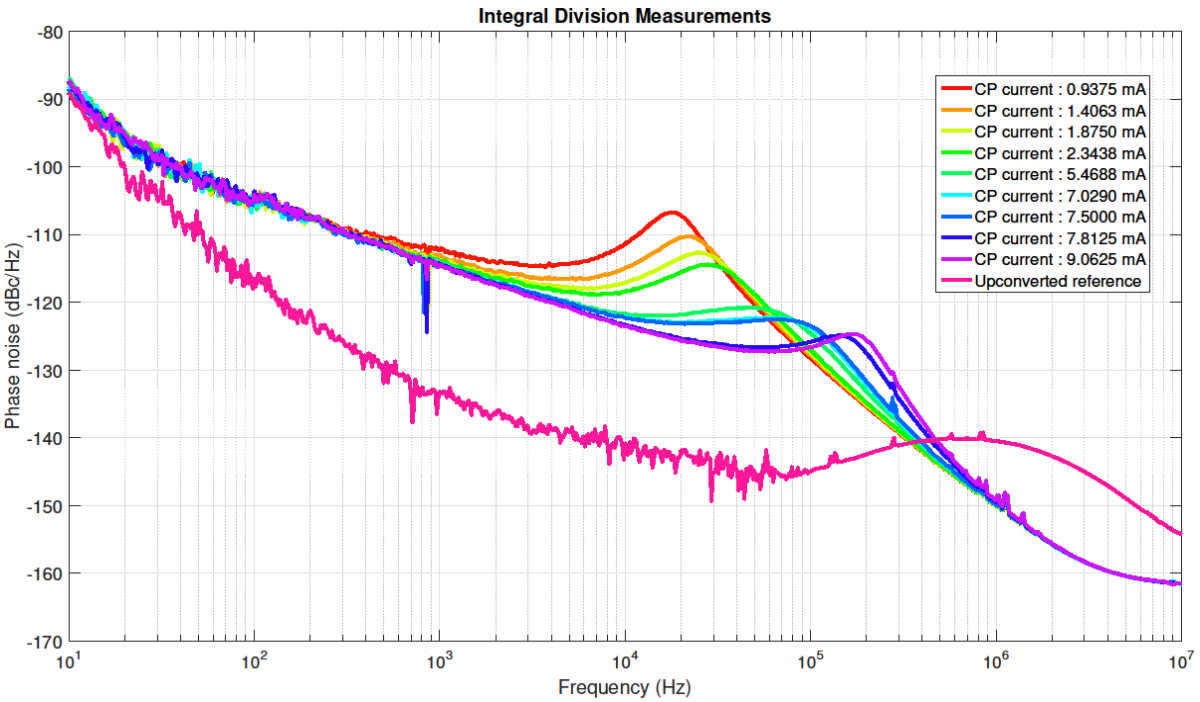

Figure 6. Measured phase noise spectra of the PLL using lower phase detector frequency for various charge pump currents. Integral VCO divider is used.

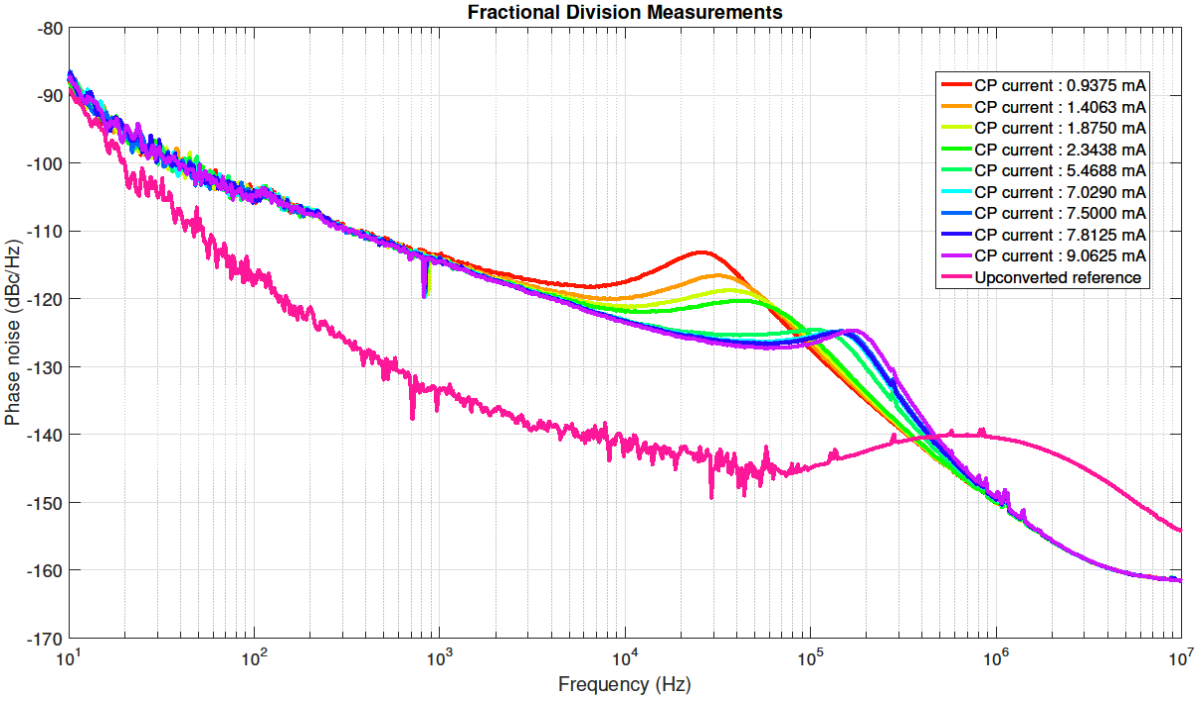

Figure 7. Measured phase noise spectra of the PLL operating with higher phase detector frequency (176 MHz) for various charge pump currents. Fractional VCO divider is used.

Table 3. Measured absolute jitter of two PLL configurations in each frequency decade. The charge pump current was select to minimize the total jitter (in the 10 Hz – 10 MHz band).

Jitter (fs)	Start offset	10	100	1 k	10 k	100 k	1 M	10
PLL Configuration	End offset	100	1 k	10 k	100 k	1 M	10 M	10 M
	Current							
Integer Division	7.8125 mA	34.8	28.0	29.6	46.5	63.2	11.6	95.7
Fractional Division	7.8125 mA	35.8	28.0	29.7	46.4	62.3	11.6	95.6

Direct Analog Scheme Preliminary Evaluation

Figure 8 shows the block diagram of the solution utilizing the direct analog scheme and its measurement setup. The components used are listed in Table 4. Due to limited availability of IF band-pass filters at the time of preliminary evaluation the intermediate frequency was set to 44.02625 MHz.

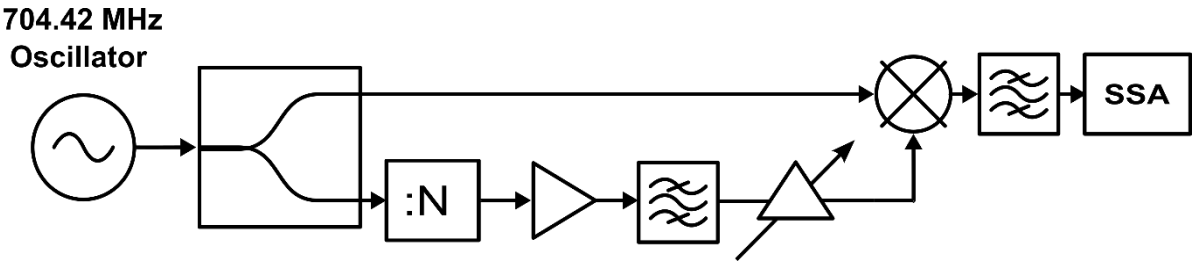

Figure 8. Block diagram of the solution utilizing the direct analog scheme and its measurement setup.

Table 4. List of components used in the preliminary direct analog scheme test setup.

Component name	**Manufacturer and model**
Oscillator	Holzworth HSX9004A
Frequency divider	Analog Devices AD9515 (Evaluation board : AD9515/PCB)
IF Signal Amplifier	TriQuint AH202F (Evaluation board : AH202-PCB900)
IF Band-pass filter	MiniCircuits SIF-50+
LO Band-pass filter	K&L D5BT-750/1500-5-N/N-GRI
Mixer	MiniCircuits HJK-272H (Evaluation board : TB-12)
Signal Spectrum Analyzer	Agilent E5052B

The phase noise of the mixer output signal is a sum of the reference signal noise and the additive noise of the frequency divider signal (increased by any amplifier in the chain). The measured phase noise curve of the direct analog scheme follows closely the curve of the reference signal. This scheme adds no visible 1/f noise. The increase of phase noise between 30 kHz and 2 MHz might be caused by poor grounding, power supply noise, or declining correlation between signals. Above 300 kHz the PLL-based solution offers better performance because it's no longer following the reference signal, which has a bump centered at 100 kHz.

LO Synthesis Scheme Selection

As can be seen in Figure 9, the direct analog scheme offers better phase noise performance in the 10 Hz – 10 MHz band even when it's feed with a suboptimal reference signal. Therefore it was selected

as the LO frequency synthesis scheme. The following sections focus on optimization of the mixer-based design and selection of the IF dividers.

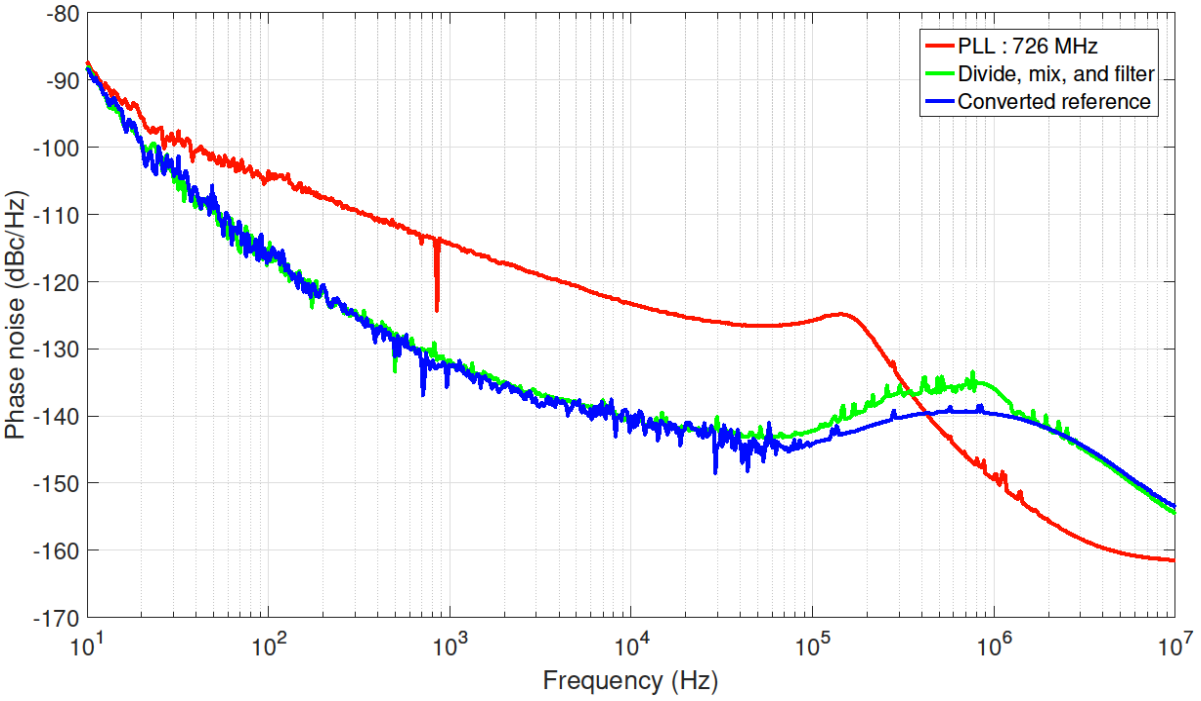

Figure 9. Measured phase spectrum of direct analog LO frequency synthesis scheme against spectrum of the scheme using PLL and the reference.

Mixer Selection

A real upconverting mixer has at its output following spectral components:

- desired sideband,
- undesired sideband,
- carrier ($f_{carrier}$),
- higher order mixing products, including $f_{carrier} \pm N \times f_{intermediate}$.

All the undesired components are filtered out using a band-pass filter. The pass-band width is limited by IF signal bandwidth on one side and the closest undesired spectral components (carrier and $f_{carrier} \pm 2 \times f_{intermediate}$) on the other. To lessen the requirements on the filter the mixer should have isolation (opposite of transmission of signal between LO and RF ports) as high as possible.

Near the given carrier frequency (704.42 MHz) the best isolation is offered by two models from MiniCircuits. ADE-R5LH+ (55.53 dB @ 680.1 MHz; 69.22 dB @ 740.1 MHz) and ADEX-R10LH+ (55.81 dB @ 700.1 MHz; 77.09 dB @ 760 MHz) have nominal LO power of +10 dBm. ADE-R5LH+ was selected for the detailed performance evaluation, due to expected higher isolation at the reference frequency.

It should be noted that the isolation is measured for down-conversion mode of operation (RF and LO ports as inputs, IF port as output) and the impedance seen at the IF port, when it is used as an input, influences this factor.

Typically, in the frequency synthesis, the mixer works in the saturated mode, with both inputs controlling the switching element. The selected mixer is designed for low nominal LO power level (+10 dBm), which also implies low output power level. Therefore the desired sideband must be amplified (after filtering). To avoid degradation due to noise added by the LO signal amplifier, the sideband's power should be kept around 0 dBm, and a low noise amplifier should be selected. In the proposed circuit the saturated mode of operation equalizes any differences in the gain of the IF signal conditioning path.

Mixer's Power Spectrum Test Setup

The power spectra of the mixer were measured using a test setup depicted in Figure 10. Table 5 provides a list of components used in the setup. The IF band-pass filter has high rejection for 2nd and 3rd harmonics (> 50 and >70 dB, respectively).

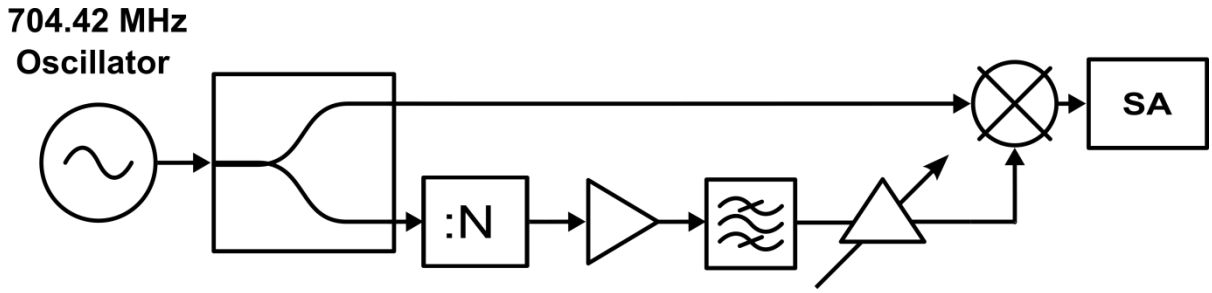

Figure 10. Schematic block diagram of the setup used for power spectrum measurements.

Table 5. List of components used in the mixer power spectrum test setup.

Component name	Manufacturer and model
Oscillator	Agilent E8257D
Frequency divider	Analog Devices AD9515 (Evaluation board : AD9515/PCB)
IF Signal Amplifier	TriQuint AH202-F (Evaluation board : AH202-PCB900)
Band-pass filter	MiniCircuits SXBP-29+ (Evaluation board : TB-368)
Programmable attenuator	Hittite/Analog Devices HMC472ALP4E (Evaluation board : 106977-4)
Mixer	MiniCircuits ADE-R5LH+ (Evaluation board : TB-03)
Spectrum Analyzer	Agilent N9030A PXA

Mixer's Power Spectrum

Figures 11 and 12 present the spectral components power levels as functions of the IF power level for two intermediate frequencies (27.09 MHz and 32.02 MHz). The lower frequency is different from 25.158 MHz given in requirements (Table 1) because the measurements were done before the IFs were selected.

The desired sideband level changes very little for IF power level higher than +10 dBm, equalizing the changes in losses of the filter and gain of the IF signal amplifier. The carrier level is almost independent of the IF power level, making strong output signal even more preferable. The carrier is weaker by roughly 37 dB than the desired sideband.

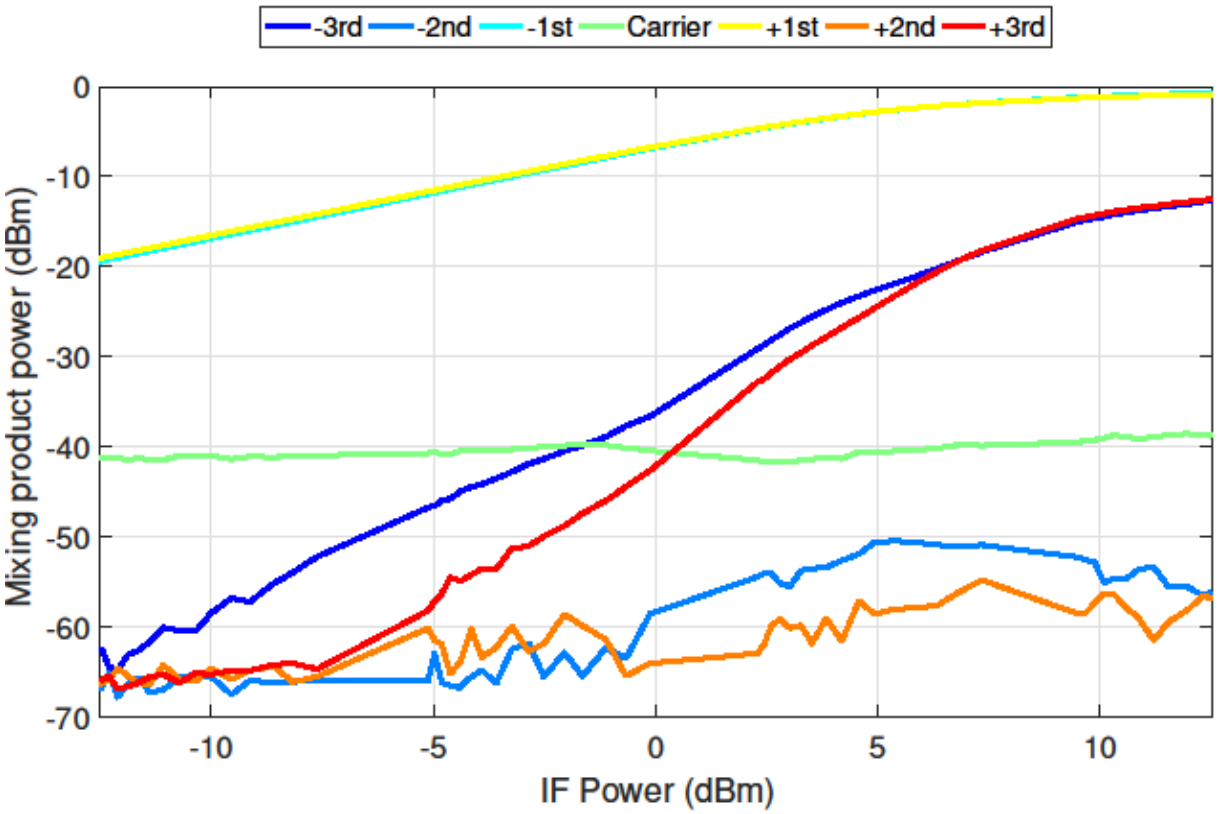

Figure 11. Spectral components at the mixer's output. LO Power = +8.1 dBm, IF = 27.09 MHz.

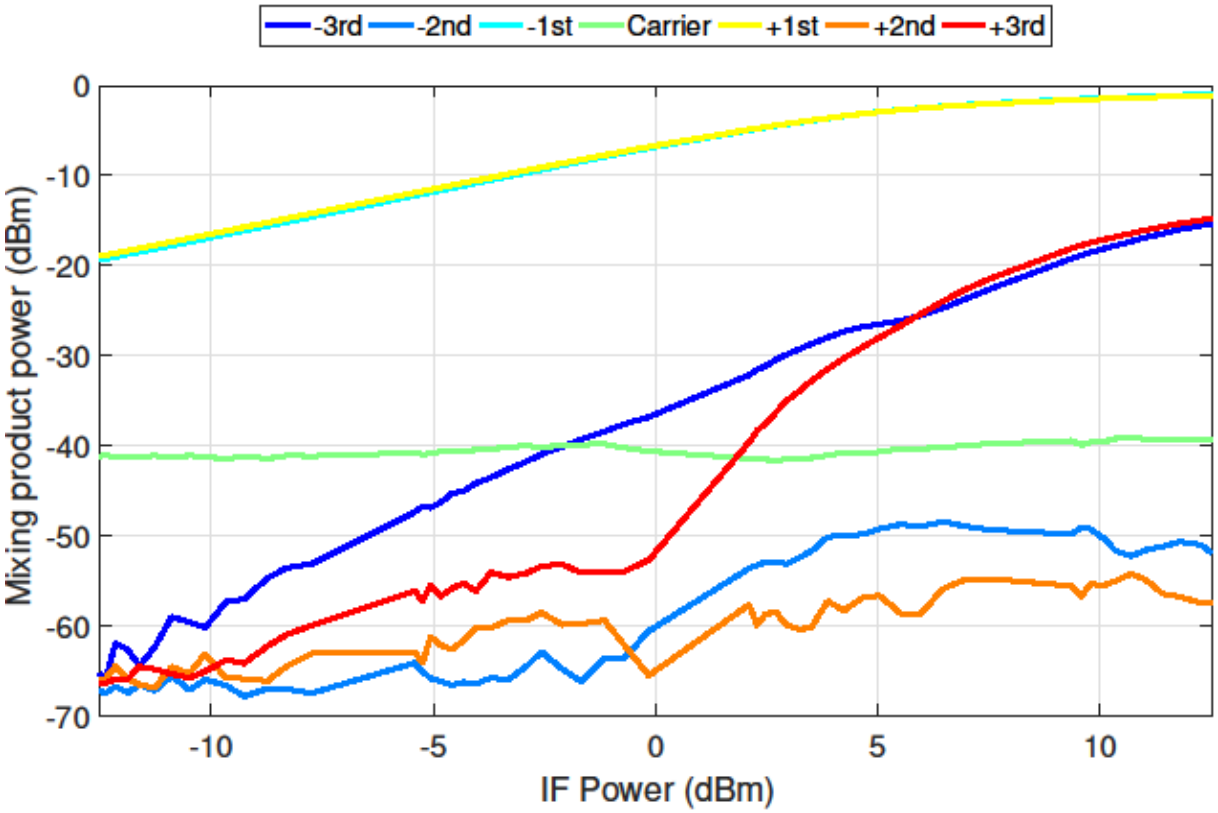

Figure 12. Spectral components at the mixer's output. LO Power = +8.1 dBm, IF = 32.02 MHz.

The third harmonic ($f_{LO} \pm 3 \times f_{intermediate}$) increases rapidly with the IF power level. For +12 dBm drive it's only 13 dB weaker than the desired sideband.

All the unwanted spectral components should be suppressed in order to achieve 60 dB SFDR. Filter parameters derived from the measurements' results and the aforementioned assumption are presented in Table 6.

Table 6. Proposed filter characteristics.

Spectral component	**Suppression**
Desired sideband	S_0
Undesired sideband	S_0 + 60 dB
Carrier	S_0 + 23 dB
2nd harmonic ($f_{LO} \pm 2 \times f_{intermediate}$)	S_0 + 10 dB
3rd harmonic ($f_{LO} \pm 3 \times f_{intermediate}$)	S_0 + 47 dB

The specification was send to various manufacturers for quotation. The offer from T-Ceram was selected based on suppression of the undesired spectral components, price, and lead time. Figure 13 provides measurements of scattering parameters of a sample filter.

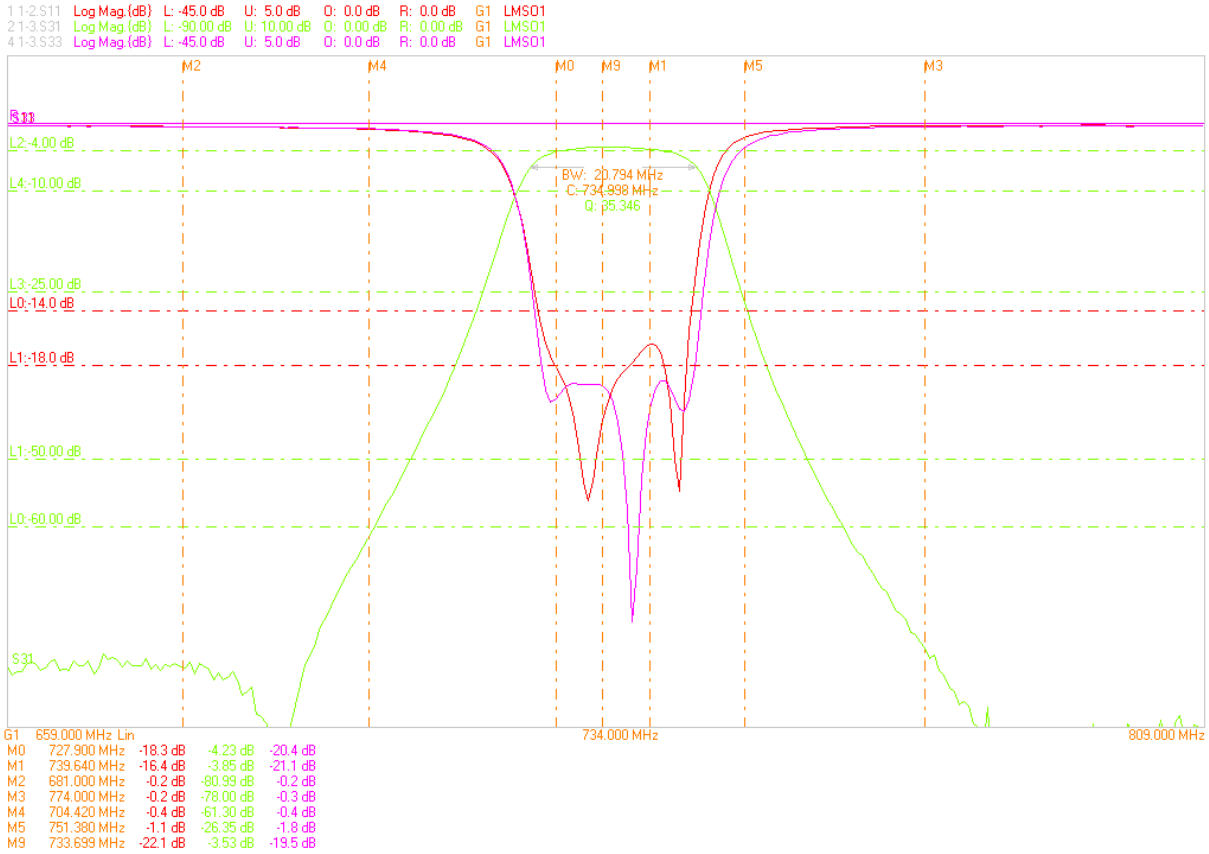

Figure 13. Plot of measured scattering parameters of a sample filter (type TDF-6-0734-16-P1 1).

LO and IF Phase Noise Measurement Setup

The LO signal's phase noise was measured using a test setup shown in Figure 14. The frequency synthesizers available at PEG's laboratories had insufficient phase noise performance above 50 kHz offset, therefore a custom PLL-based synthesizer was designed. Agilent E8257D generates a 704.42 MHz reference signal for the PLL. The phase noise of the reference signal was measured (see Figure

15). Total jitter in the 10 Hz – 1 MHz band equals 14.15 fs (with spur omission). The full list of components is given in Table 7. If needed frequency divider's differential output signals were converted to single-ended using the ADT2-1T-1P transformer.

Table 7. List of components used in the if signal conditioning circuit test setup.

Component name	Manufacturer and model
Oscillator	Agilent E8257D
Frequency divider	Analog Devices AD9515 (Evaluation board : AD9515/PCB) Analog Devices AD9508 (Evaluation board : AD9508/PCBZ)
Band-pass filter	K&L D5BT-750/1500-5-N/N-GRI
Mixer	MiniCircuits ADE-R5LH+ (Evaluation board : TB-03)
Signal Source Analyzer	Agilent E5052B

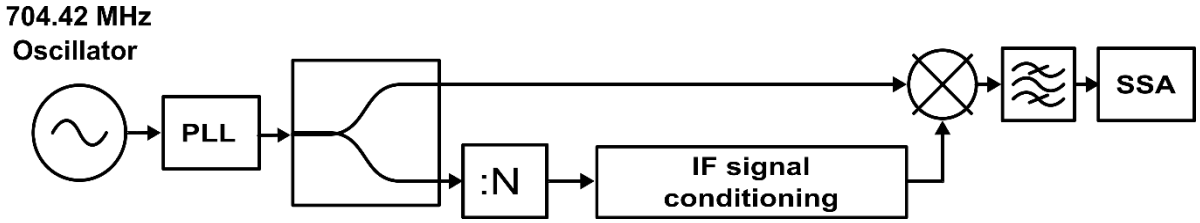

Figure 14. Schematic block diagram of the setup used for comparison of the IF divider and IF signal conditioning circuit on the LO signal's phase noise.

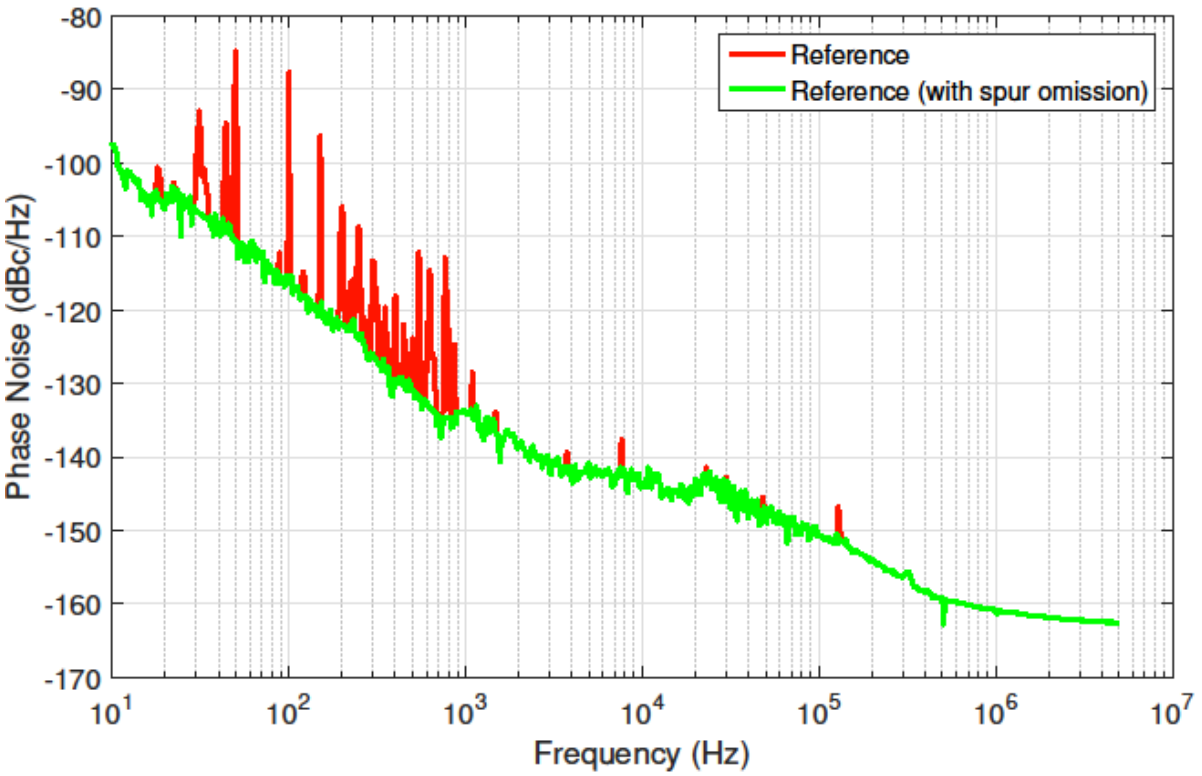

Figure 15. Measured phase noise spectrum (with and without spur omission) of the designed PLL-based reference synthesizer.

Selection of IF Signal Frequency Divider

The frequency divider for this scheme must divide the input frequency by a high programmable ratio (28 or 22). Many frequency divider ICs are available on the market, but only a very limited subset of them can be used for this design. Most of them belong to the AD95XX family made by Analog Devices,

with few chips from other series and manufacturers. The AD95XX family supports multiple signaling standards, including CMOS, HSTL, LVPECL, and LVDS. Products meeting the aforementioned functionality criteria are provided in Table 8. It was assumed that the two types frequency division logic (1-1024 and 1-32) and outputs buffer circuits are common for all chips in the family. The performance of different standards was compared using two devices (AD9508 and AD9515).

Table 8. Comparison of chips from the AD95XX family suitable for intermediate frequency synthesis.

Model	Max input frequency	Output standards	Division ratio
AD9508	1650 MHz	CMOS, HSTL, LVDS	1 - 1024
AD9510	1600 MHz	CMOS, LVDS, LVPECL	1 - 32
AD9511	1600 MHz	CMOS, LVDS, LVPECL	1 - 32
AD9512	1600 MHz	CMOS, LVDS, LVPECL	1 - 32
AD9513	1600 MHz	CMOS, LVDS	1 - 32
AD9514	1600 MHz	CMOS, LVDS, LVPECL	1 - 32
AD9515	1600 MHz	CMOS, LVDS, LVPECL	1 - 32
AD9516	1600 MHz	CMOS, LVDS, LVPECL	CMOS/LVDS : 1-1024 LVPECL : 1 - 32
AD9517	1600 MHz	CMOS, LVDS, LVPECL	CMOS/LVDS : 1-1024 LVPECL : 1 - 32
AD9518	1600 MHz	LVPECL	1 - 32
AD9520	1600 MHz	LVPECL	1 - 32
AD9522	1600 MHz	LVDS	1 - 32

The phase noise spectra of the dividers' output signal in divide-by-22 and divide-by--28 configurations are compared in figures 16 and 17 (only the best plots for each divider are presented). To simplify the analysis the phase noise was integrated (see Tables 9 and 10) per frequency offset decade (up to 5 MHz, limited by Agilent E5052B's offset bandwidth in the given input frequency range).

When LVDS standard was used a significant bump was visible in the spectra at few hundred kHz. The bump is present for differential measurements at output of both dividers and for single-ended measurements of the AD9515. It's present for different division ratios (measurements not included in the report) and different input frequencies. This bump significantly distorts the signal and LVDS was excluded from further considerations.

In the divide-by-22 configuration the AD9515 frequency divider using LVPECL 790 mV standard offers the lowest phase noise up to roughly 60 kHz offset. In the 10 Hz – 5 Mhz band the lowest integrated jitter was measured at the AD9508's outputs using differential CMOS and HSTL (8 mA) standards.

In the divide-by-28 configuration the AD9508 frequency divider using differential CMOS and HSTL (8 mA) standards offers similar performance to the AD9515 frequency divider using LVPEC 790 mV standard up to 10 kHz. The best performance is offered by the AD9508 frequency divider using HSTL (8mA) and differential CMOS standards.

The AD9508 frequency divider was selected as the IF divider for the LO RTM project.

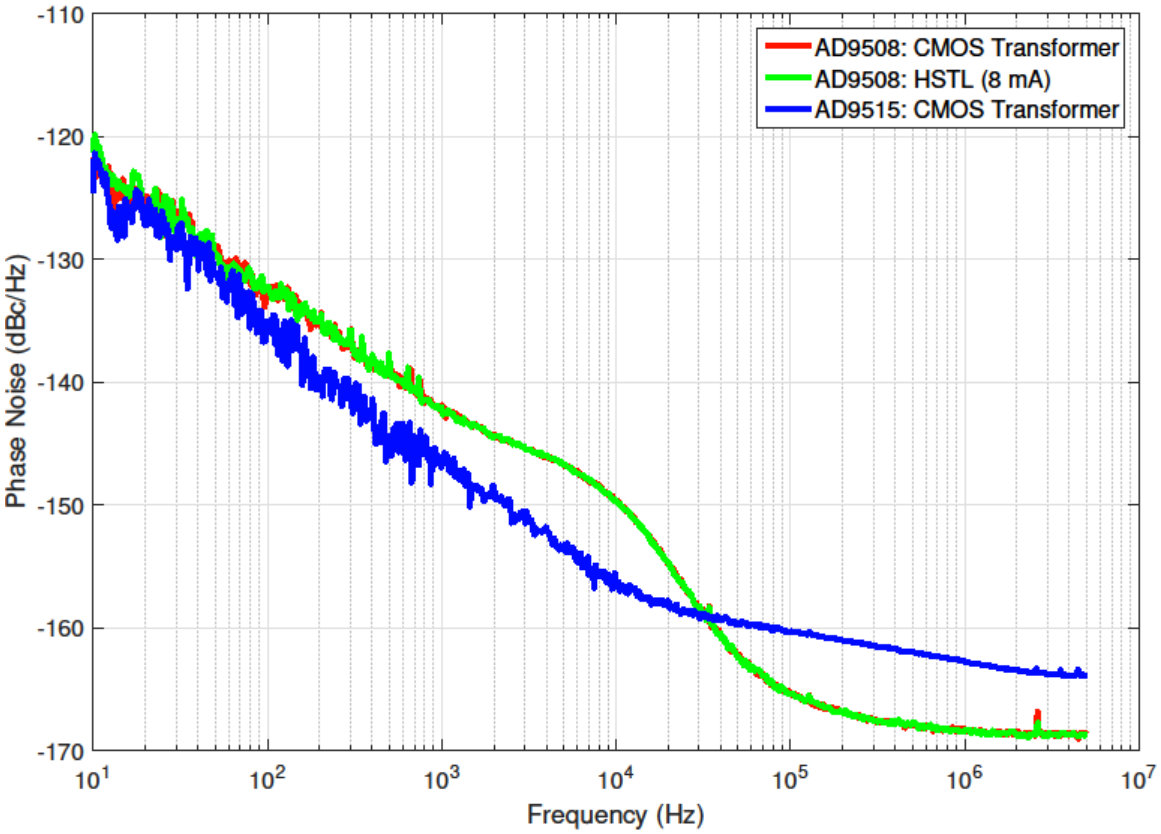

Figure 16. Phase noise spectra of frequency dividers for various output signaling standards and types of counters. Division ratio: 22, input frequency: 704.42 MHz.

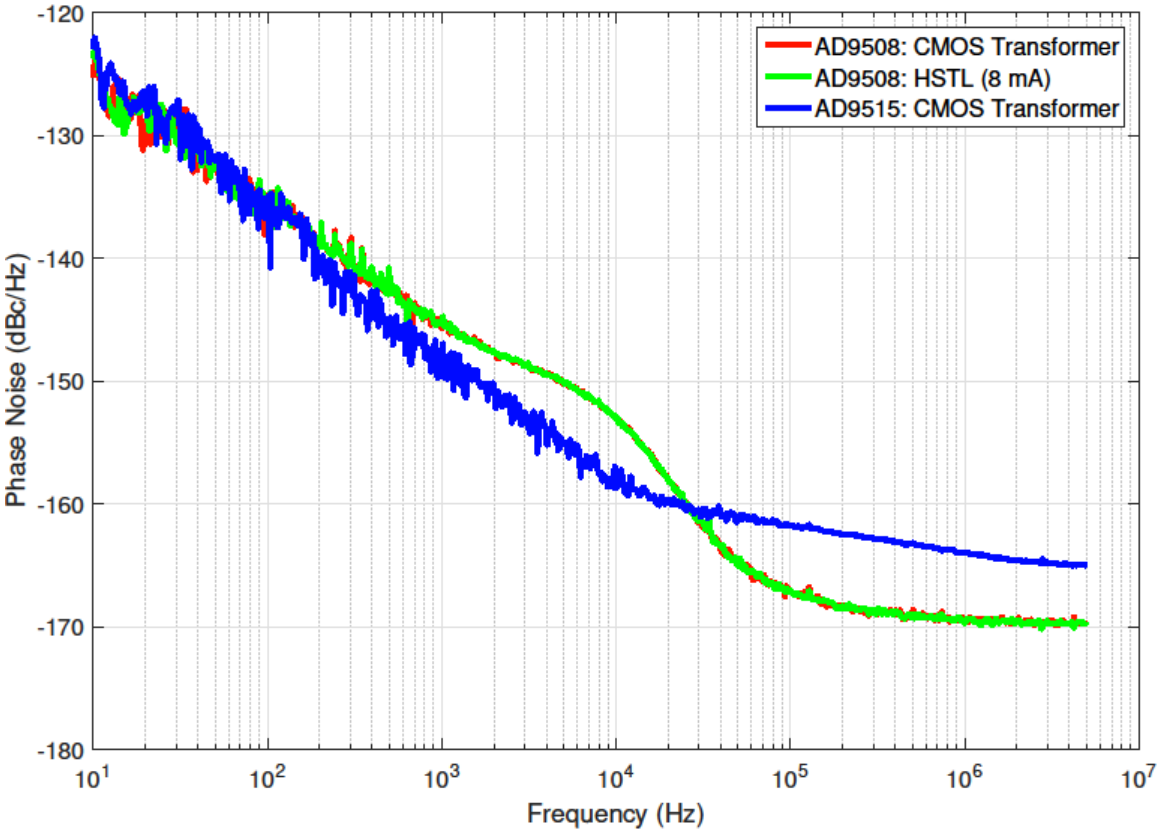

Figure 17. Phase noise spectra of frequency dividers for various output signaling standards and types of counters. Division ratio: 28, input frequency: 704.42 MHz.

Table 9. Comparison of output signal's Jitter (integrated phase noise) per frequency offset decade of selected frequency dividers. Division ratio: 22, input frequency: 704.42 MHz.

	Start offset	10	100	1 k	10 k	100 k	1 M	10	1 k
	End offset	100	1 k	10 k	100 k	1 M	5 M	5 M	5 M
	Standard								
AD9508	CMOS Single-ended	29.64	29.63	35.51	27.17	30.72	60.45	91.43	81.23
	CMOS Transformer	26.83	24.76	28.26	21.80	24.54	47.20	73.77	64.06
	LVDS (3.50 mA) Transformer	54.34	39.17	37.55	46.48	171.33	235.87	305.11	297.60
	LVDS (4.38 mA) Transformer	44.99	36.21	36.72	44.05	158.38	214.56	278.88	272.79
	HSTL (8 mA) Transformer	25.66	24.94	28.37	21.80	24.55	47.45	73.63	64.30
	HSTL (16 mA) Transformer	29.83	27.59	32.17	24.46	25.13	48.70	79.35	68.10
AD9515	CMOS Single-ended	25.60	18.80	16.39	23.38	55.41	97.19	119.78	115.46
	CMOS Transformer	21.64	16.23	16.03	22.80	53.50	92.76	113.93	110.64
	LVDS	40.26	28.50	20.95	38.91	120.79	229.69	267.87	263.26
	LVDS Transformer	30.72	22.80	17.82	26.51	116.43	141.89	190.24	186.40
	LVPECL 400 mV	28.33	19.21	11.33	19.12	58.81	128.02	146.74	142.64
	LVPECL 790 mV	19.52	11.79	7.55	13.29	43.35	116.22	127.06	124.97

Table 10. Comparison of output signal's Jitter (integrated phase noise) per frequency offset decade of selected frequency dividers. Division ratio: 28, input frequency: 704.42 MHz.

	Start offset	10	100	1 k	10 k	100 k	1 M	10	1 k
	End offset	100	1 k	10 k	100 k	1 M	5 M	5 M	5 M
	Standard								
AD9508	CMOS Single-ended	27.52	24.08	27.01	22.28	34.24	67.81	91.32	83.64
	CMOS Transformer	27.86	21.49	21.72	18.09	26.60	51.27	73.36	64.30
	LVDS (3.50 mA) Transformer	72.15	50.29	41.34	60.60	238.26	344.95	434.69	425.62
	LVDS (4.38 mA) Transformer	58.03	42.04	38.75	57.12	221.69	315.52	398.31	391.75
	HSTL (8 mA) Transformer	27.37	21.40	21.80	17.96	26.38	51.20	73.00	64.15
	HSTL (16 mA) Transformer	31.51	27.12	30.14	23.47	28.16	54.75	83.60	72.47

AD9515	CMOS Single-ended	30.17	21.42	17.27	24.58	59.48	107.01	131.42	126.07
	CMOS Transformer	25.12	18.62	16.82	24.34	58.55	103.79	126.73	122.78
	LVDS	50.07	34.78	24.64	52.77	166.81	336.04	384.56	379.66
	LVDS Transformer	38.48	28.04	19.94	31.30	152.31	184.26	246.63	241.86
	LVPECL 400 mV	34.36	23.52	14.87	32.79	103.85	221.29	250.60	247.08
	LVPECL 790 mV	25.14	19.05	21.84	29.48	59.71	104.56	129.79	125.87

Influence of IF Amplifier on LO Phase Noise

As discussed earlier, the IF signal should be strong enough to have a strong desired sideband by saturating the mixer on the IF port. The output power of the selected frequency divider is around +7.5 dBm.

The LO signal's phase noise was measured for the AD515 frequency divider, using a transformer converting the differential LVPECL signal to a single-ended one (+10 dBm output power), in following configurations:

- low-pass filter (LFCN-80+)
- 4 dB attenuator, low-pass filter (LFCN-80+)
- low-pass filter (LFCN-80+), LHA-1H+ amplifier, 10 dB attenuator, low-pass filter (LFCN-80+)
- low-pass filter (LFCN-80+), LMH6702 operational amplifier (+6 dB gain), low-pass filter (LFCN-80+)
- band-pass filter (SXBP-29+), low-pass filter (LFCN-80+)
- band-pass filter (SXBP-29+), LMH6702 operational amplifier (+6 dB gain), low-pass filter (LFCN-80+)

The close-to-carrier (below 10 kHz offset) phase noise is indistinguishable between configurations (see Figures 18 and 19). As can be seen in Figures 20 and 21, above the 10 kHz offset the solution utilizing the operational amplifier offers the best performance.

The LMH6702 operational amplifier was selected as the IF signal amplifier for the LO RTM project.

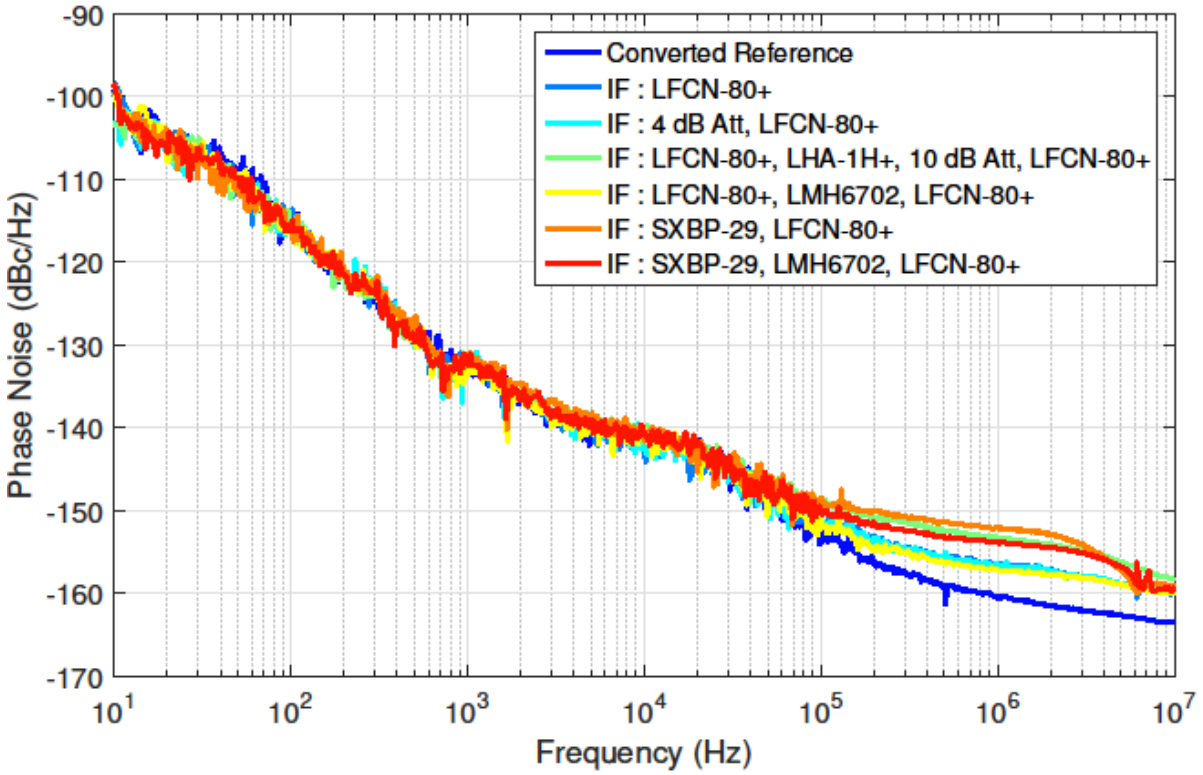

Figure 18. Phase noise spectra of LO signal for various IF signal conditioning paths. IF = 27.09 MHz.

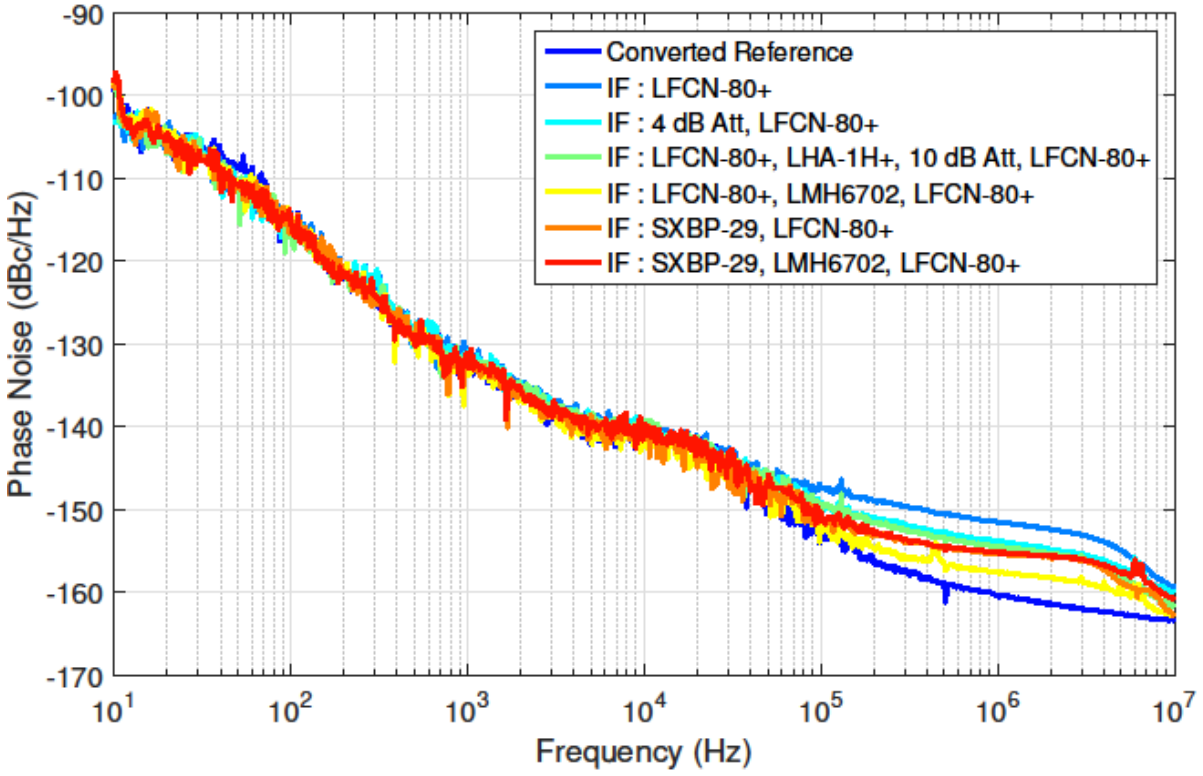

Figure 19. Phase noise spectra of LO signal for various IF signal conditioning paths. IF = 32.02 MHz.

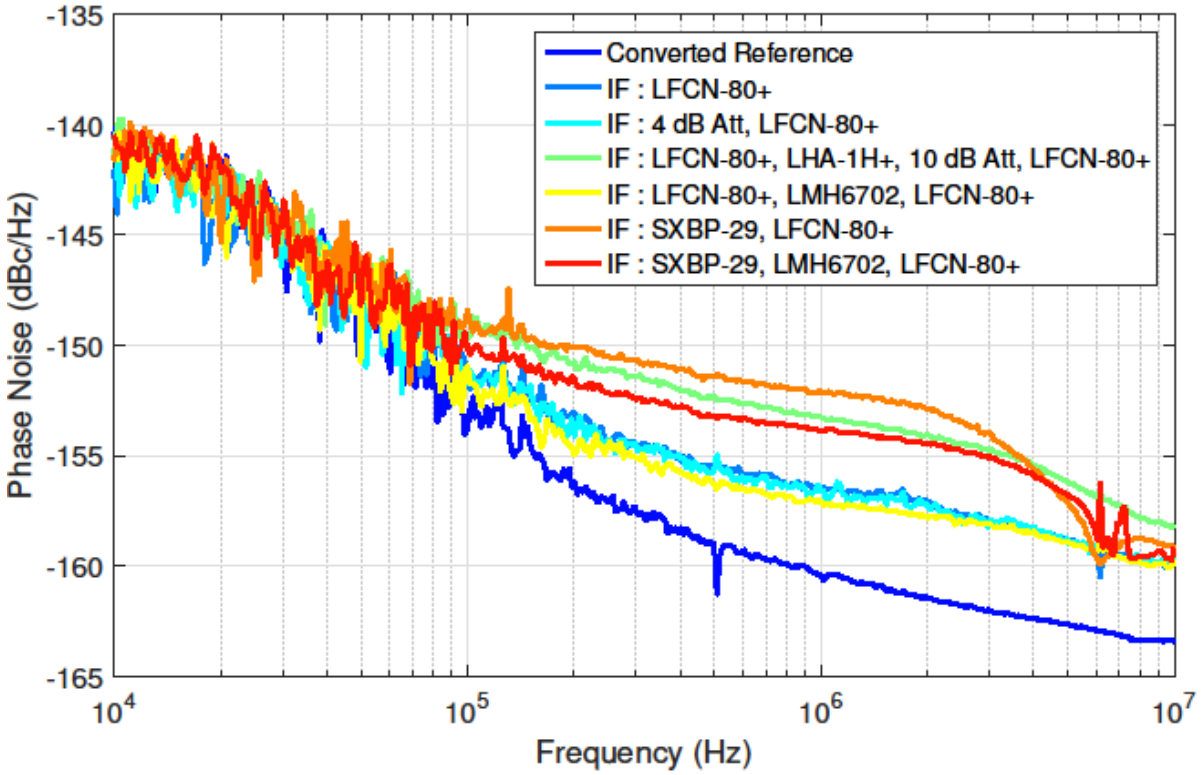

Figure 20. Phase noise spectra of LO signal for various IF signal conditioning paths (zoom in). IF = 27.09 MHz.

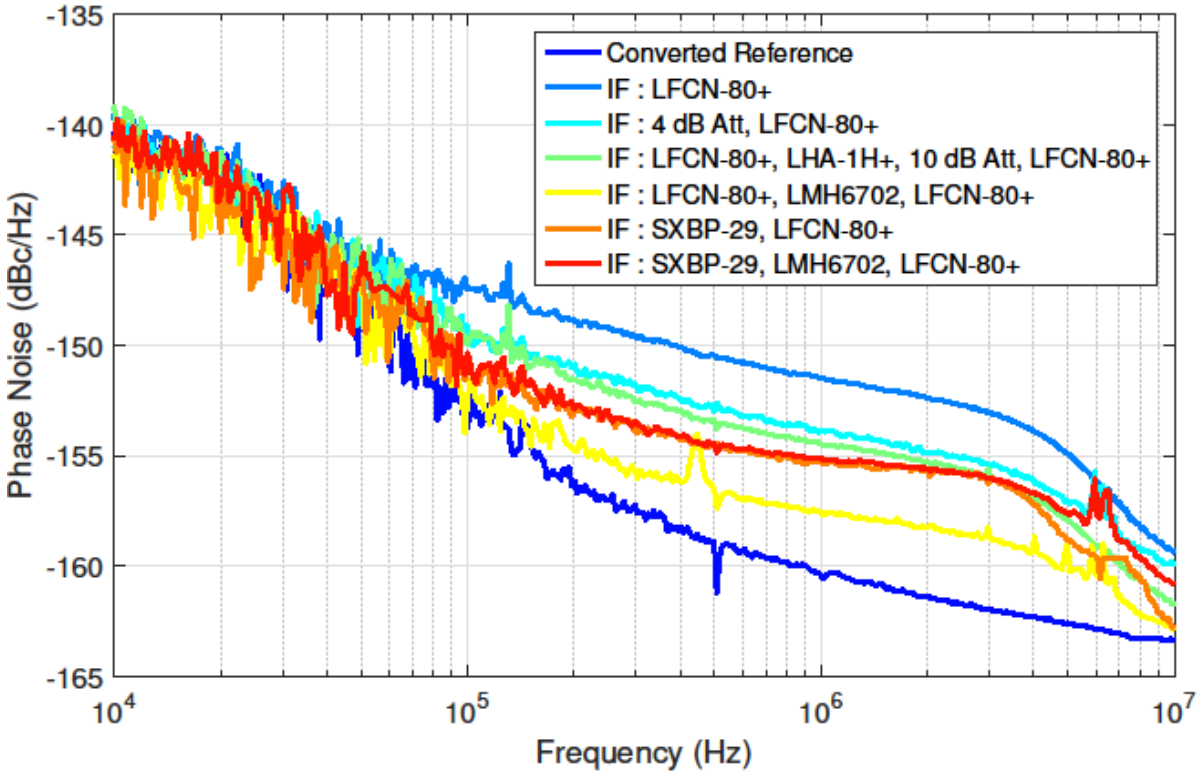

Figure 21. Phase noise spectra of LO signal for various IF signal conditioning paths (zoom in). IF = 32.02 MHz.

LO Signal Distribution

The desired sideband's power at the output of the band-pass filter is estimated to be around -5 dBm. This signal must be amplified and split to provide +15 dBm at each of four main outputs as well as feed diagnostic circuit and monitoring output.

Figure 22 depicts a block diagram of the proposed LO distribution circuit. At each of the LO outputs the nominal power is +15dB. For an ideal 4-way power splitter (6 dB loss) the signal must be amplified to +21 dBm. Extra 1 dB should be foreseen for insertion loss of the splitter and 0.5 dB to 1 dB for the low pass filter's loss. Therefore gain of 27 dB is needed and maximum output power must be above 23 dBm. Popular medium-power integrated amplifiers (for example HMC636 and ADL5530 from Analog Devices and LHA-1H+ from MiniCircuits) have insufficient maximum output power (missing more than 1 dB) and too low gain. The 1dB gain compression point is not guaranteed. Two stage power conditioning circuit is foreseen to amplify the LO signal. Low-pass filters are used to suppressed undesired harmonics of the signal. A low-pass filter after the power detector reduces the readout noise.

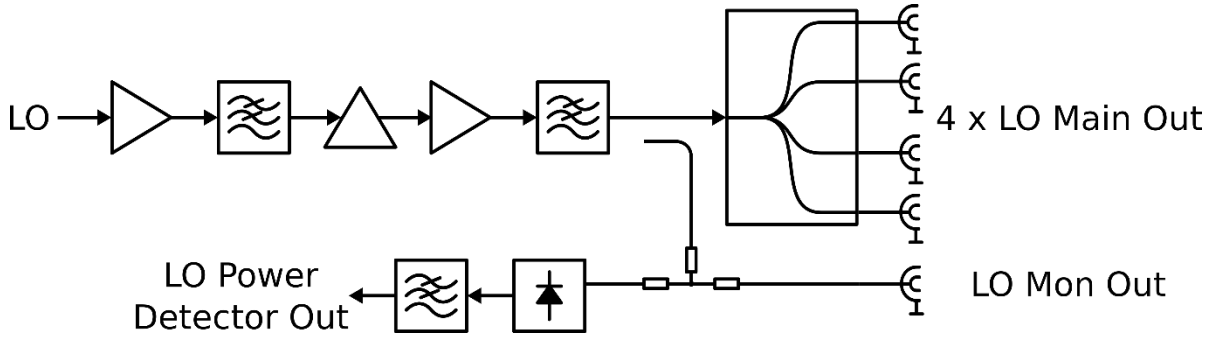

Figure 22. Block diagram of the LO conditioning circuit.

The low pass filter should suppress first few harmonics of the signal by more than 40 dB, including the 2nd one. The amplifiers and the low-pass filter were not yet selected at the time of writing of this report.

The LO amplifier's output signal should be decoupled to feed the board's monitoring output and diagnostic circuit. The DCW-30-272+ coupler from MiniCircuits was selected due to low loss and good matching. After coupling the signal can be split using a resistive divider.

The BP4C1+ power splitter from MiniCircuits was selected due to better matching at the sum port and lower losses compared to other considered splitters.

Clock frequency synthesis

As observed earlier in section “Proposed Schemes” (page 1) the clock frequency should be generated using a frequency divider. The two static frequency dividers considered for IF synthesis (AD9508 and AD9515) were compared with two stage divider using HMC794LP3E, which most probably is an injection-locked divider. This divider has the division ratio programmable in the 1 – 4 range. Two permutations of divide-by-2 and divide-by-3 exist and both were measured.

The same PLL-based reference frequency synthesizer was used as for the investigation of the IF signal’s phase noise. Both the phase noise spectra (shown in Figure 23) and the integrated jitter per decade of frequency offset (summarized in Table 11) indicate the two stage divider using HMC794LP3E as the best solution for clock frequency synthesis. Figure 23 shows only the best plots for AD9508 and AD9515 dividers.

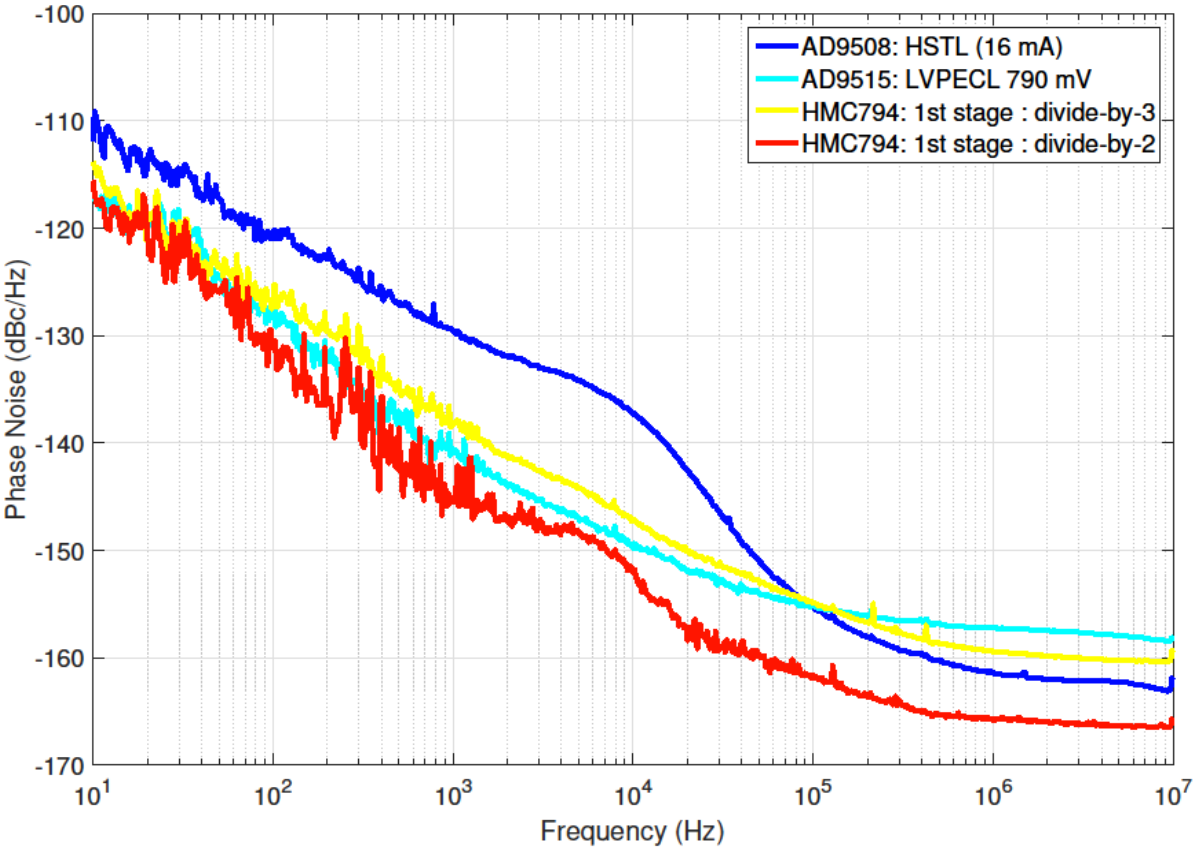

Figure 23. Phase noise spectra of frequency dividers for various output signaling standards and types of dividers. Division ratio: 6, input frequency: 704.42 MHz.

Table 11. Comparison of output signal's Jitter (integrated phase noise) per frequency offset decade of selected frequency dividers. Division ratio: 6, input frequency: 704.42 MHz.

	Start offset	10	100	1 k	10 k	100 k	1 M	10	1 k
	End offset / Standard	100	1 k	10 k	100 k	1 M	10 M	10 M	10 M
AD 9508	CMOS Single-ended	28.60	31.58	39.26	28.96	21.23	50.00	84.56	73.01
	CMOS Transformer	27.35	29.80	36.83	27.01	19.08	44.56	77.94	66.60
	LVDS (3.50 mA) Transformer	27.56	29.50	36.69	26.30	95.85	63.90	130.20	123.71
	LVDS (4.38 mA) Transformer	26.30	29.10	35.63	26.83	143.97	60.33	167.10	162.44
	HSTL (8 mA) Transformer	27.47	29.95	36.68	26.79	18.99	44.50	77.84	66.36
	HSTL (16 mA) Transformer	27.06	29.38	36.55	26.64	18.71	43.77	76.87	65.66
AD 9515	CMOS Single-ended	15.26	16.70	17.08	22.47	44.84	85.81	103.37	100.85
	CMOS Transformer	14.78	16.34	17.25	22.60	45.11	84.92	102.68	100.27
	LVDS Single-ended	15.21	16.88	17.25	23.94	58.87	94.25	117.21	114.97
	LVDS Transformer	15.79	17.22	17.63	23.80	79.39	93.91	128.66	126.49
	LVPECL 400 mV	11.88	7.45	6.72	10.15	28.56	80.68	87.58	86.45
	LVPECL 790 mV	13.68	9.39	8.88	12.18	26.44	72.87	80.70	78.97
HMC 794	1st stage divide-by-3 2nd stage divide-by-2	15.07	13.38	12.89	14.07	20.49	47.78	58.95	55.38
	1st stage divide-by-2 2nd stage divide-by-3	11.44	6.79	6.86	6.38	10.45	28.03	34.09	31.35

Clock Signal Distribution

The clock signal at the output of the frequency divider has power level around +10 dBm. This signal must be amplified and split to provide +15 dBm at each of four main outputs as well as feed diagnostic circuit and monitoring output.

Figure 24 provides a block diagram of the proposed clock distribution circuit. At each of the clock outputs the nominal power is +15dB. For an ideal 4-way power splitter (6.02 dB loss) the signal must be amplifier to +21 dBm. Extra 0.5 dB should be foreseen for insertion loss of the splitter and 0.5 dB to 1 dB for the low pass filter. The desired sideband's power at the band-pass filter output is estimated to be around +10 dBm. Therefore gain of 11.5 dB is needed and the maximum output power should be above 22.0 dBm to reach the nominal 15.0 dBm power at each output. Low-pass filters are used to suppressed undesired harmonics of the clock signal to meet harmonics' level requirement. A low-pass filter after the power detector reduces the readout noise.

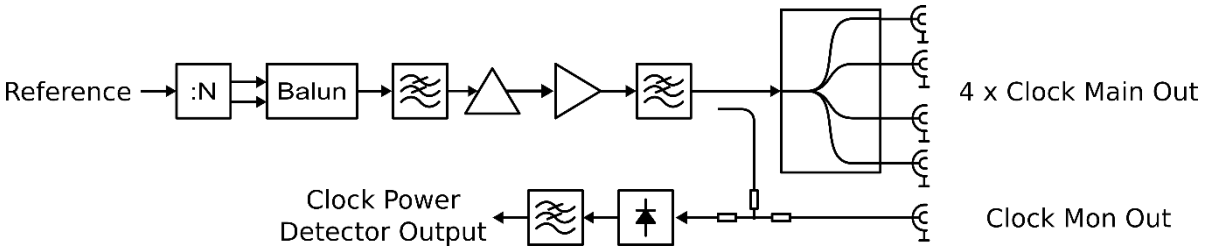

Figure 24. Block diagram of the clock conditioning circuit.

Typical medium-power integrated amplifiers (for example ADL5530 from Analog Devices and LHA-1H+ from MiniCircuits) have output power close to the desired power (22.7 dBm for LHA+1 and 21.8 dBm for ADL5530) and too high gain. Attenuating the clock signal even down to 0 dBm should not deteriorate the phase noise performance. Figures 25 and 26 present the spectral components power levels as functions of the clock power level. ADL5530 has significant 2nd harmonic present even at moderate input power levels. LHA-1H+ offers higher maximum output power level and lower 2nd harmonic in saturation (for maximum fundamental power).

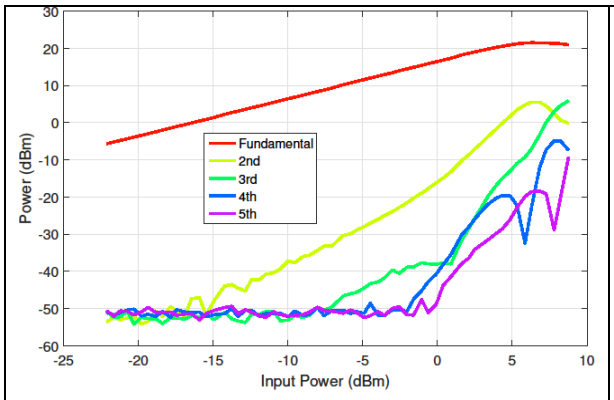

Figure 25. Spectral components at the output of the ADL5530 amplifier. Input frequency = 117 MHz.

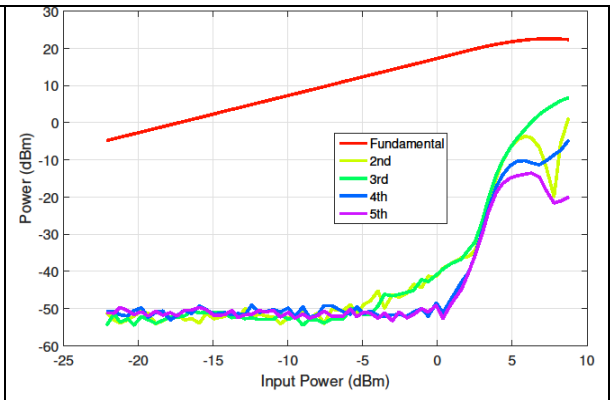

Figure 26. Spectral components at the output of the LHA-1H+ amplifier. Input frequency = 117 MHz.

The low pass filter should suppress all harmonics of the signal to -60 dBc, including the 2nd one. The LFCN-80+ from Mini Circuits satisfies the requirement.

The influence of the proposed amplifiers on the phase noise was verified. As can be seen in Figures 27 and 28, ADL5530 adds some insignificant phase noise (below 1 dB above 100 kHz offset) and LHA-1H+ adds no visible noise (the measured spurs are most probably caused by the power supply used).

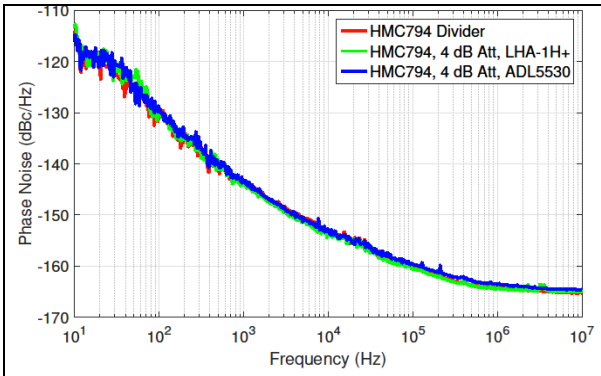

Figure 27. Phase noise spectra of frequency divider and the proposed clock signal amplifiers.

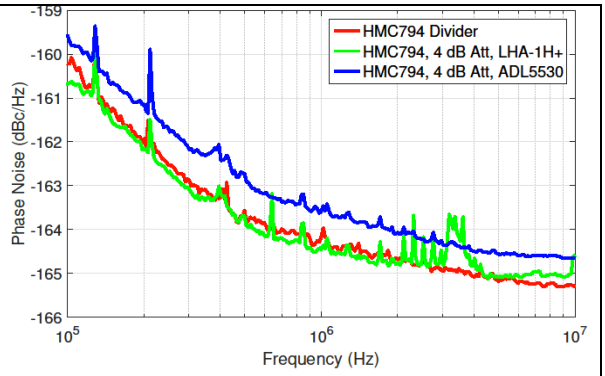

Figure 28. Phase noise spectra of frequency divider and the proposed clock signal amplifiers (zoom in).

LHA-1H+ amplifier was selected as it provides sufficient output power, has low level of odd harmonics when operating in saturation, and doesn't add any significant phase noise.

Part of the clock amplifier's output signal should be decoupled to feed the board's monitoring output and diagnostic circuit. The ADC-26-52+ coupler from MiniCircuits was selected due to low loss and good matching. The coupled signal can be split using a resistive divider. A low-pass filter after the power detector reduces the noise.

The SCA-4-10+ power splitter from MiniCircuits was selected due to good matching, lower losses compared to other considered splitters, and small difference of power between outputs (below 0.3 dB).

Reference Conditioning

The expected input power of reference signal is in the 1 dBm – 5 dBm range. The signal must be amplified and split to feed two frequency dividers (IF and clock), a mixer, and the reference output.

The power requirements of each component and the reference output are listed in Table 12. If a 2-way splitter is used (reference output connected to 1st branch of the splitter and everything else feed by a 3-way splitter connected to the 2nd branch) the amplifier's output should be at least +18 dBm (1 dB los foreseen for splitter and 1 dB for low pass filter). Figure 29 shows the proposed reference distribution circuit.

Table 12. Power of the reference signal required by different components and outputs.

Name	Power range (dBm)
Reference output	+13 ± 1 dB
IF divider (AD9508)	+7 to +13, +8 preferred
Clock frequency divider	-1 do +10
LO mixer	-5 to +10

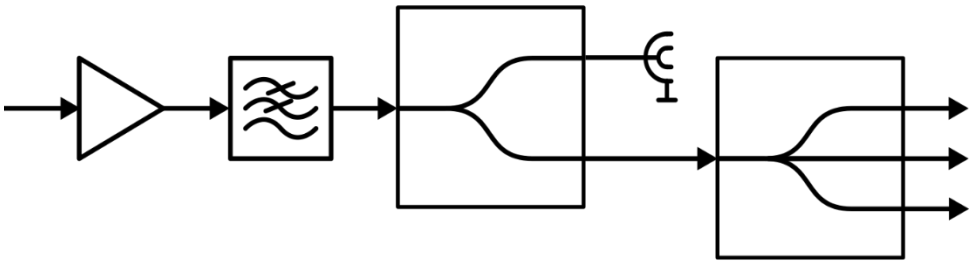

Figure 29. Block diagram of proposed reference distribution circuit.

Keeping the distributed reference power independent of the input power level can be executed by using a variable gain amplifier (typically made of an attenuator and an amplifier). Another solution is saturating the amplifier in the input power range. Figure 30 compares characteristics (output power vs input power) of different amplifiers. LTC6431-20 provides +19.8 to +20.2 dBm output power in the expected input power range and was selected for the project.

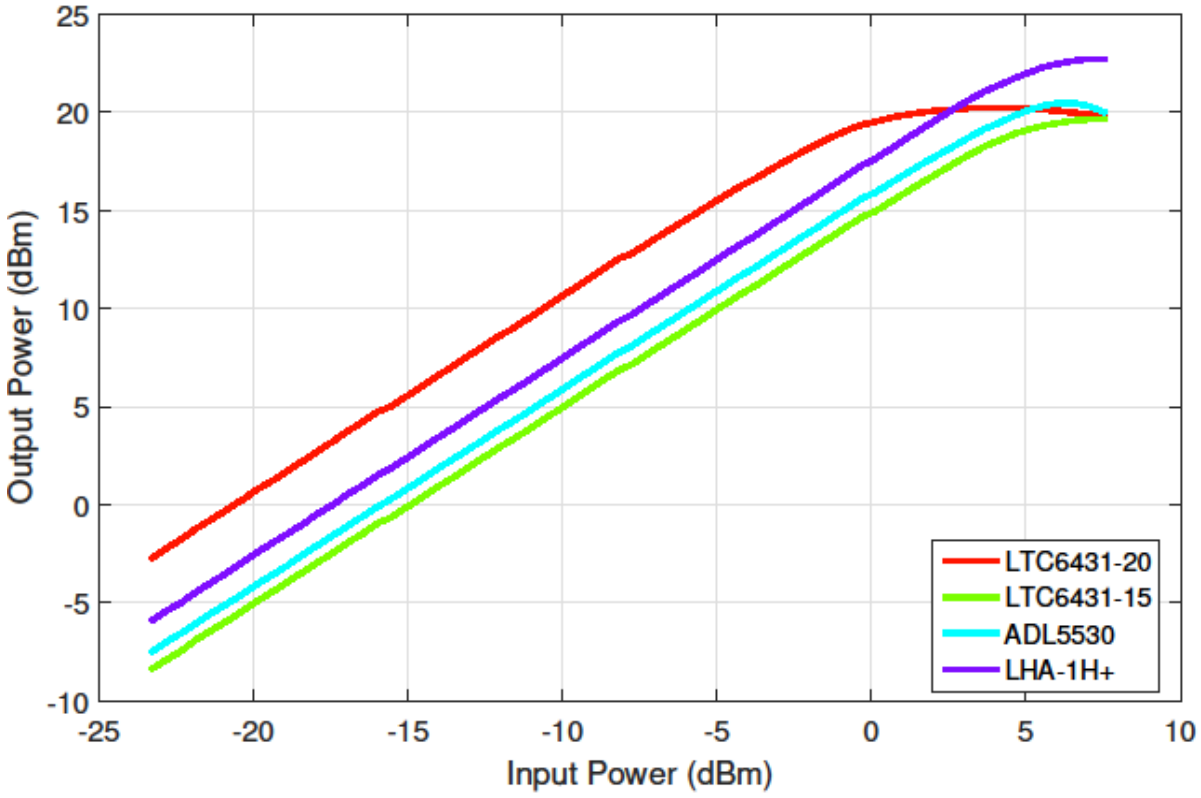

Figure 30. Power of the fundamental spectral component of different amplifiers as a function of the input power. Input frequency 704 MHz.

Diagnostic

The power of clock and LO signals before the final splitter must be measured for diagnostic purposes. The coupling of measured signals into power detector circuit was presented in previous sections of this document. The desired maximum absolute error is ± 1 dB and read-out resolution should be 0.05 dB or better. The input power should vary slightly in normal operating conditions and power detector's input power will be sufficiently high (-15 dBm for LO and -10 dBm for clock) for almost any detector to operate properly. The input signal should have sine wave shape with very little harmonics present in the spectrum. All aforementioned operating conditions of the power detector chip are favorable. AD8314 logarithmic power detector was selected based on price comparison and impedance matching numbers.

The AD8314's output signal must be digitized for the control system to read. The signal increases from close to ground to about 1.2 V as the input power increases. With 20 mV/dB slope the resolution of 0.05 dB can be achieved using an ADC with 10.3 effective bits (assuming 1.225V reference).

The AD8314's output signal should be low-pass filtered before sampling to limit the noise bandwidth. The capacitor at the output of the RC filter can also works as current source during charging of the ADC's sample and hold circuit. The digitized values must be transmitted to the control system via the AMC module.

Digital Circuit and Communication Interface

The RTM must communicate with an AMC module using two three row ADF Zone 3 connectors using pin assignment complaint with the DESY ZONE3 Digital Class D1.0 recommendation[1]. The Class allows LVDS, LVCMOS 2.5V, or open collector 2.5 V signaling over the Zone 3 connector, while various programmable integrated circuits on the LO board require CMOS/TTL 5V signaling, 3.3 V open collector, or LVCMOS 3.3V signaling. The signals might be converted using different types of level converters and buffers or by adding a programmable device communicating with both the AMC and on-board integrated circuits. The second solution was selected as it offers additional flexibility (processing of commands, start-up, stand-alone operation) at similar cost.

Devices from the MachXO2 PLD family supports various signaling standards, have built-in LDOs, generators, and non-volatile memory. The data transferred between the RTM and the AMC is fairly low, therefore serial protocol will be sufficient. Serial Peripheral Interface (SPI) typically uses single-ended signaling standards such as CMOS 5V or LVCMOS 3.3V, but we proposed to use it with LVDS signaling. Two unidirectional lines (MISO and MOSI) will be used, with PLD being the slave. Two byte transactions are foreseen, with first byte being the address and the second the data. Detailed signal assignment on the Zone 3 connectors will be agreed with RTM Carrier designers. A detailed register map will be presented in future.

MTCA.4 Management

The requirement document mandates monitoring of supply voltages and temperature. Such functionality lays within the responsibility of the MTCA.4 management circuit.

The management circuit is required for all RTM boards. At minimum an EEPROM containing FRU information and an I^2C expander controlling the status LEDs and checking power good signals must be

[1] Available at http://mtca.desy.de/resources/zone_3_recommendation/index_eng.html

present. Other components can be connected to microcontroller or directly to the Intelligent Platform Management Bus/Bridge (IPMB).

MAX6625 chip was selected for temperature monitoring. It offers 0.5° resolution, ±1.5° accuracy, and will be connected to the I^2C bus. LTC2913 IC was selected for voltage monitoring. It monitors both under and overvoltage conditions for two voltages and has open-collector outputs which can be directly connected to the power good pin on the I^2C expander.

Power supply

According to the MTCA specification the +12 V payload power is available to modules, with maximum current for the RTM board limited to 2.5A. The management circuit is powered by an independent +3.3V rail with current limited to 50 mA.

Manufacturing and Verification

The Quality Plan is a document describing PEG's quality assurance policies in detail. It is presented separately as a part of the PDR documentation.

The final deliverable of the LO RTM subproject is a set of electronic modules consisting of printed circuit board and assembled electronic components. The design should make use of standard substrate materials and components, recommended for new designs, available from main distributors, and preferably interchangeable between various manufacturers. All components must be compliant with RoHS Directive.

The PEG will outsource PCB manufacturing and assembly services to business partners. To ensure quality the bill of materials given to the assembly shop will contains manufacturer's names and ordering codes. The technical documentation (PCB design, assembly drawings, bill of materials, stack-up) will be provided in the industry standard formats (where applicable) to a selected business partner. The partner will manufacture the PCBs and assemble the electronic components. The PCBs will be electrically tested before the assembly. The assembled modules will be visually inspected by both manufacturer and the PEG and later electrically tested by the PEG to verify correctness of assembly and PCB manufacturing. The devices shall be tested using a dedicated setup. Various electrical parameters will be measured using external instrumentation. Compliance to the technical specification will be determined according to a test plan. The detailed plan of tests, including acceptance criteria, will be presented during the Critical Design Review. Test reports will be written.

The LO RTMs will be delivered to ESS as a part of MTCA-based LLRF systems assembled by the Polish Electronic Group. The whole system will be tested both in Poland and after final installation at ESS. The test procedures for those stages are not covered by this plan.

Schedule

A time schedule of planed activities is given in Table 13.

Table 13. Time schedule of planed activities

Activity	Start	End
First prototype: production and assembly	05-06-2017	31-07-2017
First prototype: measurements	31-07-2017	04-09-2017
RTM prototype: design	05-06-2017	06-11-2017
RTM prototype: CDR	13-11-2017	
RTM prototype: production and assembly	20-11-2017	15-01-2018
RTM prototype: measurements	15-01-2018	26-02-2018
M-Beta RTM: design	20-11-2017	26-03-2018
M-Beta RTM: production, assembly, testing	02-04-2018	17-12-2018
Test stand preparation	05-06-2017	30-04-2018

Design Status

The design of the first prototype (CS-LOG) is complete. A visualization of the assembled PCB can be seen in Figure 31. The PCB is not in RTM format, as it will be used in the Cavity Simulator project.

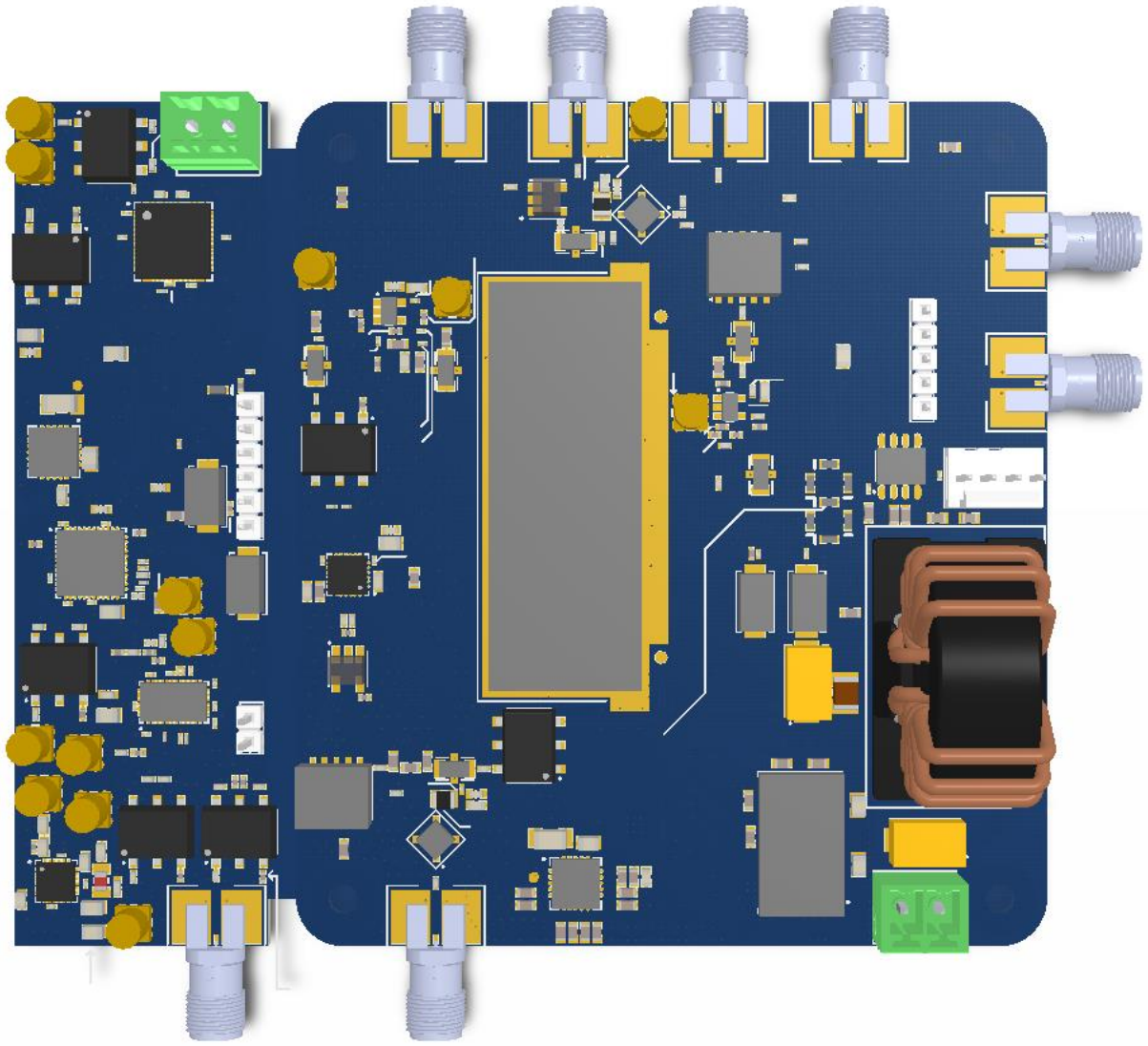

Figure 31. Visualization of the assembled PCB.

Final Block Diagram

Figure 32 depicts the block diagram of the LO RTM design.

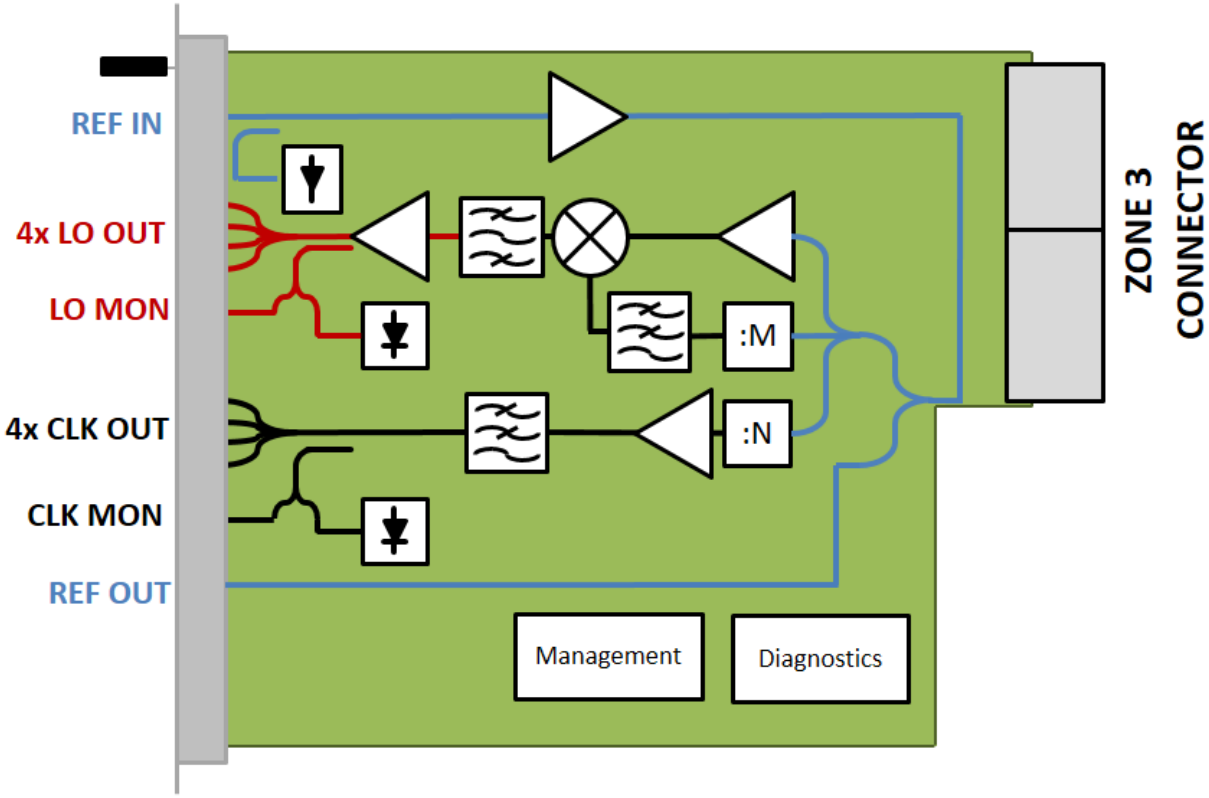

Figure 32. Simplified block diagram of the LO RTM design.

Conclusions

A list of performance and functional requirements was given. In this document three LO frequency synthesis schemes were presented. Based on comparison of measured performance characteristics the Direct Analog Synthesis was selected. For the clock signal two frequency division schemes were discussed. Direct Digital Synthesis was excluded due to systemic frequency error and solution utilizing frequency dividers was chosen. The measured characteristics of components necessary in each of the selected schemes was analyzed. The conceptual design of diagnostic, monitoring, communication, and power conditioning circuits was presented. The status of the design and final block diagram were given. An overview of quality assurance policies and time schedule of the project were provided.