Description:	This document describes the design of the Cavity Simulator designed for the tests of the ESS LLRF control system
Title:	**Preliminary Design Report for the Cavity Simulator**

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Version:	1.0
Date:	23.05.2017

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1 INTRODUCTION

1.1 Overview of the Cavity Simulator

The Cavity simulator is a device used for development and testing of M-Beta and H-Beta LLRF control systems used at the ESS facility in Lund (Sweden). It is also used for the testing of the LLRF control systems components after their installation in the ESS Klystron Gallery.

The device emulates a behavior of an accelerating cavity together with a klystron/IOT RF power amplifier. Based on the input signals (RF drive and piezos' drive) the device generates following output signals:

- amplifier input,
- amplifier forward,
- amplifier reflected,
- cavity forward,
- cavity reflected,
- cavity pick-up,
- amplifier PSU modulator I/U,
- piezo sensor.

The block diagram of the simulated system is presented in Figure 1.

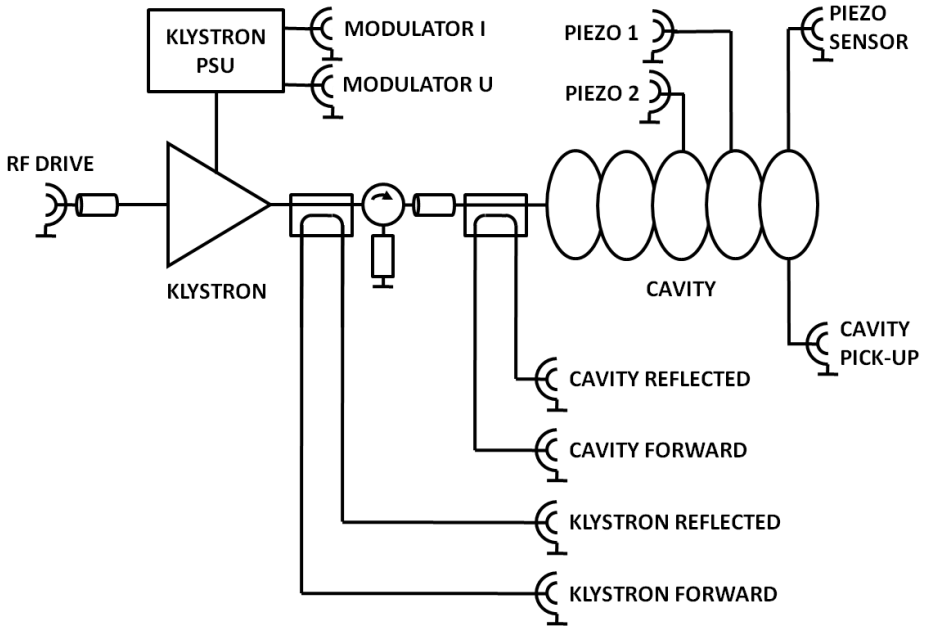

Figure 1 Block diagram of a system simulated by the Cavity Simulator.

This device simulates following effects:

- cavity dynamics (without other pass-band modes),
- cavity detuning,
- piezo compensation,
- lorentz force detuning,
- beam current,
- microphonics,
- quench,
- mechanical modes,
- coupler heating,
- ponderomotive effect,
- amplifier non-linearity,
- amplifier PSU modulator influence.

The model of the simulated system is implemented in a digital signal processing unit. To operate with analog signals, set of data converters with dedicated analog front-end is provided. Several solutions for digitizing and generating RF signal are compared in the section 2 of this document. The simplified block diagram of the Cavity Simulator is shown in Figure 2.

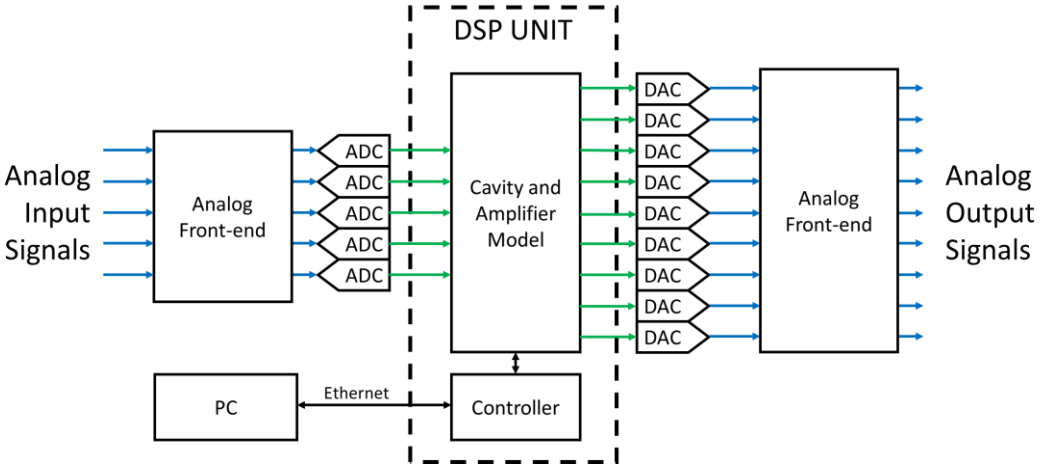

Figure 2 Simplified block diagram of the Cavity Simulator.

All parameters of the simulation can be set on-line by the control software. An application programming interface (API) for integration of the device with other systems, for example LLRF system test stand, is provided.

The internal reference signal generator is also provided inside the device.

1.2 Cavity Simulator Requirements

The main requirements are:

- RF outputs:
  - Number of outputs: 6 (main) + 6 (monitoring)
  - Maximum output power: 15 dBm (main), 5 dBm (monitoring)
  - Center frequency: 704 MHz
  - Bandwidth: 10 MHz
- RF inputs: 2
  - Number of inputs: 2
  - Center frequency: 704 MHz
  - Bandwidth: 10 MHz
- High Voltage analog inputs
  - Number of inputs: 2
  - Voltage range: ±100 V
  - Bandwidth: 100 kHz
- Fast analog outputs:
  - Number: 2
  - Bandwidth: 1 MHz
- Analog outputs:
  - Number: 1
  - Bandwidth: 100 kHz
- Communication interfaces:
  - Ethernet
  - USB (JTAG)
- Power supply: 230 V
- Power consumption: <250 W

2 CAVITY SIMULATOR HARDWARE ARCHITECTURE

The Cavity Simulator digitizes the RF drive and piezo signals coming from a LLRF control system. The signals are processed by a DSP unit. Digital signals are send to DACs, which generate the output signals that are fed back to the LLRF control system.

RF input signals can be digitized using one of the following schemes:

- direct sampling,
- down-conversion,
- analog IQ demodulation.

The operating frequency of the Cavity Simulator (704 MHz) is close to the maximum bandwidth of the typical ADCs, with sampling rate around 150 MSPS, therefore use of the direct sampling is not suitable. The down-conversion scheme requires additional LO signal, but offers better linearity and intermodulation performance than the analog IQ

demodulation. The down-conversion scheme was selected for the design. In total 2 digitizing channels are needed, but to gain some flexibility it was decided to add additional 2 fast ADCs.

The total latency of Cavity Simulator should match the delay of the real system. According to information presented in: "LLRF performance evaluation" by Friedrik Kistensen the delay of the real system is around 0,35 μs. At planned clock signal frequency (117.4 MHz) it is equal to around 41 clock cycles. The latency of a typical ADC (ADS42LB69) and DAC (AD9783) is 10 and 7 clock cycles respectively. This results in maximum delay of the signal processing to be 21 clock cycles. In order to achieve that, the signal processing is performed on a high performance FPGA. To limit the time and the cost of the design it was decided to use off the shelf module equipped with at least 2 FMC connectors that can be used to connect the data converters.

The easiest way to generate an output signal would be to use a DAC with sampling frequency higher than 1500 MHz. With 6 16-Bit DACs it will require a data transfer rate of around 144 Gbit/s. This will strongly increase the cost of the FPGA device. The other way to generate an RF signal is to use a vector modulator, that generates a signal with the bandwidth limited around a certain carrier frequency. Using vector modulator allows to limit the data rate needed for the data converters and to improve the noise performance. The device needs 6 output channels, but it was decided to add additional 7th vector modulator channel, that can be used for debugging.

Additional data converters for slow analog signals are needed (for piezo and RF amplifier modulator signals). This data converters, together with fast ADC and vector modulators, are placed on the module equipped with 2 FMC connectors. This module is connected to the FPGA processing board. Because of the limited bandwidth of a down-converter it was decided to design it as separate module.

Two high voltage inputs for piezo require dedicated analog frontend. It simulates the capacitance of the piezo and lowers the high voltage to the range acceptable by ADCs on the FMC Data Converters Module.

Down-converters require additional LO signal for operation. This signal, together with the clock signal for data converters, is generated on the LO Generation Module. It will be based

on the same scheme as proposed for the LO RTM module designed by PEG for the ESS LLRF control system.

The vector modulators and LO Generation Module require RF reference signal to operate. This signal can be feed externally or generated inside the Cavity Simulator. The Reference Generation Module is equipped with a low noise PLL driven from a crystal oscillator.

All devices present in the Cavity Simulator are powered by +12V DC. The quality of the power supply directly affects performance of the whole device. Two stages of power supply are used. First, 230V AC is converted to 24V DC using off-the-shelf AC-DC converter. Then +24V DC is lowered to +12 V DC by using the custom power supply module, with a set of low noise DC-DC converters and a protection circuits. This module is also responsible for a control of cooling fans.

The block diagram of the Cavity Simulator hardware is presented in Figure 3.

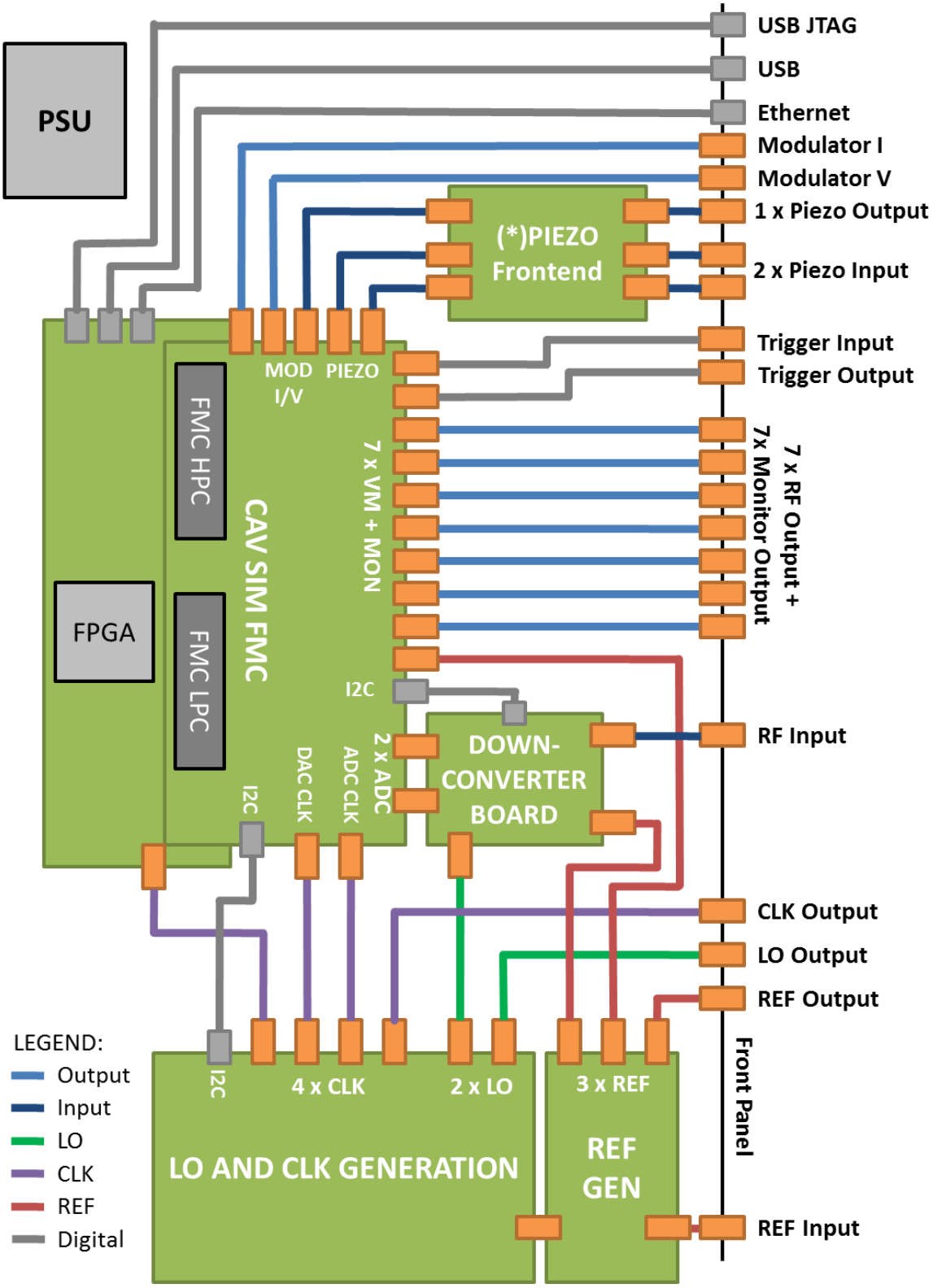

Figure 3 Block diagram of the Cavity Simulator hardware.

3 INTEERNAL MODULES DESIGN

In this section conceptual design of all internal modules used in the Cavity Simulator is presented.

3.1 FPGA Processing Module

The FPGA Processing Module is the central module of the Cavity Simulator. It communicates with all the other modules and perform complex digital processing. It was decided to use off the shelf board with two FMC connectors. Because of the engineers experience, the Xilinx FPGAs are preferred. For direct comparison 4 boards were chosen:

- Xilinx KC705
- Xilinx ZC706
- Xilinx ZCU102
- Xilinx KCU105

The comparison of the modules is presented in Table 1.

Table 1 Comparison of the FPGA modules.

	KC705	ZC706	ZCU102	KCU105
FPGA	Kintex 7 XC7K325T	Zynq 7000 XC7Z045	Zynq Ultrascale XCZU9EG	Kintex Ultrascale XCKU040
CPU	-	Dual-core ARM Cortex-A9 MPCore	Quad-core ARM Cortex-A53	-
Logic Cells (K)	356	350	600	530
Block Ram (Mb)	25.74	19.1	32.1	21.1
DSP Slices	1440	900	2520	1920
RAM Type	DDR3	DDR3	DDR4	DDR4
RAM Capacity	1 GB	2 x 1 GB	4 GB+512 MB	2 GB
FMC Connectors	**HPC:** 58 x LVDS, 4 x GT **LPC:** 34 x LVDS. 1 x GT	**HPC:** 34 x LVDS, 8 x GT **LPC:** 34 x LVDS. 1 x GT	**HPC:** 34 x LVDS, 8 x GT **HPC:** 34 x LVDS. 8 x GT	**HPC:** 57 x LVDS, 8 x GT **LPC:** 34 x LVDS. 1 x GT

Xilinx ZCU102 offers the biggest number of resources and an integrated CPU, that can be used for communication with a PC. Unfortunately, the availability of the module is very

limited and the standard lead time is about 2 months. To avoid delays in the project, KCU105 was selected. The photo of this module is presented in Figure 4.

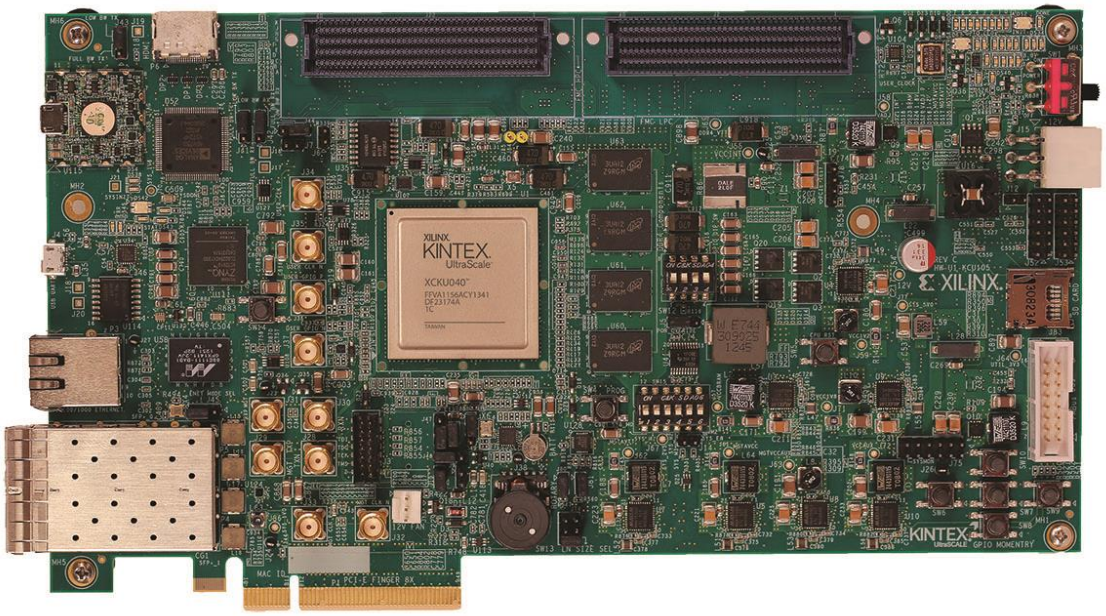

Figure 4 Photo of the Xilinx KCU105 FPGA module. Source: https://wwws.samtec.com/standards/xilinx.aspx

3.2 FMC Data Converters Module

To meet all requirements mentioned above the FMC Data Converters Module shall be equipped with:

- 7 vector modulator channels,
- 4 fast ADCs,
- 2 fast DACs,
- 2 slow ADCs,
- 2 slow DACs,
- clock generation circuit,
- reference signal distribution circuit.

Because of the limited number of IOs present in the FMC connectors, additional low cost FPGA is needed. It is responsible for configuration of all modules used in the Cavity Simulator. Slow data converters and fast DACs are also connected to this FPGA.

The block diagram of the Data Converters Module is presented in Figure 5.

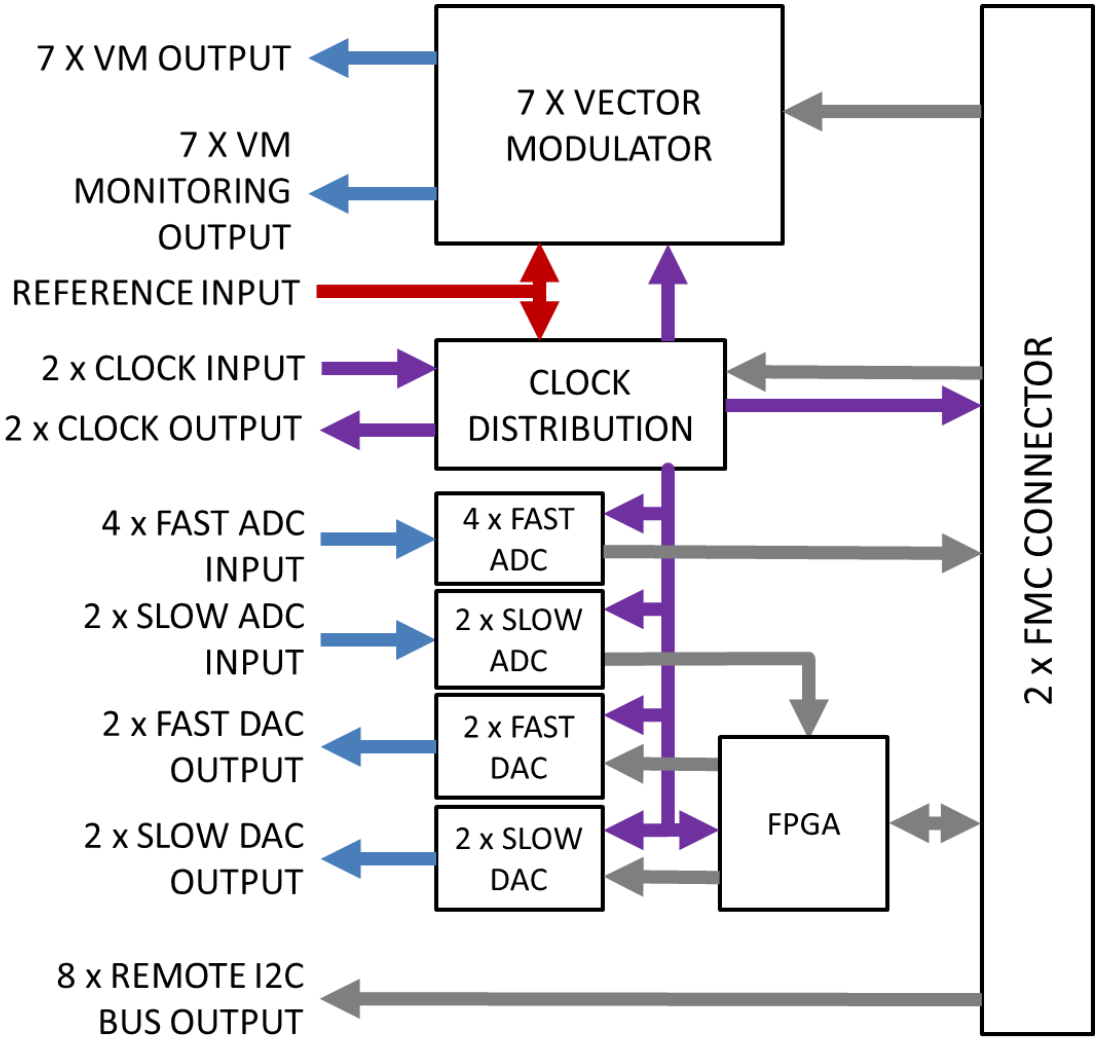

Figure 5 Block diagram of the data converters FMC module.

3.2.1 Vector Modulator Channels

The vector modulator channels are used to generate RF output signals. The I and Q signals are generated using a dual channel fast DAC.

This module will be equipped with 7 vector modulator channels. Each channel consist of:

- dual channel fast DAC,
- baseband signal conditioning circuit,
- vector modulator chip,
- RF amplifier,
- programmable attenuator,
- RF switch,
- coupler.

The block diagram of a single VM channel is presented in Figure 6.

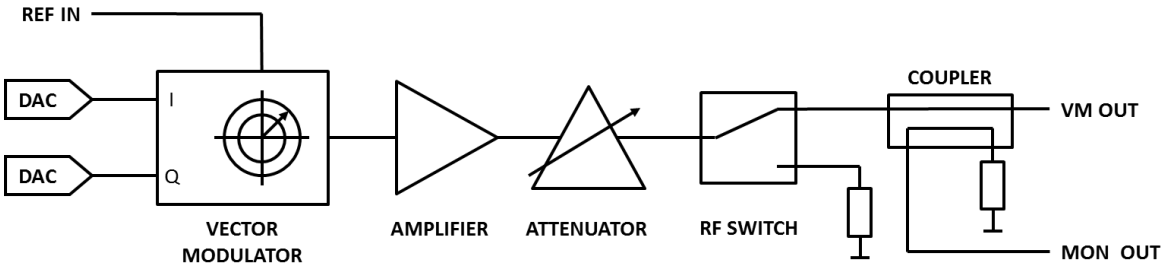

Figure 6 Block diagram of the vector modulator channel.

The most important parts of the channel are the DAC and vector modulator chip. Careful selection of this components is crucial for the noise and intermodulation performance of the Cavity Simulator. The comparison of the selected DACs and VM chips is presented in tables 2 and 3.

Table 2 DAC comparison.

Part Number	Sampling Rate [MSPS]	NSD [dBc/Hz]	SFDR [dBc]	IMD	Latency
DAC3282	625 (x2 Interpolation)	-150	-64	-69	38
DAC3283	800 (x4 Interpolation)	-160	-72	-86	59
DAC5682Z	1000 (x2 Interpolation)	---	-77	-67	78
DAC3482	1250 (x2 Interpolation)	-155	-72	-77.5	140
AD9146	1200 (x4 Interpolation)	-164	-67	-81	64
AD9783	500	-165	-80	-86	7
AD9747	250	-165	-82	-86	7

All DACs except for ADC9783 and AD9747 are not suitable, because of high latency. The AD9783 was selected for the design because of more convenient digital interface.

Table 3 VM chips comparison.

Part Number	Bandwidth [MHz]	Noise Floor [dBm/Hz]	Uncalibrated Carrier Suppresion [dBc]	Uncalibrated Sideband Suppresion [dBc]	P1dB
TRF370317	400 – 4000	-163	40	45	12
TRF370417	50 – 6000	-162	38	50	12
TRF370315	350 – 4000	-163	40	40	9
TRF370333	350 – 4000	-163	40	40	9
HMC1097	100 – 6000	-160	40	40	11
LTC5598	5 – 1600	-165	55	50	8.5
LTC5588-1	200 – 6000	-160	45	53	8.6

All considered VM chips offer similar performance and are footprint compatible. TRF370417 was selected for the design, because of the widest bandwidth.

3.2.2 Fast ADC Channels

Two dual, fast ADCs are used in the module. Because of the limited number of the LVDS pairs on the FMC connector it was decided to use two kinds of ADCs, one with a parallel LVDS interface and one with a JESD204B interface.

The clock frequency used in the design is 117,3 MHz. In order to avoid operation of the ADC close to its limit, the ADC used in the design shall have sampling frequency higher than 150 MSPS. For the best performance 16-bit ADCs shall be selected.

The comparison of the ADCs from various manufacturers is presented in Table 4.

Table 4 Comparison of ADCs with parallel LVDS interface.

Part Number	**Sampling Rate [MSPS]**	**SNR @ 70 MHz [dBFS]**	**SINAD @ 70 MHz [dBFS]**	**ENOB @ 70 MHz**	**SFDR @ 70 MHz [dBFS]**	**Apperture jitter [fs]**
AD9652	310	75	74.6	12.1	87	100
ADS42LB69	250	75.5	74.2	12 (170 MHz)	90	85
ADC16DV160	160	76	75	-----	95	80
ADS42JB69	250	75.6	75.3	12 (170 MHz)	88	85

The ADCs chosen for the design are ADS42LB69 with a parallel LVDS interface and ADS42JB69 with a JESD204B interface.

3.2.3 Reference Signal Distribution

The reference signal is distributed to 7 vector modulator channels and a clock distribution circuit. For the best performance, the power delivered to the input of the vector modulator should be around 10 dBm. To improve the performance at low input power levels, a variable attenuator and an amplifier are added. When high power level delivered to the board, the amplifier and the attenuator can be bypassed. 7 SBTC-2-10L+ 2-way splitters are used, because their total power loss is smaller than the power loss of avaiable 8-way splitters.

The block diagram of the reference signal distribution is presented in Figure 7.

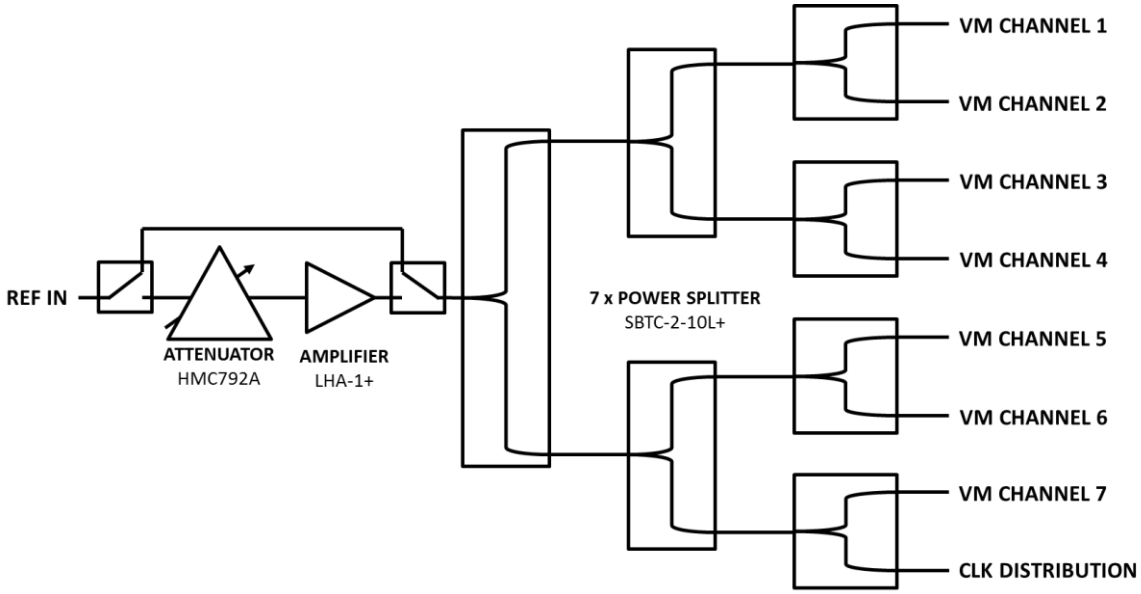

Figure 7 Block diagram of the reference signal distribution circuit.

3.2.4 Clock Distribution

The clock distribution circuit delivers clock signals to all data converters, FPGA and FMC connectors. This circuit is split into two parts:

- DAC clock distribution,
- ADC clock distribution.

Both parts are realized using LMK04808 clock distribution chip from Texas Instruments. Two clock inputs are provided, so independent clocks for DAC and ADCs can be used. The LMK04808 has integrated PLL with VCO. It can generate additional clock signal from the reference signal.

The block diagram of the clock distribution circuit is shown in Figure 8.

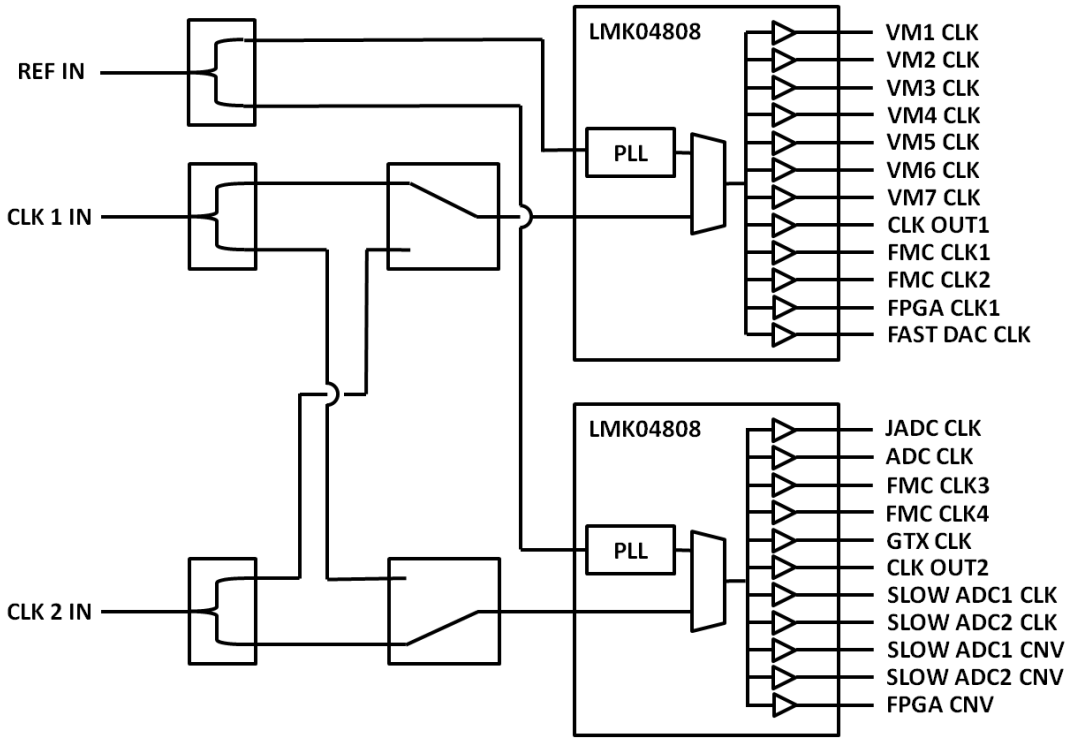

Figure 8 Block diagram of the clock distribution circuit.

3.2.5 Power Supply

In order to achieve the best performance, the power supply section of the module needs to be designed carefully. To lower the overall power consumption following approach is proposed:

- for analog circuits: a low ripple DC-DC converter followed by a low noise LDOs,
- for digital circuits: only a low ripple DC-DC converter.

All power sections of the board can be switched off, except for the DC-DC converters powering the digital section. The power tree proposed for the design is presented in Figure 8.

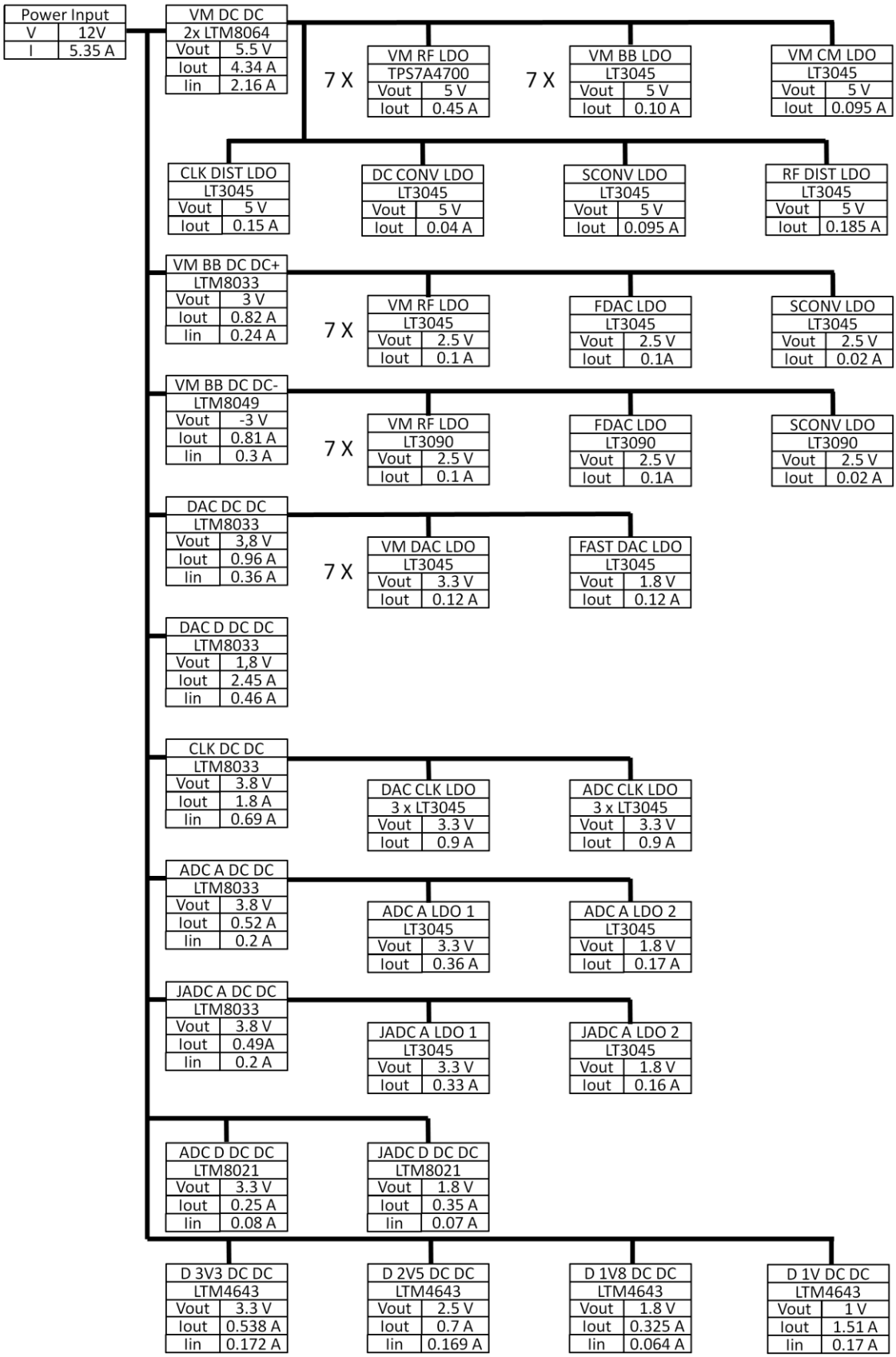

Figure 9 Power tree proposed for the Data Converters Module

3.2.6 Cooling

This module dissipates around 65W of power, so additional cooling solution must be implemented. The power is dissipated by many small elements placed around the board it, therefore it is impossible to place heat sinks on all devices. It was decided to use several BGA heat sinks connected directly to the board ground plane. ATS-1040-C3-R0 heat sink was selected. It is presented in Figure 10.

Figure 10 Photo of ATS-1040-C3-R0 heat sink.
Source: https://www.digikey.com/products/en?keywords=ATS1406-ND

In order to verify the performance of this solution a test board with 9 heat sources, temperature sensors and mentioned heat sink was designed. The size of the board is 10 x 10 cm. The photo of the board is presented in Figure 11.

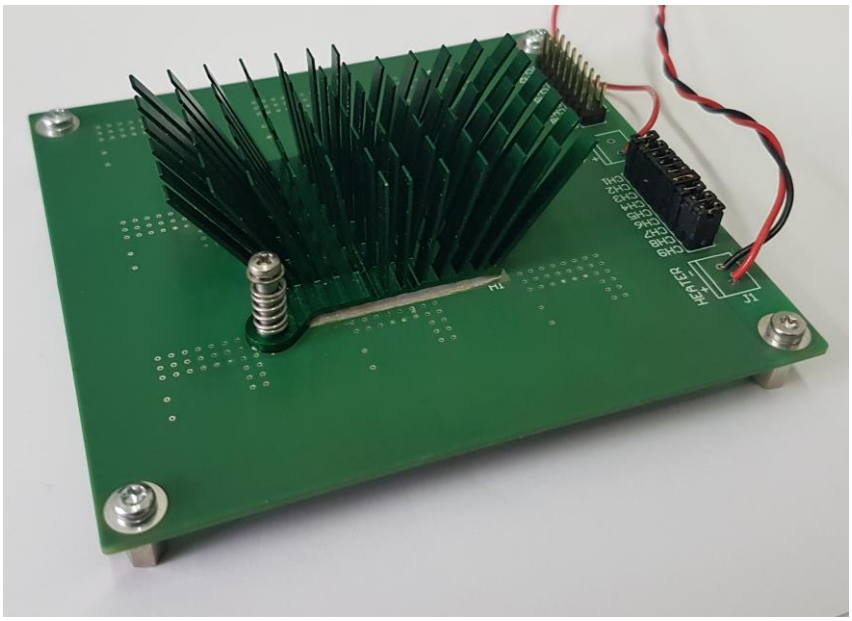

Figure 11 Photo of the cooling test board.

Four different scenarios were tested:

- board with no heatsink and no forced airflow,
- board with no heatsink and forced airflow,
- board with heatsink and no forced airflow,
- board with heatsink and forced airflow,

The airflow was generated by Everflow R128025DU fan, placed 15 cm from the edge of the board. According to the data provided by the manufacturer the air flow through the fan should be around 47.5 CFM. The result of the measurements are presented in Table 5.

Table 5 The results of the cooling measurements.

Power dissipated	**No heatsink, no forced airflow**	**No heatsink, forced airflow**	**Heatsink, no forced airflow**	**Heatsink, forced airflow**
0W	23,9 °C	23,9 °C	23,8 °C	23,8 °C
10W	85,2 °C	-	60,6 °C	-
25W	-	74,6 °C	-	50,8 °C
Thermal resistance	6,13 °C/W	2,03 °C/W	3,68 °C/W	1,08 °C/W

The expected size of the board is around 20 x 30 cm. Together with 6 heat sinks and power dissipation of around 65 W, we can expect the temperature raise of around 40 °C with no forced airflow. In case of forced airflow the temperature raise is expected to drop to around 12 °C. This solution is then suitable for this module and should protect it from overheating even without forced airflow.

To additionally protect the board from overheating temperature sensors are placed around the module. In case of too high temperature detection the power of the analog circuits will be automatically switched off.

3.3 Down-converter Module

This module is equipped with 2 down-converter channels. Each channel consist of:

- digitally controlled attenuator,
- down-converting mixer,
- output amplifier,
- low pass filters.

In addition the power level of the LO signal can be controlled by a programmable attenuator.

The block diagram of the Down-Converter Module is presented in Figure 12.

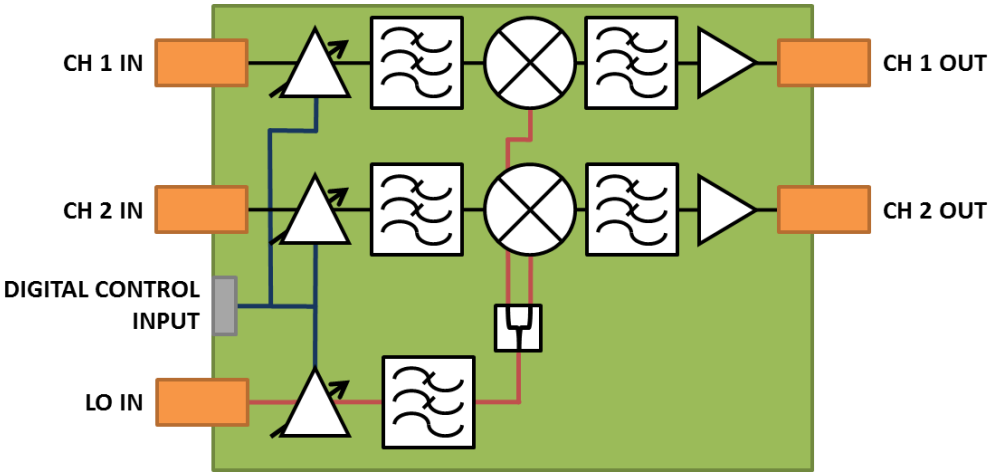

Figure 12 The block diagram of the down-converter module.

3.4 LO Generation Module

The module generates 2 LO signals and 4 CLK signals. It uses the same direct analog generation scheme as the one used in the LO RTM module for ESS LLRF. The block diagram of the LO Generation Module is presented in Figure 13.

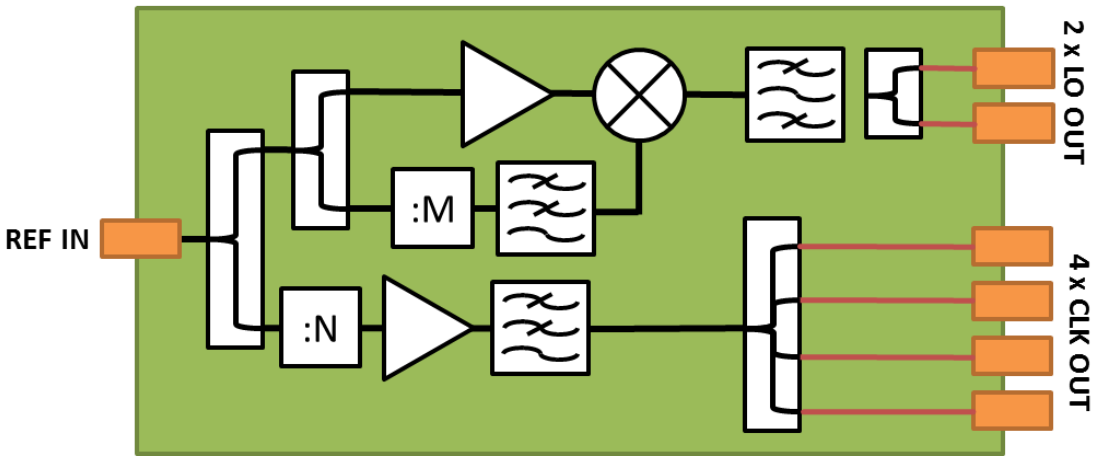

Figure 13 The block diagram of the LO generation module.

Expected phase noise performance of the module was measured using test setup constructed from evaluation boards. The measurement results are presented in Figures 14 and 15.

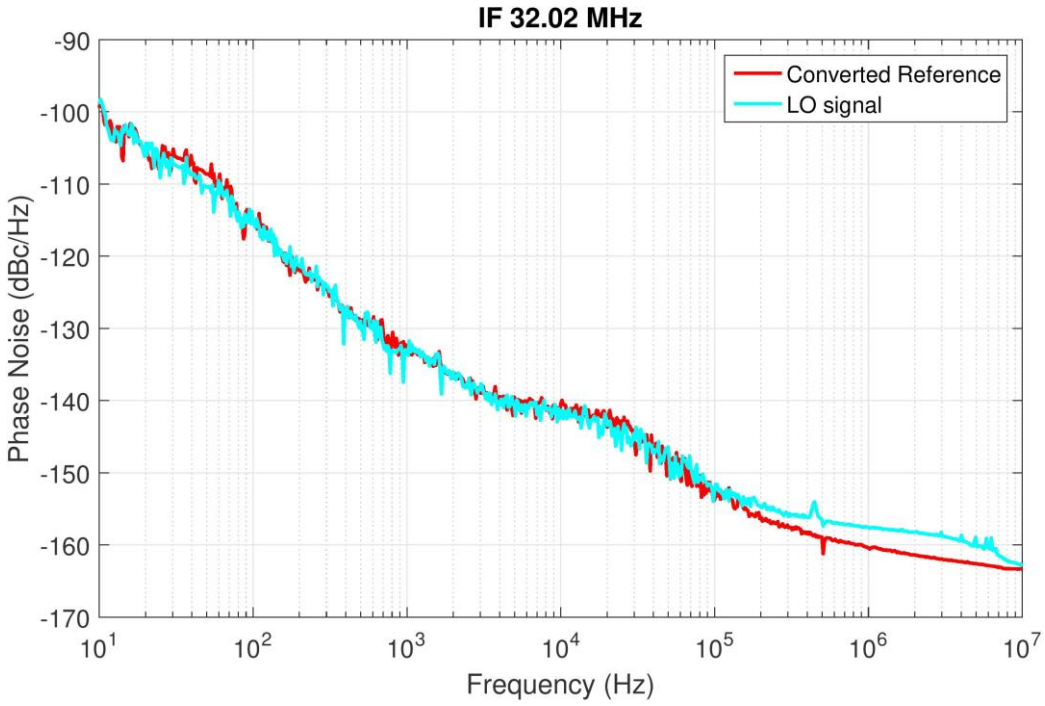

Figure 14 Expected phase noise spectrum of the LO signal.

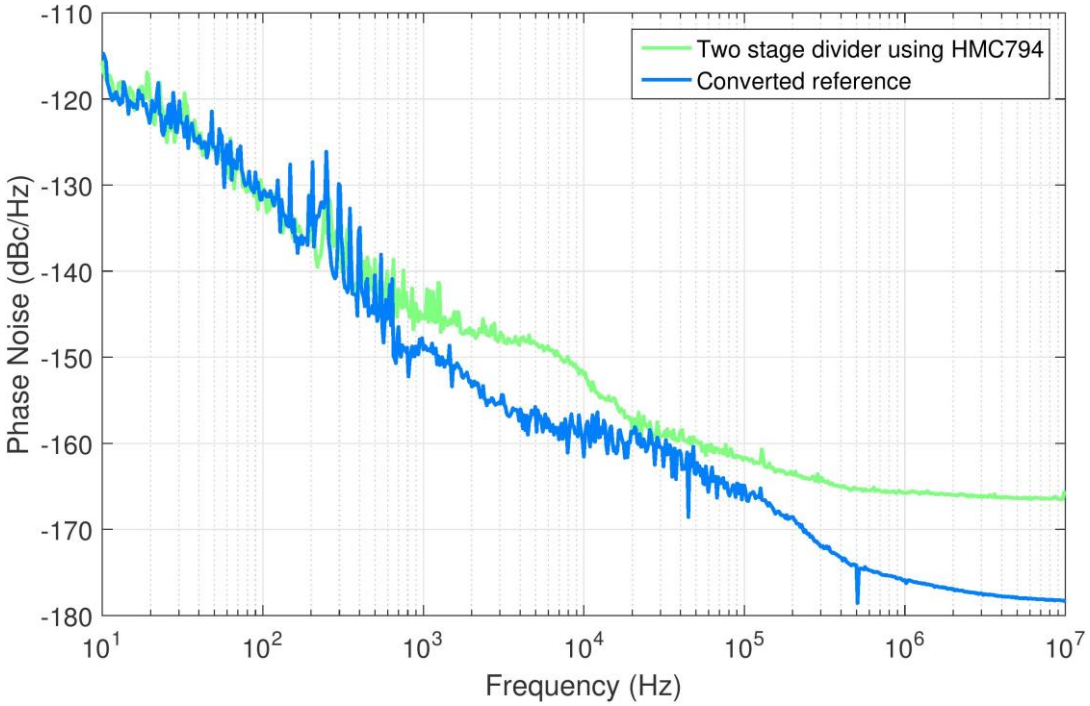

Figure 15 Expected phase noise spectrum of the clock signal.

3.5 Reference Generation Module

This module is generates and distributes RF reference signal. This signal is fed to:

- FMC module,
- Down-converter module,
- LO generation module,
- front panel.

The module supports two modes of operation:

- distribution of external reference signal,
- distribution of locally generated reference signal.

The reference signal generation circuit is based on Texas Instruments LMX2592 PLL with an integrated VCO. The reference signal for this PLL will be generated by a 32 MHz crystal oscillator. In case of insufficient performance of the LMX2592 PLL, a possibility of connecting an external 1:1 PLL is provided.

The block diagram of the Reference Generation Module is presented in Figure 16.

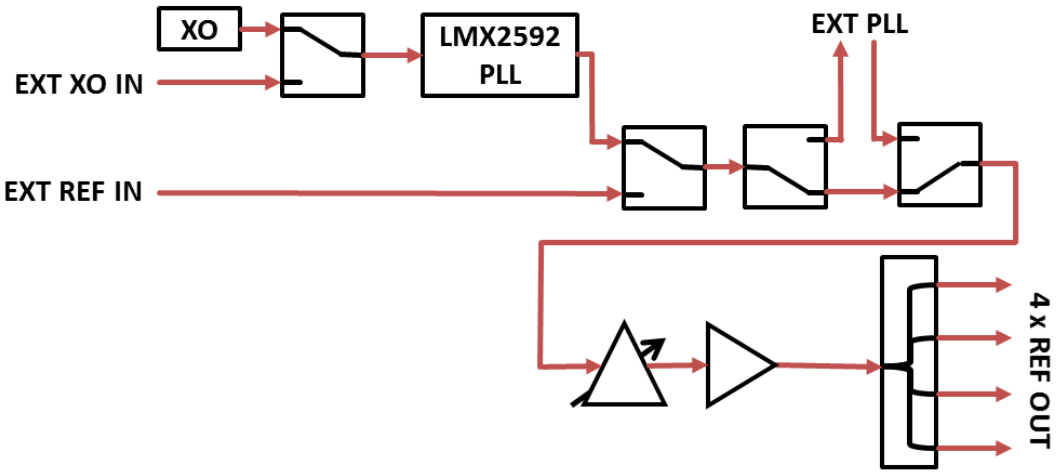

Figure 16 The block diagram of the Reference Generation Module.

3.5.1 LMX2592 Measurements

The phase noise performance of the LMX2592 was evaluated. The following equipment was used for measurements:

- Texas Instruments LMX2592 evaluation board,
- Agilent E5502B Signal Source Analyzer,
- Agilent E8257D RF Generator

The photo of the test setup is presented in Figure 17.

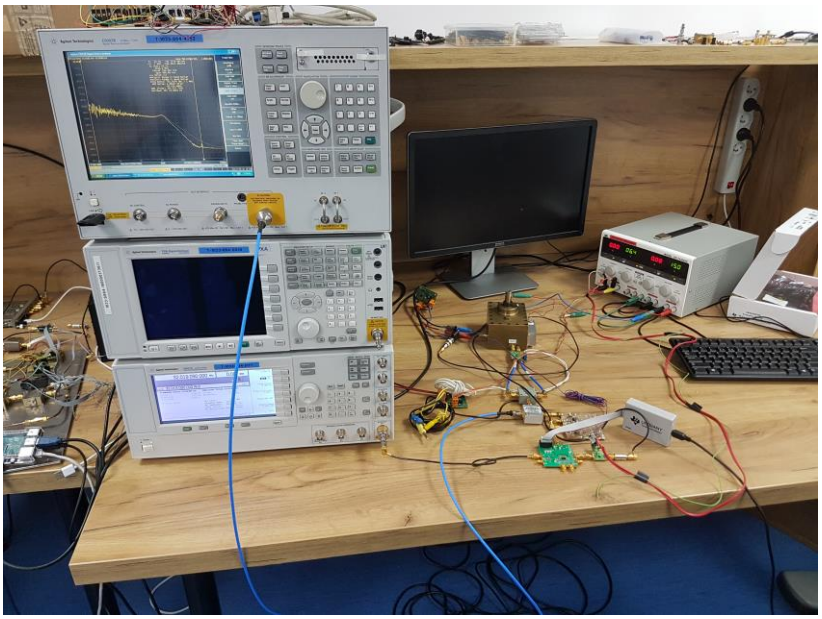

Figure 17 The photo of the LMX2592 test setup.

The results of the measurements are shown in Figure 18.

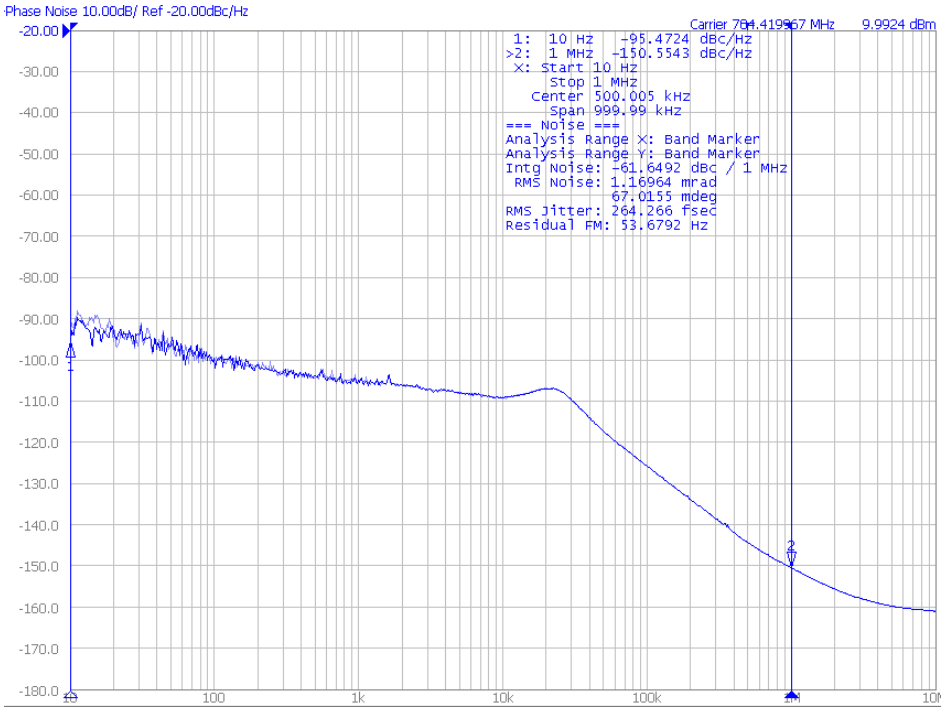

Figure 18 Phase noise spectrum of the signal generated by LMX2592.

3.5.2 External PLL

The External PLL Module is a custom low noise PLL with 2.816 GHz dielectric oscillator. This PLL will generate the output signal of the same frequency as the input signal, but with improved far from carrier phase noise.

The block diagram of this module is presented in Figure 19.

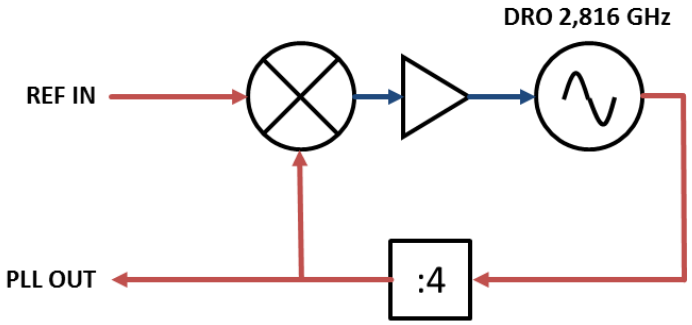

Figure 19 Block diagram of the External PLL Module.

The performance of this module was measured using the same test setup as for the LMX2592 PLL measurements. The results of the phase noise measurement are presented in Figure 20.

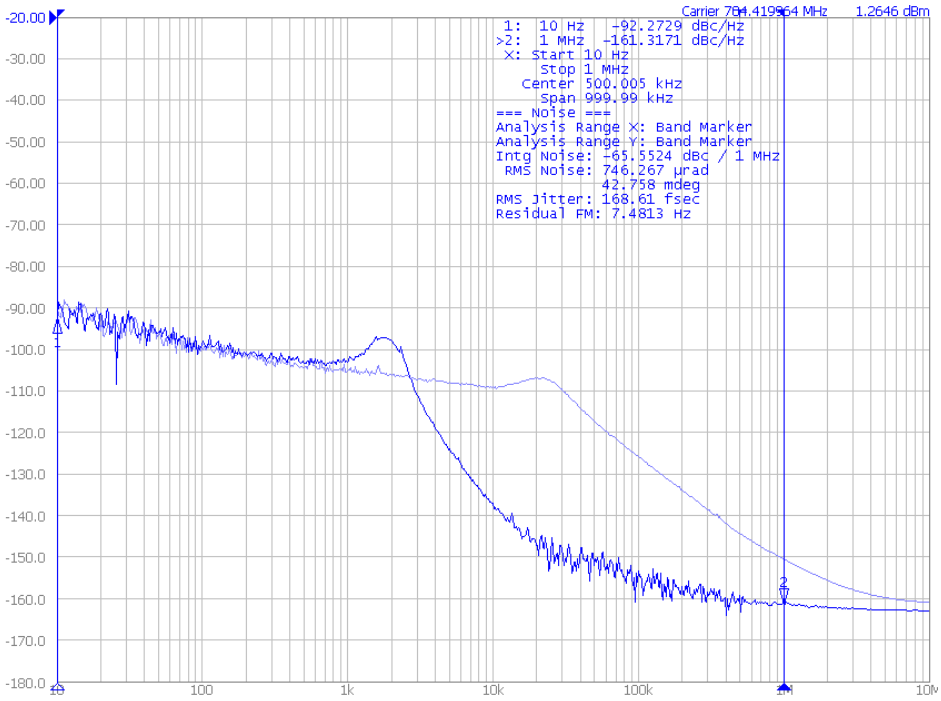

Figure 20 Phase noise spectrum of the custom PLL driven from the signal generated by LMX2592.

3.6 Power Supply Module

This module delivers power to all other modules used in the Cavity Simulator. It is powered from an external 24V AC-DC power supply. The low-noise DC-DC converters lower the input voltage to +12V that is used to power the remaining modules used in the Cavity Simulator. In total 3 DC-DC converters are present: 1 for FPGA Processing Module, 1 for Data Converters Module and 1 for all remaining modules.

Each output is equipped with an individual power switch and current monitoring. In case of over-current detection the output is switched off.
This module is also equipped with a frontend to control the speed of up to 6 fans.
The block diagram of the power supply module is presented in Figure 21.

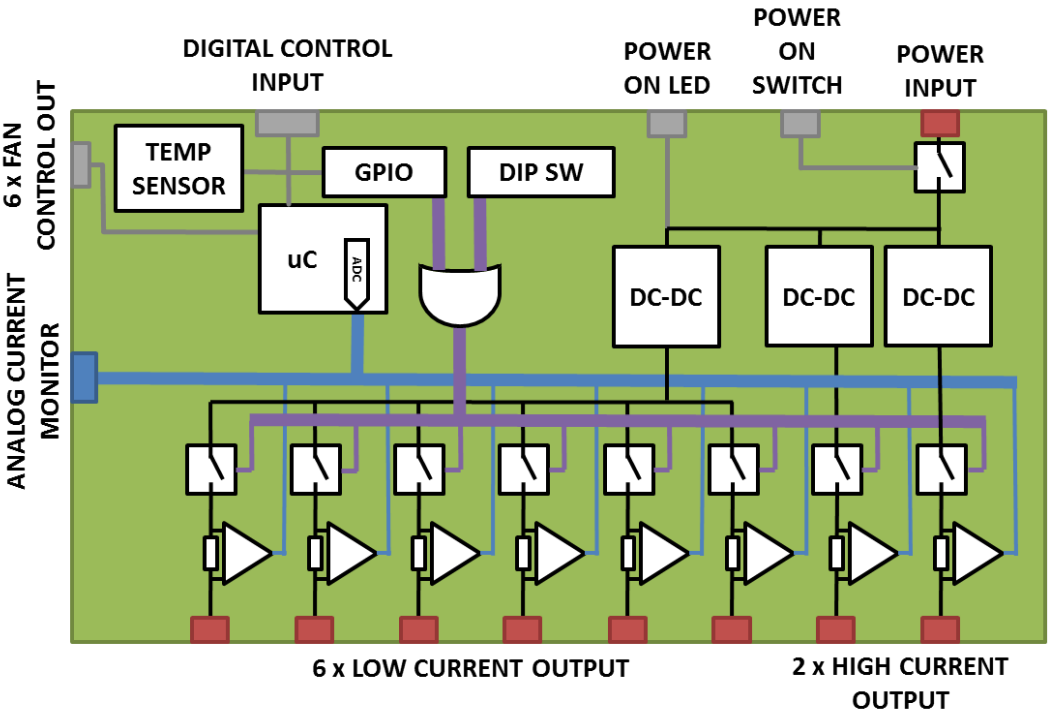

Figure 21 The block diagram of the Power Supply Module.

This module is equipped with a STM32 family micro-controller. It is responsible for constant current monitoring and the control of the fans. It is also used for correct initialization of the whole Cavity Simulator.

3.6.1 AC-DC Converter

The AC-DC Converter changes the 230 V AC power grid voltage to 24V DC, that can later power the Power Supply Module. A wide selection of such AC-DC converters is available on the market.

The estimated power consumption of the Cavity Simulator is 200 W. To guarantee stable operation it was decided to use a power supply with maximum output power of at least 500W. The TDK-Lambda GWS-500-24 power supply was selected. It is presented in Figure 22.

Figure 22 The photo of the TDK-Lambda GWS-500-24 power supply.

4 FIRMWARE AND SOFTWARE

Two FPGAs are used in the Cavity Simulator:

- Xilinx Kintex Ultrascale in the FPGA Processing Module,
- Xilinx Artix 7 in the Data Converters Module.

In this section concepts for firmware for both FPGAs are described.

4.1 Firmware for the FPGA Processing Module

The firmware for the FPGA Processing Module is responsible for:

- communication with a PC,
- gathering data from ADCs,
- sending data to vector modulators,
- data acquisition,
- digital signal processing for cavity simulation.

The main part of the firmware is the simulation model. It requires the RF signal data in IQ format, therefore the data coming from ADCs has to be first IQ demodulated. The first part of the simulation model is the amplifier model. It generates the amplifier's forward and reflected signals. The forward signal is then fed to Cavity model which generates cavity forward, reflected and pickup signals. All this signals are send to DACs, that generate the I and Q analog signals for vector modulators. Each output can be delayed and rotated individually.

For proper simulation the amplifier model require signal from a power supply modulator. This signal is generated inside the firmware and is fed to the model and to two DACs that generate analog output signals.

The cavity model is fed with the beam current and detuning calculation signals. The beam current signal is generated in the firmware based on the phase of the reference signal. The detuning calculation is based on the information from cavity and a piezo model. The piezo model acquire data from two ADCs and generates the output signal proportional to the detuning of the cavity.

To synchronize the Cavity Simulation with LLRF control system synchronization signal is required. It can be generated locally or external signal can be used. This signal is fed to the amplifier modulator and data acquisition.

For the purpose of testing the Cavity Simulator, a simple LLRF controller and arbitrary waveform generator are provided. This tools can be used to verify the proper operation of the device and will simplify firmware development.

To communicate with the controlling PC a Xilinx MicroBlaze softcore microprocessor is used. It is responsible for the interpretation of the control commands sent to the device through the Ethernet, setting the parameters of the simulation and readout of the data recorded by the data acquisition.

A simplified block diagram of the firmware for the FPGA Processing Module is presented in Figure 23.

4.2 Firmware for the Data Converters Module

The firmware for the Data Converters Module is responsible for:

- communication with other modules,
- forwarding data from slow ADCs,
- forwarding data to DACs,
- configuration of all modules,
- digital signal processing for cavity modeling.

The firmware for the Data Converter Module consist of the following blocks:

- 2 I2C controllers,
- SPI controller,
- power and temperature monitoring,
- 2 DDR transmitters.
- 4 DDR receivers.

Two I2C controllers are used. First is responsible for configuration of all devices used in the Data Converters Module with I2C interface. The second controller is connected to 1:8 I2C switch and communicates with all other modules used in the Cavity Simulator. The SPI controller is used to configure the devices with SPI interface. All these controllers can be interfaced from the FPGA processing module.

The power and temperature monitoring communicates with the I2C temperature sensors and in case of over temperature condition detection whole module is turned off. This part of firmware is also responsible for the power sequencing of all devices used in the module.

To minimize the number of lanes needed for transmission from the ADC and to DACs the DDR transceivers are used. This way, two channel data can be easily transmitted with only one data lane.

A simplified block diagram of the firmware for the FPGA used on the Data Converters Module is presented in Figure 24.

4.3 Control Software

Two software tools are provided to control the cavity simulator:

- Standalone application
- API for integration with other systems

4.3.1 Standalone application

The standalone application gives the user the ability to control the device through graphical user interface. The application will support Microsoft Windows and Linux x86 (Ubuntu) operating systems.

4.3.2 API

The Cavity Simulator API is a tool dedicated for integration in more complex system where automated control over the device is needed. This tool allows the user to easily integrate the device inside his test system.

The detailed description of this tools, including a list of methods and parameters, will be presented in future.

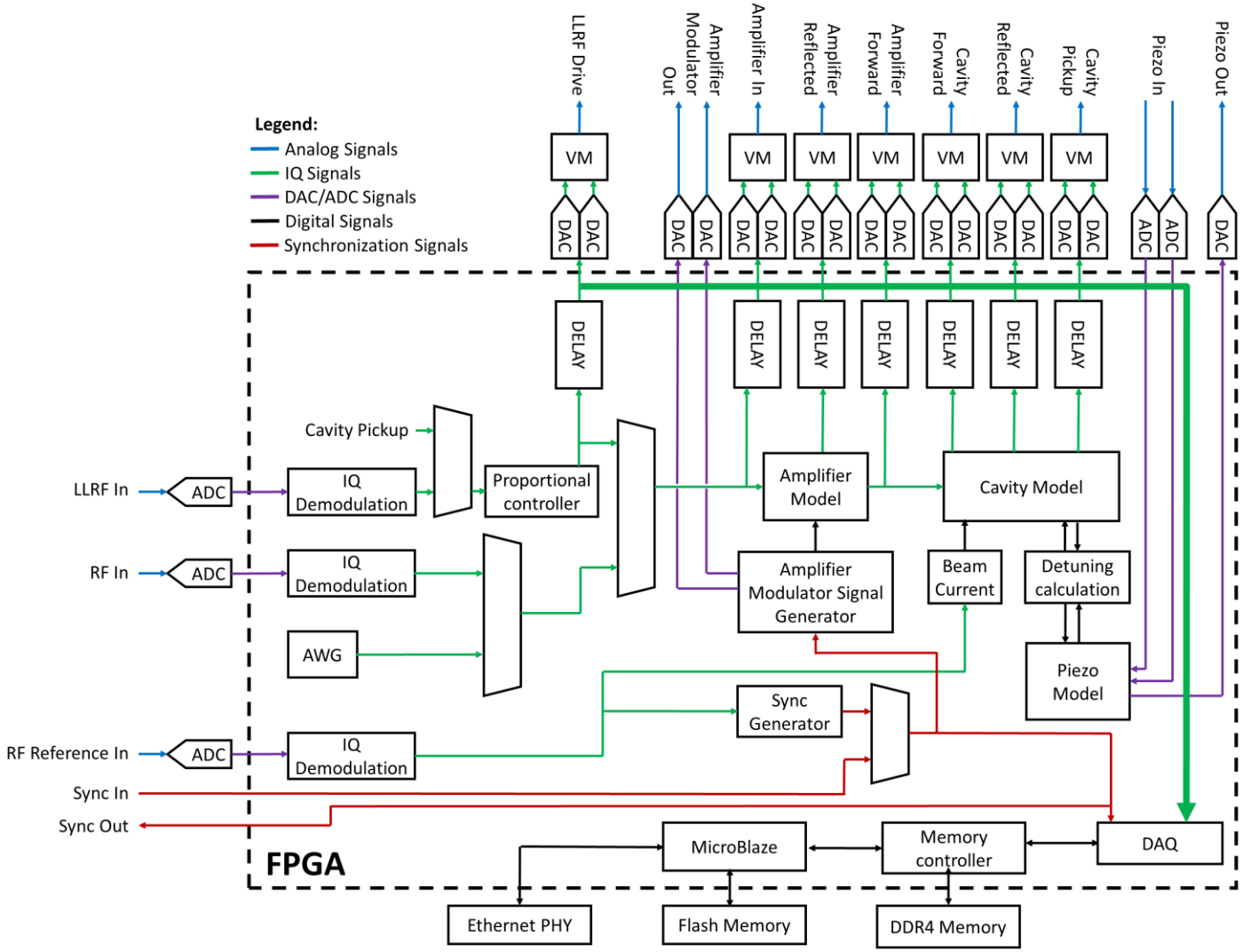

Figure 23 Block diagram of the firmware for the FPGA Processing Module.

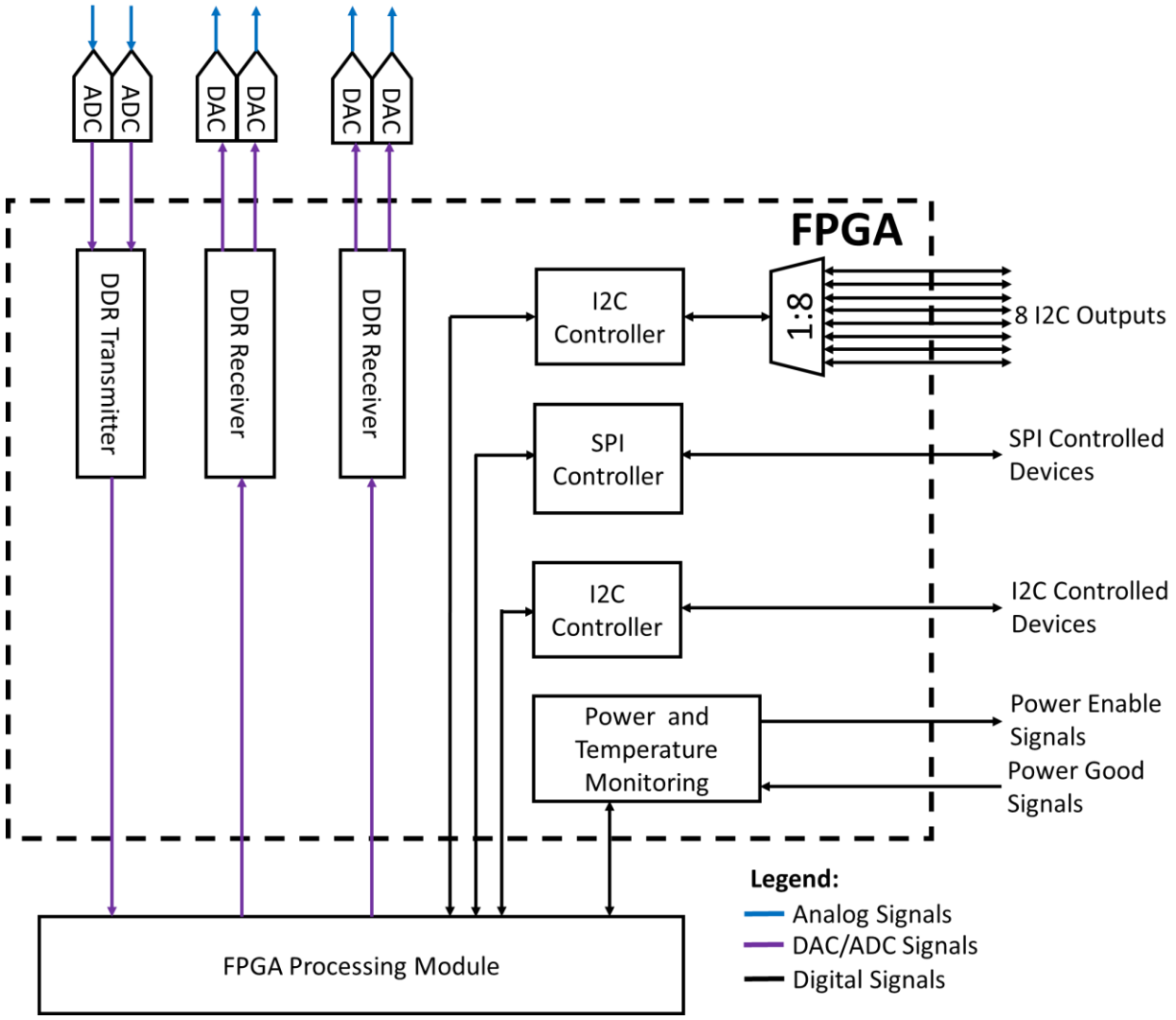

Figure 24 Block diagram of the firmware for the FPGA on the Data Converters Module.

5 DESIGN STATUS

Current actions focus on the hardware design. As for May 22nd 2017, 4 modules are being developed:

- Data Converters Module,
- LO Generation Module,
- Reference Generation Module,
- Power Supply Module.

5.1 Data Converters Module

The schematics of the module are complete and the PCB design is in progress. The 3D visualization of the current status of the PCB is shown in Figure 25.

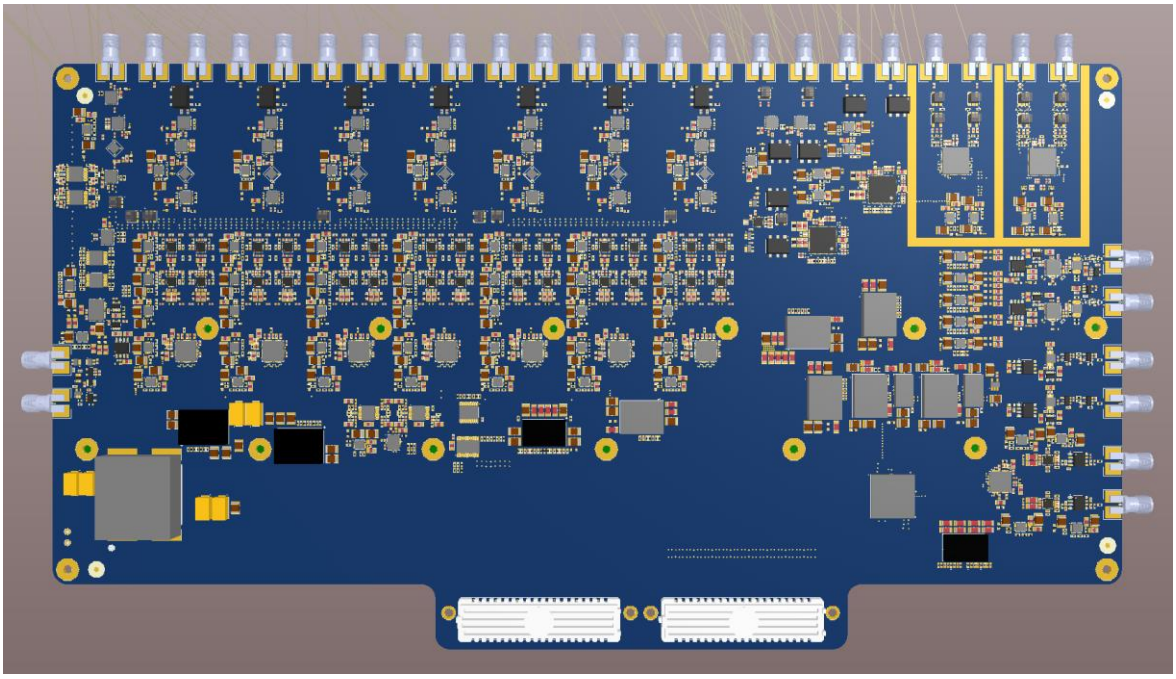

Figure 25 Visualisation of the Data Converters Module.

5.2 LO Generation Module

The LO Generation Module is almost complete and will be manufactured soon. The 3D visualization of the PCB is presented in Figure 26.

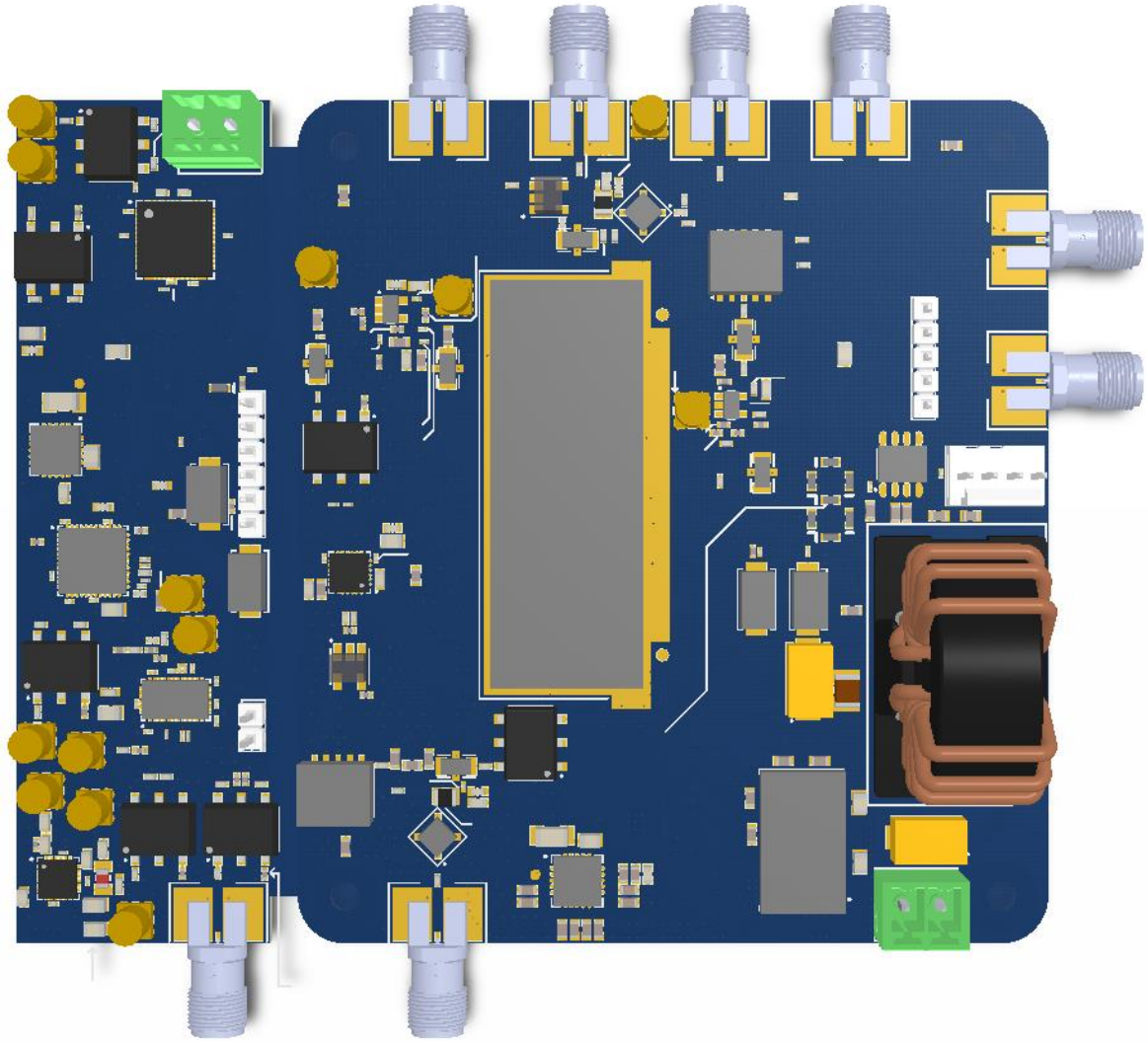

Figure 26 Visualization of the LO Generation Module.

5.3 Reference Generation Module

The measurement to verify the performance of the Reference Generation Module was performed. The schematics of the module are almost complete and PCB design should start soon.

5.4 Power Supply Module

Main components for the Power Supply Module were selected. The performance evaluation of the AC-DC and DC-DC converters is performed. When the measurements will be finished, the schematics design will begin.

6 CONCLUSIONS

In this document the concept of the design of the Cavity Simulator was presented. All internal modules designs were described, together with the concept of the FPGA firmware. The measurement results of the expected phase noise of the reference, LO and clock signals were presented.