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Description:	This document describes the design of the RTM Carrier designed for the tests of the ESS LLRF control system
Title:	**Preliminary Design Report for the RTM Carrier**

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1. Introction

1.1 Concept of the board

Architecture of the ESS LLRF system is based on the MTCA.4 architecture, where several devices (actually LO generation and Piezo control) will be implemented as a RTM units. To control those RTM devices, according to MTCA.4 standard, an AMC board - “RTM Carrier” is needed.

In the actual ESS LLRF system concept, the RTM devices will be the functional units dedicated to particular tasks, such as LO generation or piezo drive and control in technology independent way, and AMC boards shall provide FPGA device for data processing and communication. Such architecture allows to easily upgrade the FPGA devices by replacing AMC boards when used technology will become obsolete, without touching the functional RTMs.

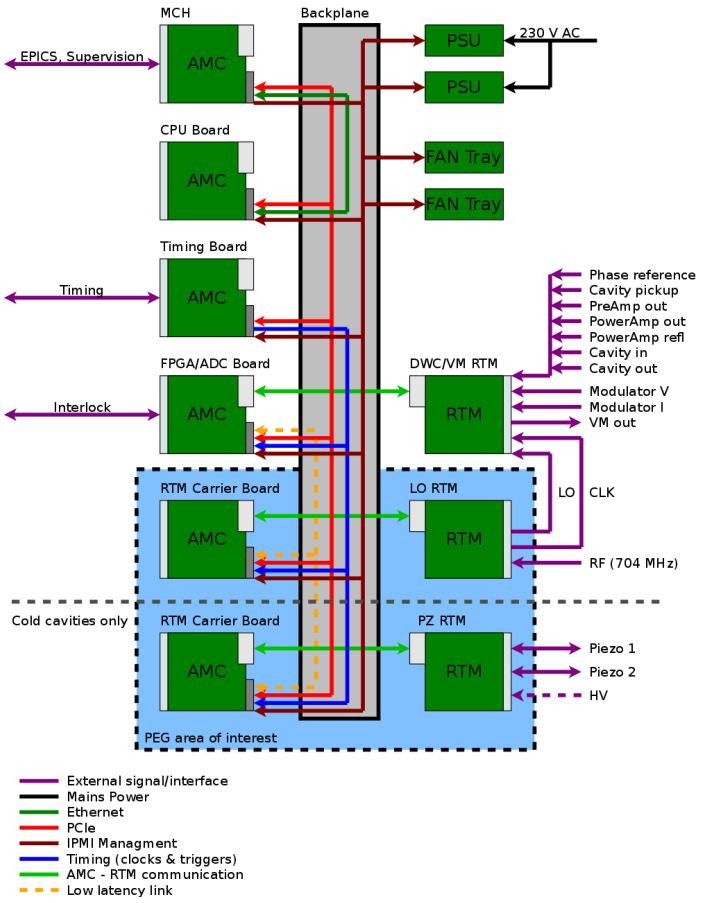

Figure 1.ESS LLRF System

Figure 1 shows where in the ESS LLRF system, RTM Carrier boards are used.

In the described concept, the AMC board for supporting the RTMs shall provide minimal functionality that allows RTMs to operate, and this is base of RTM Carrier device concept. The

general required functionality of the board is following:

- Communication with the RTM via ZONE 3
- Providing power to the RTM units
- Communication with the other devices using PCI-Express on the MTCA.4 backplane
- Data processing in the FPGA
- Fulfilling all the requirements for the AMC board defined in the MTCA.4 standard

At the time when architecture of the ESS LLRF system architecture was defined, there was no low cost MTCA.4 board fulfilling listed above goals. Considered alternative DAMC-FMC25 was expensive in comparison with needed functionality, because it had many features not needed in described application. Also it had unsupported in the latest development software (Xilinx Vivado) FPGA chip – Virtex-5.

Designing RTM carrier gives ability to create low cost device that fulfills exact needs of the ESS LLRF system, where estimated savings, in comparison with DAMC-FMC25, will easily cover the development cost.

1.2 Board interfaces

Described device shall have following interfaces:

- MTCA.4 ZONE 3 – I/O communication with the RTM
- MTCA.4 Backplane connectivity:
  - PCI-Express on AMC ports 4-7
  - Low-Latency Links for direct board-to-board communication, AMC ports 12-15
  - MLVDS clocks, triggers and interlocks on AMC ports 17-20
  - Telecom clocks (TCLKA, TCLKB)
  - MTCA.4 management signals (IPMB, Geographical Address, PS0#, PS1#, ENABLE#, AMC JTAG)
- Front panel:
  - External clock input
  - External; clock output
  - Diagnostic connectors
- Custom/on-baord interfaces:
  - Xilinx JTAG connector for FPGA programming
  - JTAG Connector for MMC MCU

1.3 RTM Carrier requirements

Based on description of the board concept above, the following requirements can be described:

1. Provide proper voltages (12V, 3.3V) for the RTM
    a) Provide as large as possible amount of power for the RTM (especially for piezo driver)
    b) Provide as high as possible current for specified time after start-up (in-rush current) for the RTM (especially for RTM)
2. Provide data transfer between MTCA.4 backplane and the RTM
    a) Zone 3 I/O configuration compatible with DESY D1.0 Recommendation
        i. All pins on the Zone 3 connector shall be connected to the FPGA
    b) Provide FPGA resources for implementing RTM-specific data exchange algorithms (SPI communication with the RTM, etc.)
    c) Provide access to RTM resources via the PCIe interface on the the MTCA backplane (ports 4-7)
    d) Provide connectivity between RTM and MTCA.4 extensions (MLVDS, ports 17-20)
        i. Provide clocks and triggers from the MTCA.4 backplane to the RTM
        ii. Provide interlock signals from the MTCA backplane to the RTM
        iii. Provide interlock signals from the RTM to the MTCA backplane
3. Provide MTCA management for the RTM
    a) Provide I2C connection from the MMC
    b) Provide support for accessing RTM management resources via I2C: (MTCA required LEDs, Hot-Swap handle, sensors, etc.)
    c) Represent the RTM resources (identification, sensors) in the IPMI records to the MCH
    d) Provide power control for the RTM
    e) Provide standard sensors on the AMC board
4. Provide clocks signals interconnect
    a) Provide MTCA clocks (TCLKA, TCLKB) for the RTM and for the FPGA
    b) Provide External clock source for the RTM and for the FPGA
    c) Provide on-board programmable clock generator for the RTM and for the FPGA
    d) Provide RTM clock for the FPGA
    e) Provide External clock output for monitoring selected on-board clock
    f) Provide local (non-programmable, always enabled) clock for the FPGA
    g) Provide dedicated clock infrastructure for PCIe interface
5. Provide diagnostics and support for out-of-crate board debugging
    a) Provide external power supply connector (12V, optionally 3.3V management power)

b) Dual channel USB-Serial interface to FPGA and MMC
   i. Provide possibility to supply the management power (3.3V MP from the USB connector)
c) LEDs on the front panel
d) JTAG interface for FPGA and for the RTM

6. Board should be low cost
   a) Price goal to be below 1000 Euro in mass production
7. Board should use latest low cost FPGA device

2. RTM Carrier hardware design

Based on conceptual design and requirements described above, the following hardware design presented in fig.2 has been created.

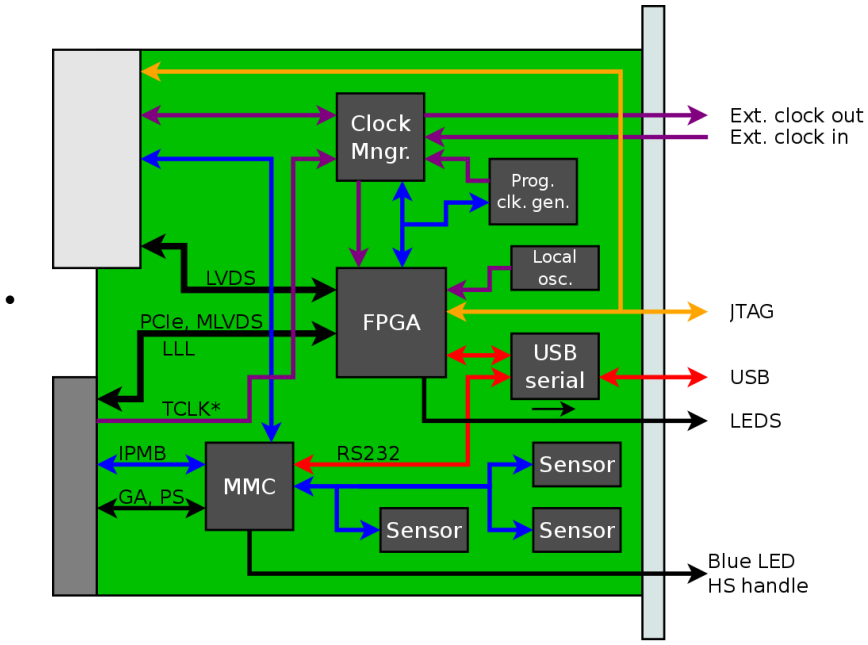

Figure 2. RTM Carrier Block Diagram

2.1 FPGA

The core component of the board is FPGA device. In this project, **Xilinx Artix-7** device has been chosen. This decision was made due to the following reasons:

- **Vendor**: Xilinx devices are used widely in accelerator control, as well as in other areas of experimental physics. Those devices was used in X-FEL LLRF system, they are proven to be reliable, and PEG member has experience with this technology – PCB design for Xilinx FPGA, software tools knowledge for FPGA programming, etc.
- **Gigabit transceivers** (MGT, RocketIO) – Providing support for PCI-Express and Low-Latency Links requires gigabit transceivers, because of this other FPGA families, such as

Spartan-7 can not be used.

- **Low Cost** – Artix-7 is a Xilinx low cost FPGA device with gigabit transceivers
- **Latest architecture** – Artix-7 is a part of Xilinx 7-th Generation FPGA devices (“7 Series”), and in contrast with 6-generation and older devices, it is supported by most recent Xilinx development tools – **Vivado**.

Artix-7 FPGA devices family contains several devices in different packages, where different devices are foot-print compatible. In the described project, **FGG484/FBG484** footprint for the FPGA has been chosen. This footprint allows assembly of the following devices:

- XC7A15T
- XC7A35T
- XC7A50T
- XC7A75T
- XC7A100T
- XC7A200T

Part Number	Logic Cells	Slices	CLB Flip-Flops	Total Block RAM (Kb)	DSP Slices	Max. single ended IOs (6.6 Gb/s GTPs)
XC7A15T	16,640	2,600	20,800	900	45	250 (4)
XC7A35T	33,280	5,200	41,600	1800	90	250 (4)
XC7A50T	52,160	8,150	65,200	2700	120	250 (4)
XC7A75T	75,520	11,800	94,400	3780	180	285 (4)
XC7A100T	101,440	15,850	126,800	4860	240	285 (4)
XC7A200T	215,360	33,650	269,200	13140	740	285 (4)

Table 1. Available FPGA resources

FPGA Configuration

FPGA configuration process will be controlled by the Module Managment Controller (MMC).

The following configuration modes are foreseen to be used:

- Master SPI – FPGA loads firmware from SPI flash by itself
- Slave Serial – MMC can disable SPI Flash ans push bitstream to FPGA
- JTAG – fail-safe configuration mode using external programming cable

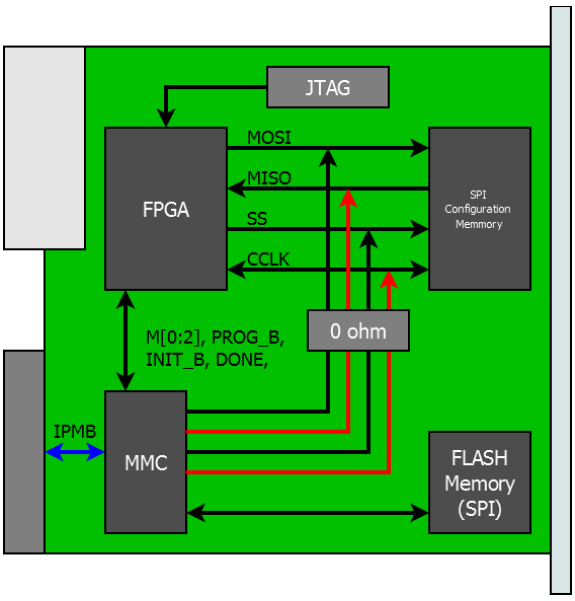

Figure 3. General FPGA configuration scheme

“Master SPI” and “Slave Serial” modes use the same configuration pins: CCLK and MOSI/D0. In Master SPI mode CCLK is driven by FPGA and MOSI/D0 by SPI flash memory, and in Slave Serial mode, both lines will be driven by MMC. To have two different configuration sources, (SPI Flash and MMC), mentioned lines are hard-wired on the PCB to all three devices (FPGA, MMC, SPI Flash). To make proposed solution working, MMC has to control the configuration process, which included also selecting proper configuration mode and enabling/disabling requested devices. MMC may disable SPI Flash from driving MOSI/D0 by selecting any FPGA configuration mode except SPI and BPI, in such case pulled-up SPI Flash Chip Select (FCS_B) becomes high-impedance. Also MMC can disable FPGA from driving CCLK by selecting any slave configuration mode. Disabling FPGA can also allow MMC to update the SPI flash.

Proposed solution use minimal resources (PCB routing) to achieve following goals:

- Allow FPGA to load bitstream directly from SPI flash memory (configuration mode preferred by Vendor)
- Allow FPGA to update by itself the SPI flash during runtime; this allows “remote firmware upgrade” using user data transfer interface – PCI-Express.
- Allow MMC to load bitstream directly to FPGA; MMC may handle several firmware revisions, and select which one shall be used. This also provides the “remote firmware update” via MMC feature
- Allow MMC to update SPI flash
- Allow MMC to readback the SPI flash

In case of unexpected problems, zero-ohm resistors has been place on the configuration lines, allowing selection SPI flash or MMC (slave serial) mode only.

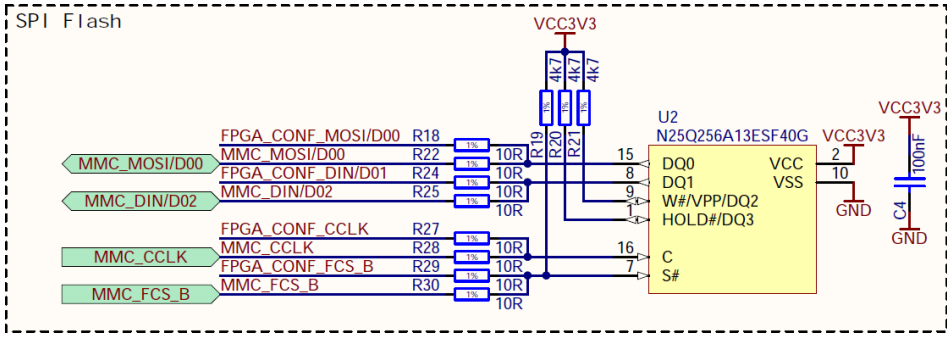

Figure 4. SPI configuration flash memory and signals routing

As a SPI flash memory **N25Q256A13ESF40G**, has been selected. This is commonly used memory for Xilinx FPGAs configuration, and this particular device allows to keep bitstream for biggest Artrix-7 supported by RTM Carrier. This memory is supported by both ISE and Vivado development tools, and it is compatible witch serial configuration modes of the 7-Series Xilinx FPGAs.

For development and in case of FPGA troubleshooting, JTAG configuration mode is provided. Describes desing has two JTAG slave devices:

- FPGA device
- RTM Interface

and two JTAG master interfaces:

- Xilinx JTAG Connector
- AMC JTAG interface

There JTAG slave devices can be connected in one chain, but in case when RTM device would be missing, JTAG chain would be broken, and non-functional. On the other hand, there are two master interfaces, and they could be also hard-wired together, as long as they do not operate in the same time - Xilinx JTAG connector could be used only in out-of-crate operation, because other way the board could be damaged.

Taking into account above considerations, the JTAG chain must be switchable. Electronic switching is discouraged here, because JTAG is last resort debugging interface, and it must simple and robust, because it is used to debug other components, and there is no resources to diagnose JTAG itself. Proposed solution is to use simple jumpers, which can be used to bypass selected slave devices in

the chain, and also select which master interface is controlling the chain. Figures 5a, 5b and 5c below presents JTAG switching jumpers concept.

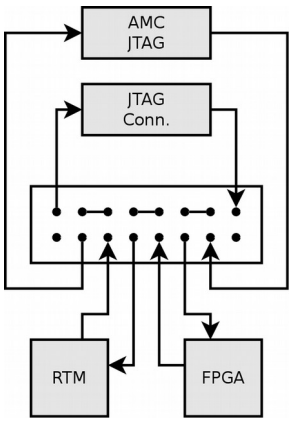

Figure 5a. General JTAG concept

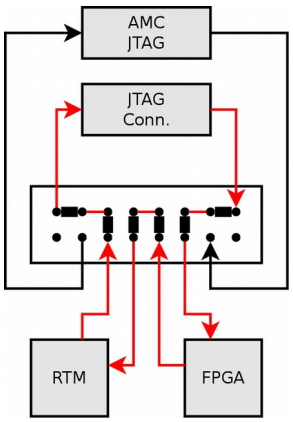

Figure 5b. All devices controlled from JTAG connector

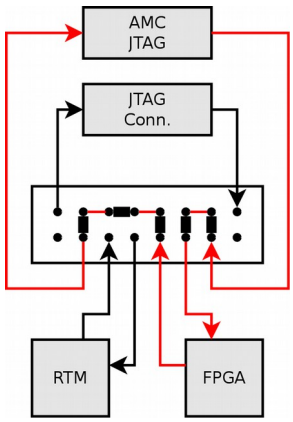

Figure 5c. FPGA controlled by AMC JTAG, RTM bypassed

2.2 Board interfaces

RTM Carrier has following interfaces:

PCI-Express

Selected FPGA devices family has 4 MGT interfaces, and due to requirement of having support for Low-Latency Links (LLL), not all MGT can be used for PCI-Express. As a compromise, 2 MGTs has been assigned for PCI-Express, and 2 for LLL, resulting in having PCI-Express x2 (Gen2) on the AMC ports 4 and 5.

Low-Latencty Links (LLL)

This interface is for fast board-to-board communication over the MTCA backplane. As it was mentioned above, 2 (of 4) MGTs has been assigned to LLL. Board to board communication has been foreseen on AMC ports 12-15. But to the limitation of MGT amount (2), all for ports are covered using two 2:1 switches, having 12 or 13 on one MGT, and 14 or 15 on another MGT. Communication parameters strictly depends on the FPGA configuration, and it must be compatible with other device in the crate.

Device chosen as a LLL switch is **AD8153ACPZ**, it is I2C controlled single mux/demux for gigabit links. Using these two switches allows to have all LLL connected to FPGA without soldering and desoldering zero-ohm resistors.

MTCA.4 Zone 3

This is interface for communication with RTMs, in described design zone 3 will be implemented according to DESY D1.0 recommendation. Zone 3 connector will be fully covered, providing 96 LVDS pairs and supporting clock signals.

MLVDS

This will provide general purpose clock, trigger or interlock signals on AMC ports 17-20. Each signal can operate in both direction, board can read or drive it on the MTCA backplane. For implementation of MLVDS bus, **DS91M040TSQE/NOPB** devices has been used, which was the cheapest quad MLVDS transceiver, which performance is compatible with MTCA standard.

Telecom clocks (TCLKA, TCLKB)

Board will use available on the MTCA backplane telecom clocks, TCLKA and TCLKB. These signals will be routed through the clocking cross-switches, that they can be delivered to RTM and FPGA.

MTCA.4 management signals

Except data transfer interfaces such as PCI-Express, board will support management signals available on the MTCA backplane, such as: IPMB, Geographical Address, PS0#, PS1#, ENABLE#, and AMC JTAG.

Clock input and output

Board will provide external TTL clock input and TTL clock output on the front panel.

Debug interfaces

For the purpose of board diagnostics, it will be equipped in several debug interfaces. Board will have dual USB-Serial connector, where one channel will be connected to the MMC system serial port, and other channel will be connected to the FPGA providing user the ability to create simple communication interface, which is not dependent on other infrastructure, especially MTCA. It can be useful for accessing FPGA in case of MTCA communication problems.

Except the USB transceiver for serial ports, there will be another micro USB connector on the front panel, which will be the USB interface of the MMC. This second interface may utilize the additional functionality availale in MMC, such as acting as dedicated USB device, like processor

programming interface, etc.

Except USB on front panel, board will have on PCB dedicated JTAG connectors, Xilinx JTAG connector for FPGA programming and supporting RTM JTAG chain (if any), and MMC MCU dedicated JTAG Connector.

2.3 Clock distribution

The clock distribution scheme is shown in the picture below

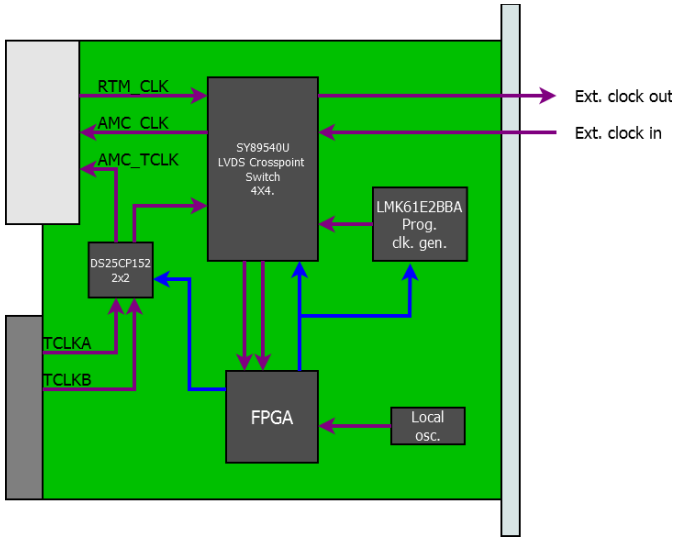

Figure 6. Clock distribution

The main task for the clock distribution is to support clocks foreseen in DESY D1.0 recommendation for the RTM – RTM clock input, RTM output clock and telecom clock to RTM.

Features of presented solution:

- Clock from RTM can be delivered to the FPGA and to front panel clock output
- External clock can be delivered to FPGA and to RTM
- Each of 4x4 cross-point switch input can be routed to 3 destinations: FPGA clock capable pin, external output via lvds-to-ttl buffer, or RTM clock input.
- Both telecom clocks can be delivered to FPGA and RTM via 2x2 cross-switch, but one signal cannot go to both receivers - TCLKA may go to RTM and TCLKB to FPGA (through cross-switch), or TCLKB may go to RTM and TCLKA to FPGA (through cross-switch)
- There is programmable clock generator, to have flexible clock source
- FPGA has local always enabled clock source, to bootstrap and configure the rest of clocking infrastructure, such as cross switch or programmable clock generator

External clocks are connected via lvds to TTL buffers (fig 7.).

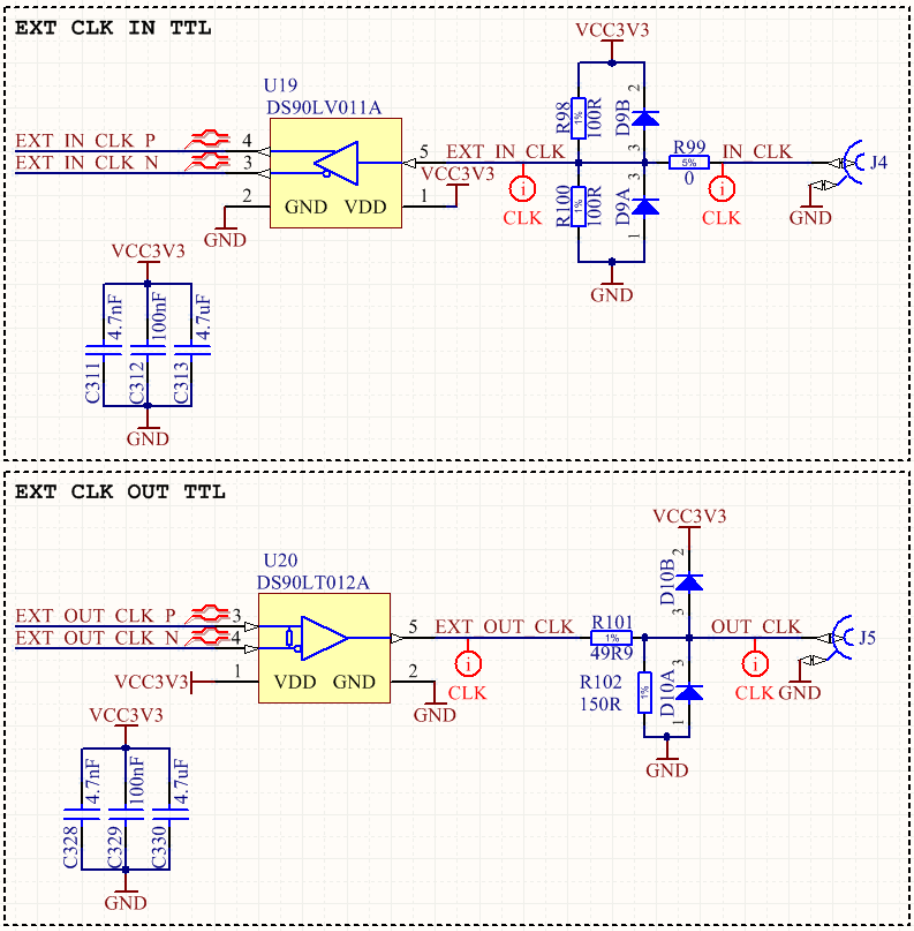

Figure 7. External Clock input and output

Main clock infrastructure components:

- **DS25CP152** - small footprint 2x2 LVDS cross-point switch designed for backplane acquiring signals, it has low additive jitter (max. up to 1 ps), which allows to use this device as clock switch
- **SY89540U** - small footprint 4x4 LVDS cross-point switch designed for high data rates with good channel-to-channel crosstalk performance, it has very low additive jitter (<0.1 ps), which allows to use this device as clock switch
- **LMK61E2BBA-SIAT** - programmable LVDS oscillator witch internal EEPROM. This device has internal power conditioning that provide excellent PSRR. Output frequency is in range from 10 MHz to 900 MHz, footprint is compatible with well known SI598, but this device is much cheaper and has better availability.
- **CFPS-39IB 50.0MHZ** - 50 MHz single ended locked frequency oscillator

2.4 Power distribution

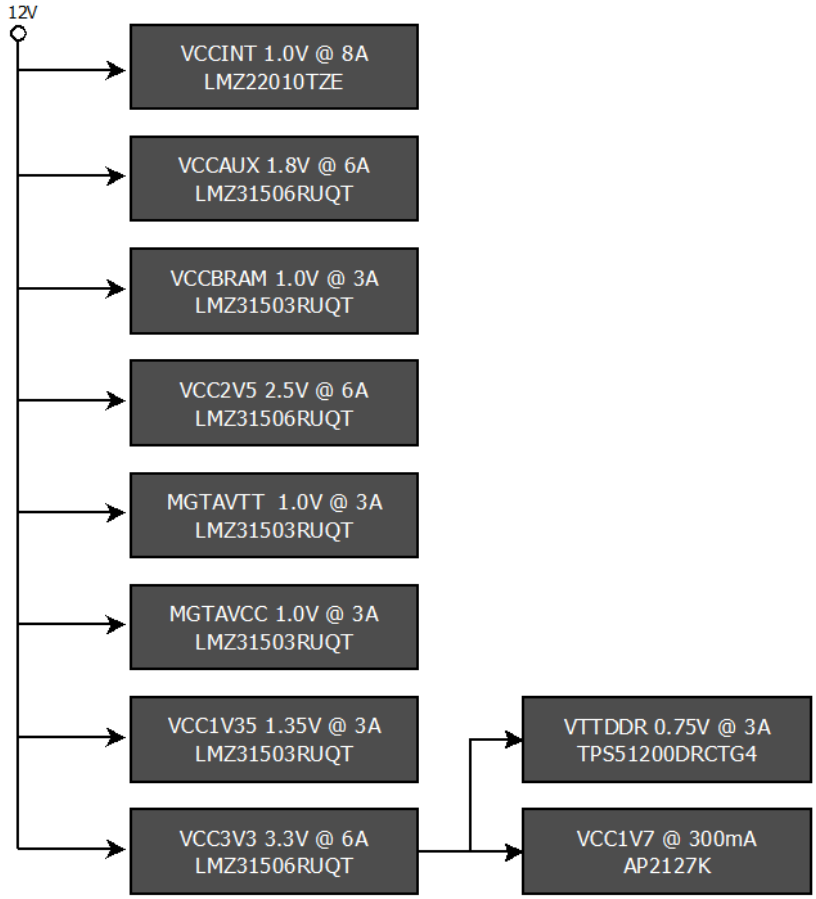

Figure 8. Power distribution scheme

For RTM Carrier, family of **SIMPLESwitcher** devices produced by Texas Instruments (TI) has been chosen. These are power modules with integrated shielded inductors that simplified PCB design and has low EMC emission. Three type of switchers, with output current of 8, 6 and 3 A, are used in design. Each specific FPGA power has own power supply that allows to implement maximum device resources utilization for biggest bga484 Artix-7 device. In addition, according to Xilinx documentation, MGT power supplies MGTAVTT and MGTAVCC should have own supplies.

FPGAs banks needs 3 types of supplies:

- 2V5 for LVDS_25 that are compatible with ZONE3 specification,
- 3V3 for bank connected to FPGAs peripherals, JTAG, and configuration memory
- 1V35 for bank connected to DDR3 memory, which allows to implement SSTL I/O standard needed for DDR memory communication

2.5 Managment

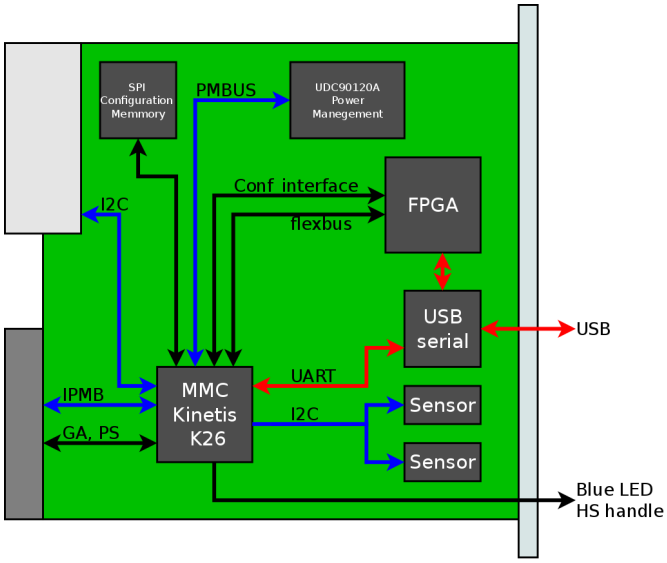

Figure 9. Board Managment

MTCA.4 standard requires extensive management resources, to achieve expected availability of the system. RTM Carrier will have MMC (Module Managment Controller) based on the Kinetis K-26 ARM microcontroller (**MK26FN2M0VLQ18**). This device has been chosen because it has four I2C interfaces, USB interface that allows to implement serial device, low current consumption, 256KB of RAM memory, and 2MB Flash memory. Also its possible to monitor on-board voltages using internal 16 bits ADC with build in voltage reference .

To simplify board operation, and avoid potential problems with MMC software controlled power start-up sequencing, a hardware power sequencer was placed on the board.

For RTM power control **TPS2459** device has been chosen. This is hot-plug controller for AMC, with digitally controlled inrush current and over-current protection. It has I2C interface, and it is possible to set current limits by software directly from MMC.

Except described devices, RTM carrier will be equipped in following management comonents:

- 2x I2C on-board temperature sensors **MAX6626RMTT**
- 1x I2C Temperature sensor **SA56004EDP** for readout of FPGA internal temperature sensor
- 1x EEPROM memory **24AA025E48T-I/OT** (typically for board identification data)
- 1x SPI Flash **N25Q256A13ESF40G**, foreseen for additional FPGA firmware storage

Board will have also USB-serial converter for communication with MMC serial port and/or FPGA.

2.6 Memory

RTM Carrier will have DDR3 memory of capacity 8Gb (1GB – one gigabyte). Memory will be implemented using single **MT41K1G8SN-125:A** device. It has internal organization 1Gx8, This memory has 8-bit data bus width, because this is only way to implement DDR3 interface utilizing single FPGA bank of Artix-7, but is not a problem since it can run with frequency of 300 MHz or more. Devices of this family is supported by latest Vivado design software, availability of this memory on the market has been confirmed.

3. Manufacturing and Verification

3.1 Description of planned test and measurements

The prototype units will be verified manually step-by-step against each implemented functionality, starting with electrical tests and finishing with communication with other components. Boards coming from series production will be tested in prepared RTM Carrier Teststand, where prepared tests will be performed as much as possible in automated way.

In both cases general board testing procedure shall include:

- Visual inspection, if there is no visible damage, if there is no missing components, if soldering looks good, if there are no external bodies that may cause short, etc. - if there is nothing suspicious
- Check with ohmmeter resistance between GND and major power nets (if there is no short)
- Power-on the board with the management power
- Check standby management power consumption on the power supply - if it is in the expected range;
- Check visually if LEDs expected to be active are illuminating.
- Check management power voltage level with multimeter
- Connect MMC programmer and load test firmware for MMC

- Measure management power consumption with loaded test firmware
- Check if result of MMC test firmware operation is as expected
- Power on the payload power;
- Check standby payload power consumption on the power supply - if it is in the expected range
- Check visually if LEDs expected to be active are illuminating.
- Check voltages derived from payload power if they are correct
- Connect the FPGA programmer and load test FPGA firmware
- Measure payload power consumption with loaded test firmware
- Check if result of FPGA test firmware operation is as expected
- Load operational MMC code on the board
- Power-off the board
- Place board in the MTCA crate
- Power on the crate
- Check if board was properly initialized
- Load test firmeare 2 to FPGA,
- Check connectivity with the CPU via PCIe
- Check connectivity with RTM
- Check the connectivity with test boards using LLL
- Check triggering and receiving signal via MLVDS bus

3.2 Standard used for engineering design, construction and verification of the RTM carrier.

RTM Carrier has been designed using Altium Designer software. Board does not use voltages over 12V, so it does not need to fulfill any special safety rules or regulations

3.3 Quality plan

Quality assurance of the RTM Carrier PCB project is based on:

- Continuous in parallel project (schismatics, PCB and libraries) review by other PCB design engineers, skillful in the used technologies, such as Xilinx FPGA.
- Drawing schematics using consistent conventions, such as naming convention, drawing

style, etc.

- Project files are stored in Subversion version control (SVN) system repository on the server. This helps in tracking changes, guarantees always safe “step-back” option to the latest correct design version, and provides a form of backup – project is places always in at least 2 places: on engineer’s computer (actual working copy) and on the server (last committed version with all history of changes). Regardless of this, server with SVN repository is backed-up independently by itself.

For keeping project

3.4 Schedule for procurement, manufacturing, testing and delivery.

Actual agreement defines following schedule concerning the RTM Carrier:

Phase	**Beginning**	**End**
Design of the first prototype	01-01-2017	01-08-2017
Design of the M-Beta prototype	01-10-2017	01-04-2018
Design of the H-Beta prototype	01-10-2019	01-04-2020

Table 2. Project schedule

3.5 Risk analysis

Table below presents potential risks and treatment plan

Event	**Cause**	**Impact**	**Treatment plan**
Late change of requirements	Insufficient data during requirements analysis	Late modules delivery.	Use as good as possible estimated requirements, if final ones are not available and build first prototype, expecting that for the next iteration(s), final requirements will be provided.
Delay in prototype design	Insufficient manpower	Delay in board delivery, increased cost	Increase manpower, find new employees

Prototype doesn't meet the requirements	Bad board concept	Delay in board delivery, increased cost	- Identify the reason of the problem - Correct the board concept and selected technology - Correct the prototype design - perform one more design iteration
Problems with components avaiablility	Long time between concept of the board and implementation/assembly	Delay in board delivery, increased cost	- Wait for components if unavailability is temporary - Try to order missing components, even if they are much more expensive - Try to find matching replacement components if possible - Consider which board functionality depends on the missing components and if this is acceptable - look for functional walk-around of the missing feature if possible - Redesign the board, to avoid using missing components
Broken components soldered on prototype	Problems with manufacturing technology, bad/broken components ordered, components stored/handled n the wrong way or Insufficient quality control.	Delay in board delivery, increased cost	- Identify affected units - Order required amount of good components - replace bad components
Broken components soldered on M-Beta version	Problems with manufacturing technology, bad/broken components ordered, components	Delay in board delivery, increased cost	- Identify affected units - Order required amount of good components - replace bad components - send repair team to ESS if affected units has been already shipped

	stored/handled n the wrong way or Insufficient quality control.		
Broken components soldered on H-Beta version	Problems with manufacturing technology, bad/broken components ordered, components stored/handled n the wrong way or Insufficient quality control.	Delay in board delivery, increased cost	- Identify affected units - Order required amount of good components - replace bad components - send repair team to ESS if affected units has been already shipped
Not detected design mistake in final version	- Insufficient quality control - error in test-stand, which covered described mistake - Error in board testing software, which covered this mistake	Increased cost of maintenance. Decreased performance. Reduced functionality.	- Identify mistake severity - Identify functionalities disabled by this mistake - Consider if this mistake could be acceptable (in contrast to full redesign and reproduction cost) - Perform board redesign and fabrication of all boards if there is no other way

Table 3. RTM Carrier project risks

3.6 Actual status and schedule

First prototype is at the stage of PCB design, schematics are finished – only minor changes are done while PCB layout is done. First prototype is going to be delivered on time.