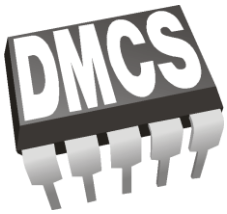

Description:	This document describes the design of Piezo Control Device (PCD) of Piezo Control System (PCS) for elliptical superconducting cavities of the ESS accelerator
Title:	**Preliminary Design Report for Piezo Control Device**

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Version:	1.0
Date:	2017.05.24

Revision Table

Revision	Date	Modification
1.0	2017.05.24	Final version provided for review
1.1		
1.2		
1.3		
1.4		
1.5		
1.6		
1.7		
1.8		
1.9		
2.0		

Table of Contents

1. Introduction

The European Spallation Source (ESS) accelerator operates in a pulsed mode with a repetition rate of 14 Hz. The Piezo Compensation System (PCS) is required for compensation of detuning of superconducting cavities caused by a Lorentz Force and microphonics. Piezo actuators are commonly used for applying force to the cavity (actuator mode) and measuring its mechanical stress (sensor mode).

The design of the Low Level RF (LLRF) system including PCS was developed by ESS prior to handling it to TUL-DMCS. According to the ESS, the PCS system should be designed using the state-of-the-art MicroTCA.4 technology. The PCS will consists of two modules:

- Digital Controller (DC) including processing power (FPGA) will be realised as double-width, full-size Advanced Mezzanine Cards (AMC).
- Piezo Control Device (PCD) including amplifier, DAC/ADC converters and high voltage power supply section will be designed as Rear Transition Module (RTM) compatible with MicroTCA.4 specification.

Both, the Digital Controller and Piezo Control Device will be installed in the MicroTCA.4 chassis of the LLRF control system. The PCS will share several common MicroTCA.4 components available in the chassis including CPU, MCH and PSM.

Lodz University of Technology, Department of Microelectronics and Computer Science (TUL-DMCS) was assigned to design, manufacture and install the Piezo Control Device hardware required for Lorentz force detuning of medium and high beta cavities[1].

National Centre for Nuclear Research (NCBJ) is responsible for the design of Digital Controller hardware realized in form of Advanced Mezzanine Card module. The low- and high-level software and FPGA firmware will developed and provided by ESS.

There are no commercially available piezo controller solutions matching PCS requirements, therefore a custom controller need to be designed. A prototype will be developed and tested prior to the mass production.

1.1. Functional specification

The Piezo Control Device should fulfil the following functional specification:

- Provide a control signal for piezo actuators of medium- and high-beta accelerator cavities operating in cryogenic temperatures.
- Measure cavity deformation using piezo device as sensor element.
- Support two independent channels with configurable mode of operation: piezo actuator or sensor.
- Provide a digital control and diagnostic interface of piezo driver via Zone 3 connector.
- Should be compatible with MicroTCA.4 standard.
- Provide health monitoring and diagnostics.
- Assure safe operation of piezo actuator.

[1] An attempt will be taken to design a powerful enough PCD module that could be used to control large capacitance piezo actuators assembled in spoke cavities.

1.2. Main ratings and parameters

Major requirements for PCD are presented in Table 1. The piezo actuators planned to be used in ESS accelerator are presented in Table 2, whereas the main parameters of the actuators are collected in Table 3 and Table 4. It is still unclear if spoke cavities will use piezo actuators manufactured by Noliac or the piezo stack composed of 3 PI actuators, see Table 4.

Table 1: Main requirements of PCD

Parameter	Value	Comments
Supported standards	MTCA.0, MTCA.4, AMC.0, AMC.2, IPMI 2.0	
Number of channels	2 bipolar channels with actuator/sensor mode	support piezo actuators listed in Table 3
Repetition Rate	14 Hz	pulse duration: max. 3.5 ms
Piezo capacitance	6.6 – 9.5 μF (room temperature)	high and medium beta cavities
Piezo supply voltage	±80 V (160 Vpp)	
Maximum actuator power	35 W per channel	
Controller Bandwidth	DC – 1 kHz	
Actuator excitation signal	Arbitrary waveform generation Sampling frequency: min. 1 MHz Number of samples: min. 30000 Resolution: 16-bits Output voltage range: ±80 V	
Piezo sensor	Sampling frequency: min. 1 MHz Number of samples: min. 30000 Resolution: 16-bits Input voltage range: ±1 V Input impedance: 10 kΩ	
Protection	Overcurrent Overvoltage Thermal protection of the driver Maximal control power of piezo	
Cable length for piezo connection	min. 30 m long, max. 45 m long	

Table 2: Supported piezo stacks

Cavity type	Piezo actuator type
Medium Beta cavities	Noliac NAC 2022 H30
High Beta cavities	Noliac NAC 2022 H30
Spoke cavities	Piezo #1: Noliac NAC2022-H90-A01 Piezo #2: PI PICMA P-888.91

Table 3. Medium- and high-beta piezo stack specification

Piezo type	Noliac NAC 2022 H30-C01
Dimensions	10 x 10 x 30 mm
Cell material	NCE51F
Number of cells	15
Capacitance (room temperature)	6.6 µF ±15%
Capacitance (cryo temperature, 20 K)	~ 2.2 µF[2]
Max. free stroke	49.5 µm
Blocking stroke in cryo temp.	3 µm
Blocking force max.	4200 N
Max. operating voltage	200 V
Max. operating temperature	150°C
Unloaded resonance frequency	248 kHz – 11 kHz
Comment	Tested at DMCS laboratory

Table 4. Spoke cavities piezo stacks specification

Piezo type	Noliac NAC2022-H90-A01	PI PICMA 2x P-888.90 and 1x P-888.50
Dimensions	10 x 10 x 90 mm	10 x 10 x 90 mm
Cell material	NCE51F	PIC252
Number of cells	45	
Capacitance (room temperature)	17.4 µF ±15%	32 µF ±20% (2x 13 µF + 1x 6 µF)
Capacitance (cryo temperature, 20 K)	~5.8 µF[2]	~10 µF[2]
Max. free stroke	145.2 µm	79 µm (2x32 µm + 15 µm)
Blocking stroke in cryo temp.	9 µm	TBD
Blocking force max.	4200 N	~3600 N
Max. operating voltage	200 V	-20 to 120 V
Max. operating temperature	150°C	150°C
Unloaded resonance frequency	248 kHz – 11 kHz	40/70 kHz
Comment	Suggested by INPO	Hybrid solution, suggested by INPO

[2] Estimated, do not use the estimated value for final design.

2. Piezo Compensation System topology

The PCD system will be designed using the state-of-the-art MicroTCA.4 technology. The PCD is designed as MicroTCA.4 module. It is connected to piezo-elements operating as sensors or actuators. The block diagram of the PCS is presented in Figure 1.

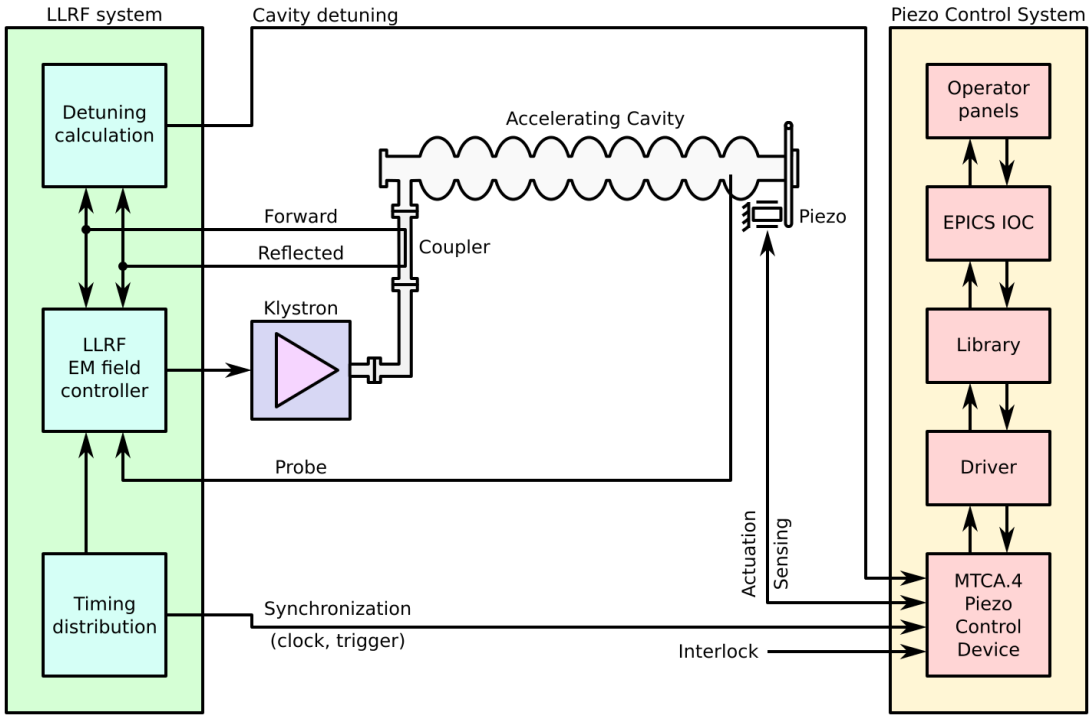

Figure 1: The Piezo Compensation System of ESS Accelerator

The PCD generates an arbitrary signal that is used to excite the piezo actuator. A cavity detuning signal is provided by LLRF controller module using MicroTCA.4 backplane. The PCS controller executes the feed-forward algorithms required for piezo control. The calculated excitation signal is amplified and then delivered to piezo actuator. The device monitors the amplifier temperature as well as the output voltage, current and power in order to assure a proper driving signal and therefore ensure long piezo lifetime.

It is foreseen that in regular operation both piezos are working as actuators. Nevertheless the PCD also allows compensating of the cavity detuning with single piezo and reading a signal from redundant piezo-element operating as a vibration sensor recording the spectrum of mechanical resonances. Each channel of PCD can be switched between actuator and sensor mode.

The PCS should be synchronized with LLRF control system. It should provide exception handling (interlock system) and piezo protection circuits.

The PCS system is connected to CPU via PCIe interface provided by MicroTCA.4 backplane. All parameters can be modified using EPICS panels.

3. Conceptual Design

The piezo control system consists of the CPU connected via PCIe interface to the piezo actuator controller. The piezo actuator controller is composed of the following modules:

- Digital Controller realised as AMC module including:
  - FPGA device with SDRAM, FLASH memories and PCIe interface.
  - Low latency connection to LLRF controller.
  - Interlock, trigger and clock inputs.
- Piezo Control Device RTM including:
  - Piezo driver with DAC circuit.
  - Piezo sensor with ADC circuit.
  - Piezo protection module.
  - Diagnostic controller.
  - Control logic.
  - Firmware upgrade module.

The block diagram of the piezo controller device connected to CPU is presented in Figure 2.

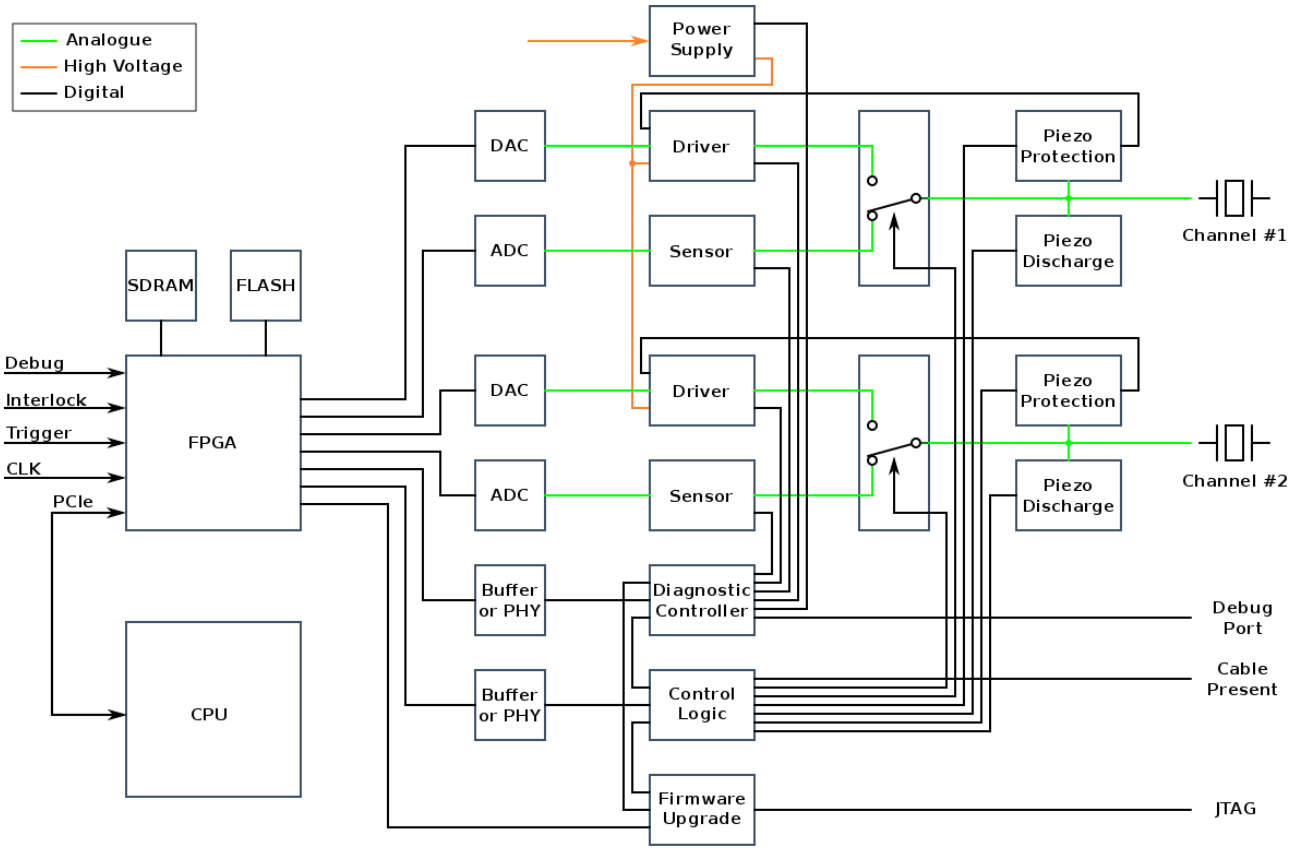

Figure 2 Block diagram of piezo control system.

The digital controller is based on Field Programmable Gate Array (FPGA) device and provide the resources required to implement a digital controller for piezo actuator. The module is equipped with data memory (SDRAM), FPGA bitstream memory (FLASH) and PCIe interface. The digital controller generates the arbitrary digital signal synchronized with LLRF controller that is used to excite the piezo actuator. The module realizes the following operations:

- Transmits the waveform from memory to DACs,
- Records the piezo sensor voltage and stores it to the memory,
- Monitors the piezo actuator voltage and current, performs calculations of piezo capacitance,
- Waits for a selected trigger,
- Provides communication channel to diagnostic controller,
- Can receive additional interlock signal (exception generated by the other module in critical situations, e.g. importer temperature of cryogenic system).

The digital controller provides the control signal for DAC device that converts the piezo actuation waveform into analogue signal that is being delivered to the driver module. This module consists of power amplifier and amplifier protection circuits. The power amplifier uses high voltage (±50 V) provided by the power supply module (DC/DC step-up converter) to amplify and generate a suitable control signal for piezo actuator. A high efficiency switching amplifier is planned to be used to limit the generated heat and power consumption.

The high amplitude driving signal is connected to piezo actuator via a switch and piezo protection systems. The piezo protection is an independent digital device that constantly monitors piezo supply voltage, current and power in order to detect conditions that could damage piezo actuator (e.g. too high voltage, current or energy transferred to piezo). Piezo protection circuit should fulfil the following requirements:

- Monitors the piezo voltage and current, calculates the dissipated power,
- Disables the driver, in order to prevent piezo from overheating,
- Disables the driver, in case of presence of excessive currents or voltages,
- Disables the driver in case of abnormal FPGA circuit operation,
- Once activated, has to be restarted by the FPGA.

The piezo device could operate in two modes: piezo-actuator and piezo-sensor. The mode of operation could be changed for both channels in order to enhance the blocking force, decrease driving signal amplitude and enhance the piezo lifetime. The piezo signal is digitized and recorded in case of piezo-sensor mode.
The piezo discharge module removes the charge from piezo element once the channel becomes disabled.
The control logic module provides a basic configuration and protection of the piezo controller. It is responsible for:

- Selection the operation mode of the piezo channels
- Implements the interlock function in a fast and reliable way
- Monitors the piezo presence
- Enables the discharge circuit

The device will be implemented using a simple programmable logic with build in FLASH memory (CPLD) in order to assure high reliability.
The diagnostic controller allows for basic diagnostics and management of the piezo actuator device:

- Monitors the board voltages, currents and temperatures on critical components,
- Controls the power supplies,
- Orchestrates the firmware upgrade process,
- Provides early warnings on the module health problems.

The firmware upgrade component provides is-system firmware upgrade of all programmable devices (microcontrollers, CPLD, FPGA) of the diagnostic controller:

The buffer/PHY module provides level translation between the controller module and actuator subsystem.

The hardware of piezo control system can be realised with three possible implementations:

- MicroTCA.4-based AMC Solution.
- External 19" Module Solution.
- MicroTCA.4-based and 19" box hybrid Solution.

Finally, the hybrid solutions with external 19” power supply was chosen by ESS. The details concerning the design of PCS hardware design is further described in the chapter 3.1.
The device will be built as a RTM component according to the following PICMG standards [1], [2], [3].

3.1. MicroTCA.4-based and 19” box hybrid solution

The piezo actuator controller is realised as Advanced Mezzanine Card module connected to Rear Transition Module via Zone 3 connector and external high-voltage power supply device.

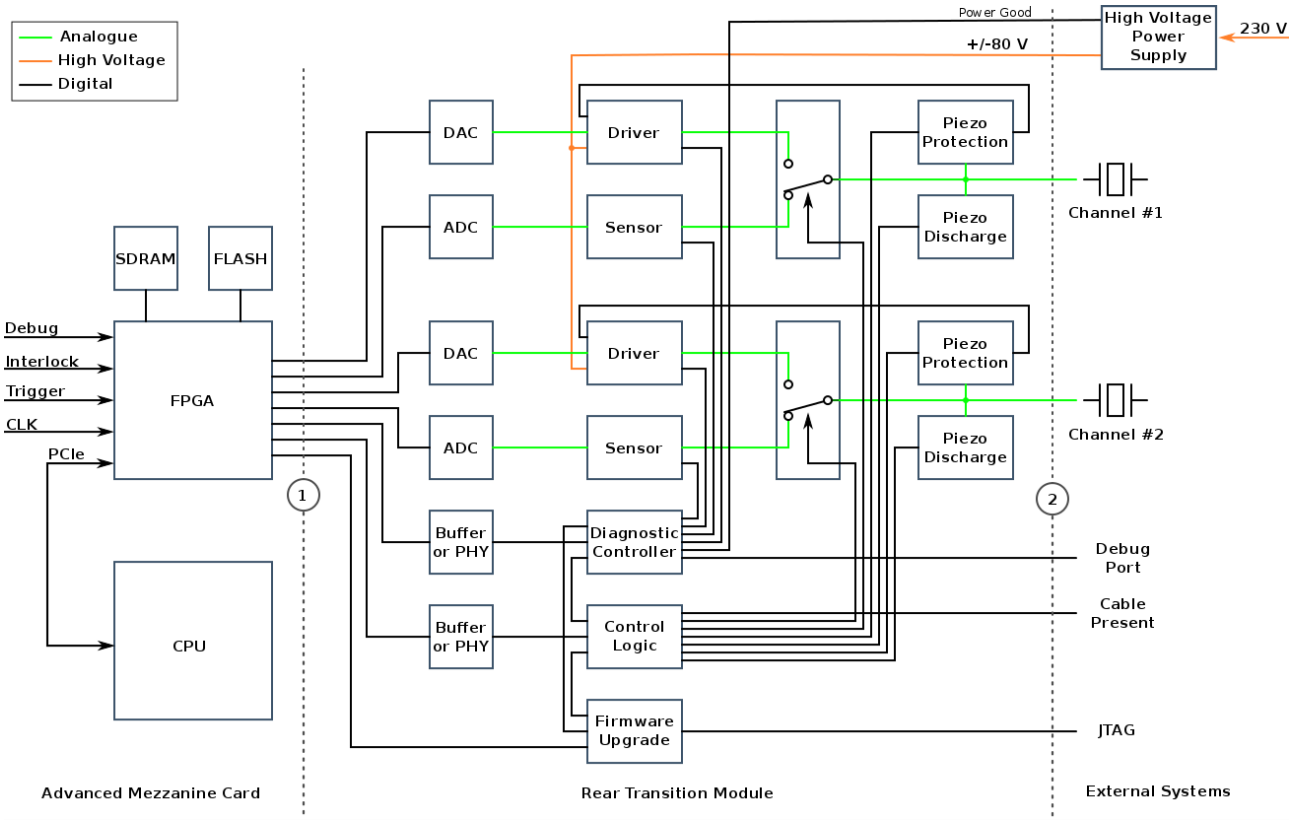

Figure 3 Block diagram of piezo control system implemented as a hybrid solution based on MicroTCA.4 and 19” box modules.

The AMC module provides FPGA processing power, communication interfaces, interlock and trigger signals that are connected to MicroTCA.4 infrastructure and external devices. The RTM device includes all components required for piezo operation (ADC, DAC, piezo driver, piezo sensor, piezo protection, switch module) and diagnostic circuits. The high voltage power supply is provided from

external powers supply unit realised as a standard 19” component. The powers supply module should provide the main power supply and basic diagnostics. At least power good signal is required or even more advanced diagnostics similar to IPMI or SMBus protocols should be provided. The diagnostics of power supply module is required to assure high reliability and availability in the similar way as it is realised in MicroTCA.4 systems.
The block diagram of the hybrid solution is presented in Figure 3. The Zone 3 signals between AMC and RTM modules are marked with 1, whereas the RTM signals and connection to the external power supply module is presented by 2.

Since, the Class-D amplifier has a high efficiency (80–90%) it seems to be realistic to implement the piezo driver module as RTM device. It is assumed that a single RTM slot could dissipate maximum 30 Watts. Further, assuming that single piezo driver channel will provide maximum 50 Watts and the amplifier efficiency is 80%, the maximum generated power is estimated to 10 Watts for a single channel. The additional 10 Watts should be enough to realize the diagnostic and protections devices.

4. Prototype of Piezo Control Device

The first prototype of the PCD was built and tested at TUL-DMCS and Freia laboratories. Piezo driver was first evaluated with capacitors emulating piezo actuators. Next, the device was evaluated with two piezo actuators of spoke cavity installed in the cryostat. More tests with in cryogenic temperature with elliptical and cope cavities are planned in the future.

4.1. Tests at DMCS laboratory

The evaluation setup used during the tests is shown in Figure 4, while system connectivity is presented in Figure 5. The control and data acquisition system was built using the MicroTCA.4 technology. The setup is controlled by a general purpose x86 computer module. It communicates with the MFMC digitiser and control module over the PCIe interface.

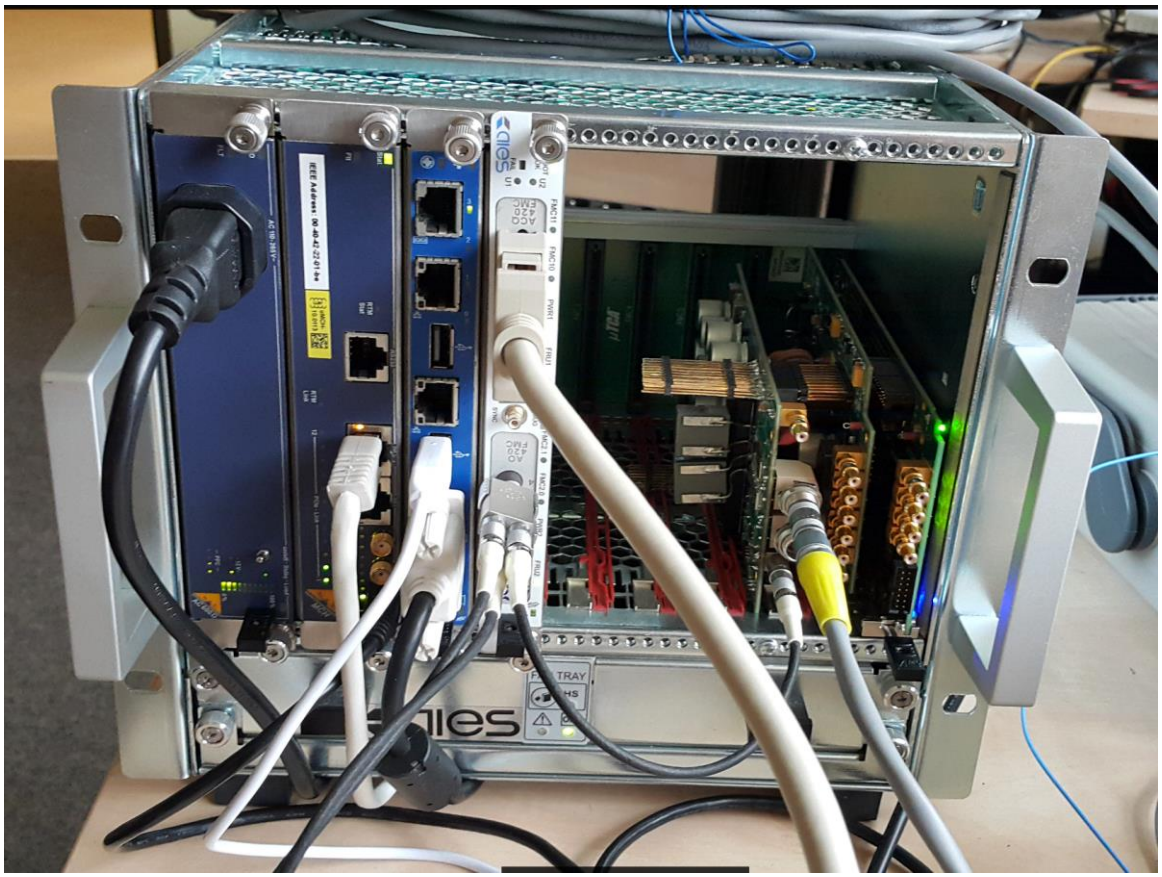

Figure 4 The MicroTCA.4 system applied for PCD testing

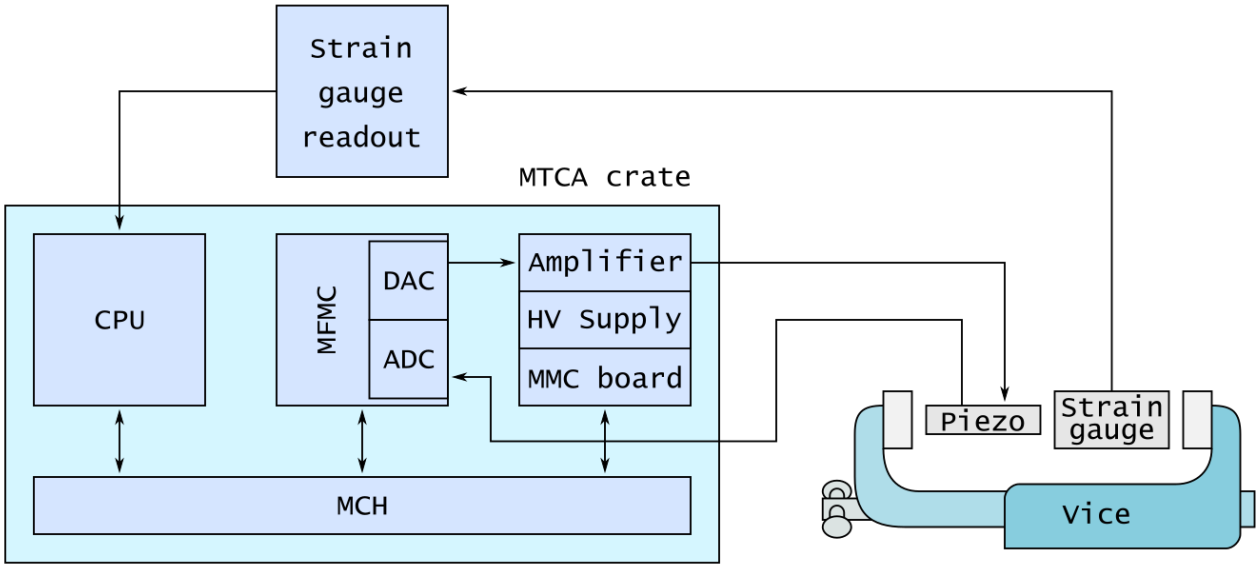

Figure 5 Measurement setup block diagram

The MFMC board, shown in Figure 6, is a dual FMC carrier with an Artix-7 FPGA. It is equipped with two FMC modules, which provide it with the analogue input and output channels. The firmware implemented on this module provides functionality of a basic oscilloscope and arbitrary generator. The analogue signals generated on the MFMC outputs are in range of ±1 V.

Figure 6 The MicroTCA.4 board with ADC and DAC modules

The low-level analogue signals are provided to the PCD prototype for amplification. The complete prototype composed of: a AMC carrier module with the Module Management Controller (module 1), high-voltage power supply (module 2) and power amplifiers (modules 3 and 4) is presented in Figure 7. Its main component, the power amplifier, is additionally shown in Figure 8. Up to two power amplifiers can be installed in this “sandwich” (modules 3 and 4). The carrier card is responsible for communication with the MTCA.4 crate, negotiation of the power supply and handling of the activation and deactivation procedure. Additionally, its microcontroller is used for development of the piezo protection mechanisms. The power supply mezzanine generates voltages of ±50 V, ±5 V and –38 V, utilized by the power amplifier.

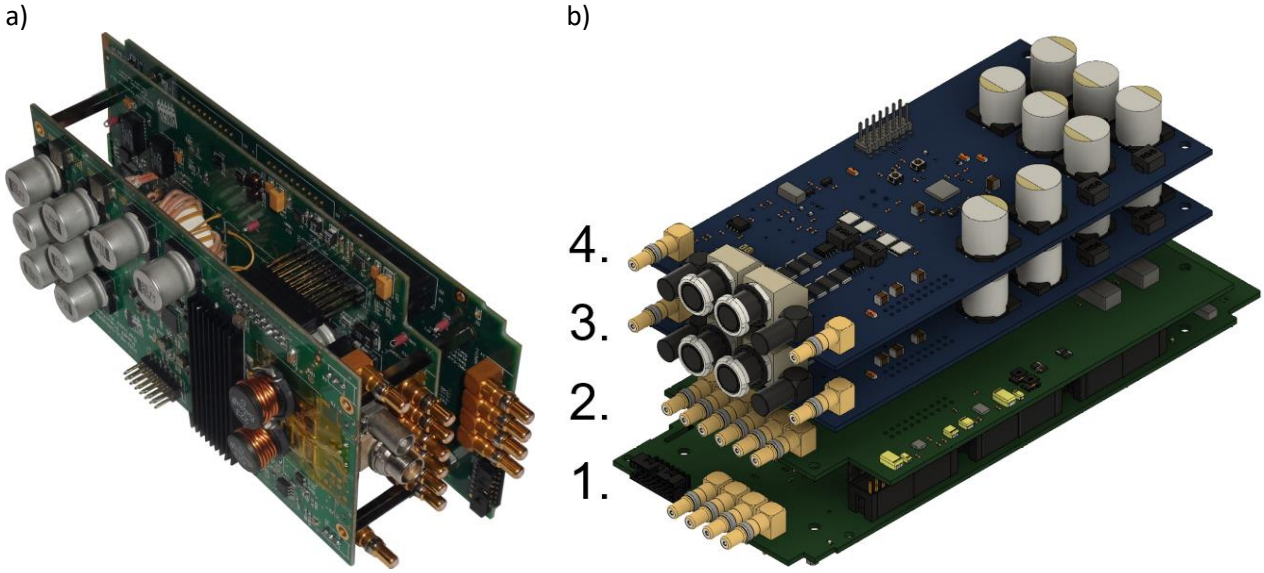

Figure 7 The piezo driver prototype

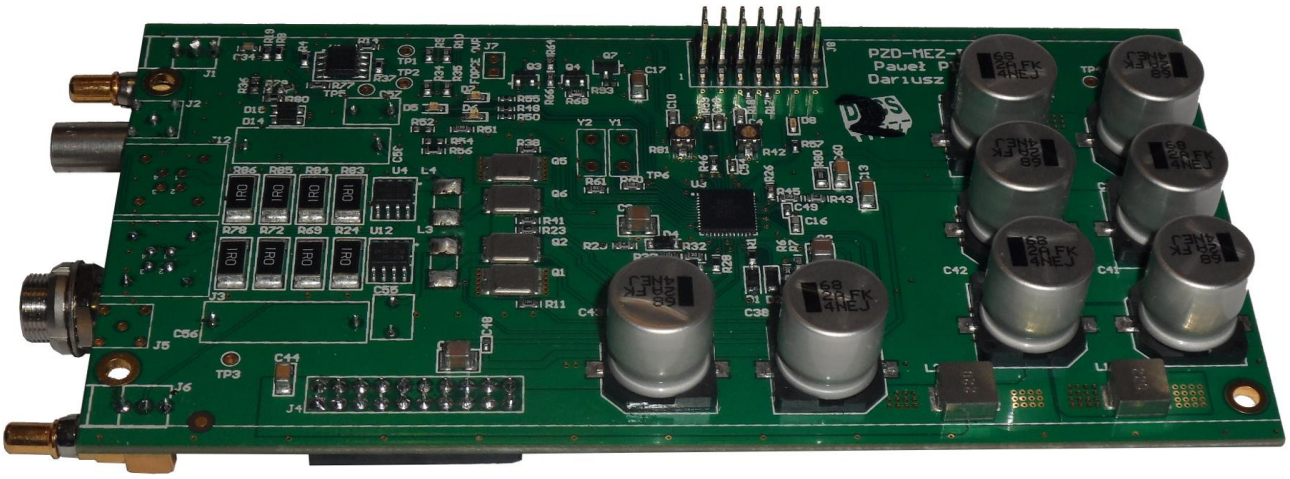

Figure 8 Piezo driver amplifier module

The D-class amplifier boosts the input signal by 40 dB (voltage multiplied by a factor of 100). It is characterized for load capacitances of up to 20 µF. Its output voltage is provided to a 15-element piezo stack from Noliac (NAC 2022 H30-C01) mounted in the machine vice, see Figure 9 for reference. The machine vice is used for ensuring a preload force of 1000 N for each piezo actuator, which is required for safe operation. The force was measured with the S-type load cell and dedicated readout

module, connected to the CPU over the USB interface.

Figure 9 Two piezo components assembled in a machine vice

The control panel for the MFMC board is shown in Figure 10. It was designed to loosely resemble the interface of modern oscilloscope (on the left) and function generator (on the right). For the sake of performance it was written in C++ with use of the Qt library and the QCustomPlot extension.

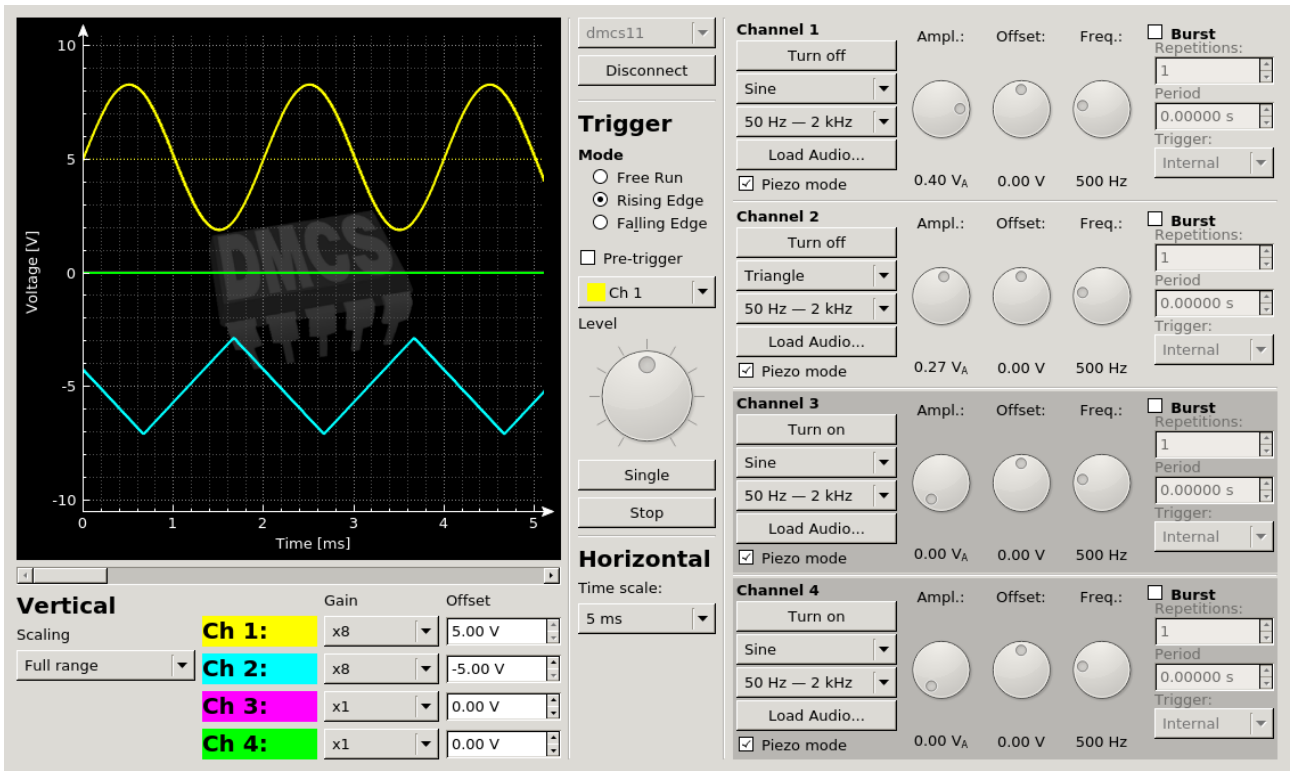

Figure 10 The control panel of the function generator developed for testing the PCD.

For safety reasons, the driver was initially tested with a set of film capacitors (from 1 µF to 20 µF), instead of the actual piezo actuator. Tests were focused on validating operation of the amplifier in different conditions, finding the power consumption for a various driving signals and finally the maximum output signal for tested capacitance. As a result Safe Operation Area (SOA) characteristics were measured for 4 various capacitive load conditions.

The next step was to find the limiting values for the device's safe operation area. The tests were done by exploration of the amplitude-frequency plane and finding the points where the amplifier is disabled by any of the built-in protection systems (mainly the overcurrent and overtemperature). The piezo amplifier was operating in Continuous-Wave (CW) mode during the tests. The resulting boundaries for several load capacitances are plotted in Figure 11.

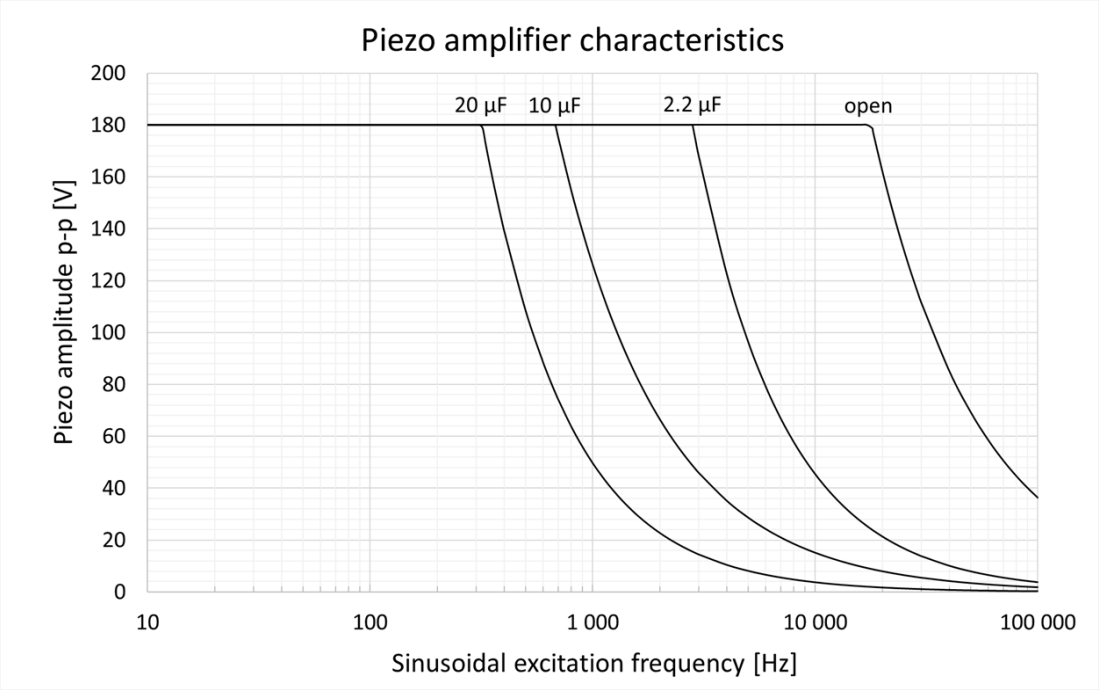

Figure 11 Safe operation area characteristics of the designed driver prototype.

The tested prototype of the amplifier allows to control the medium- and high-beta cavities Noliac NAC 2022 H30-C01 piezo actuator (capacitance in cryo temperature 2.2 µF) with 180 Vpp maximum amplitude and almost 3 kHz frequency in CW mode. The performance in pulsed mode should be even better. This measurement proves that the designed amplifier fulfils the required specification.

The developed piezo driver prototype should be able to also to drive the Noliac and PI piezo actuators planned to be used in spoke cavies (ca. 5.8 and 10 µF capacitance in cryo temperature). Figure 11 allow us to estimate the maximum driving parameters in CW mode of operation:

- For Noliac piezo we could reach maximum 180 Vpp amplitude for 1 kHz signal.
- For PI piezo we could reach maximum 120 Vpp amplitude for 1 kHz signal.

The device should be able to operate with maximum 180 Vpp amplitude for both piezo actuators in pulsed mode. However, this is strongly recommended to verify the parameters with real piezo actuators in real conditions.

The designed prototype is able to reach the point of 100 Vpp, 1 kHz signal in CW mode with load capacitance of 10 µF, whereas the commercial construction (LE200/070 EBW driver) can only drive

the load of around 2 µF at this point. A careful examination of the differences between these charts shows that the performance of the prototype solution is much better for most points of the considered part of the amplitude-frequency plane. For comparison Figure 12 presents analogous characteristics of the commercial LE200/070 EBW amplifier, dedicated for driving capacitive loads. This driver is used at Freia and Institut de Physique Nucléaire facilities.

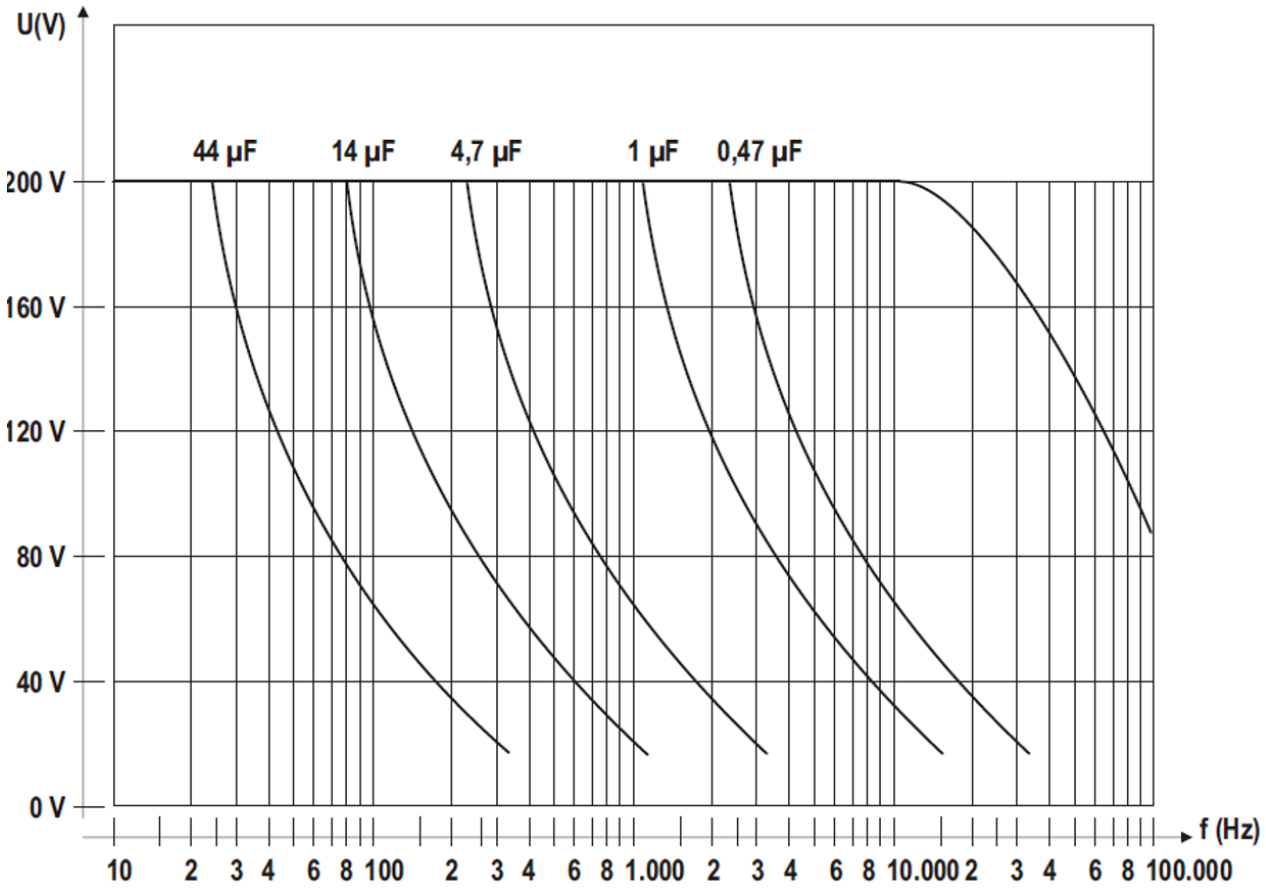

Figure 12 Safe operation area characteristics of the commercial LE200/070 EBW driver

The first test was aiming at determining the piezo-actuator and piezo-sensor coupling. As presented in Figure 13, the first piezo has been driven with 44 V_{pp}, 1 kHz sine CW excitation. The signal on the readout of the second piezo was about 0.600 mV, giving the transfer coefficient between the piezo elements about 0,014.

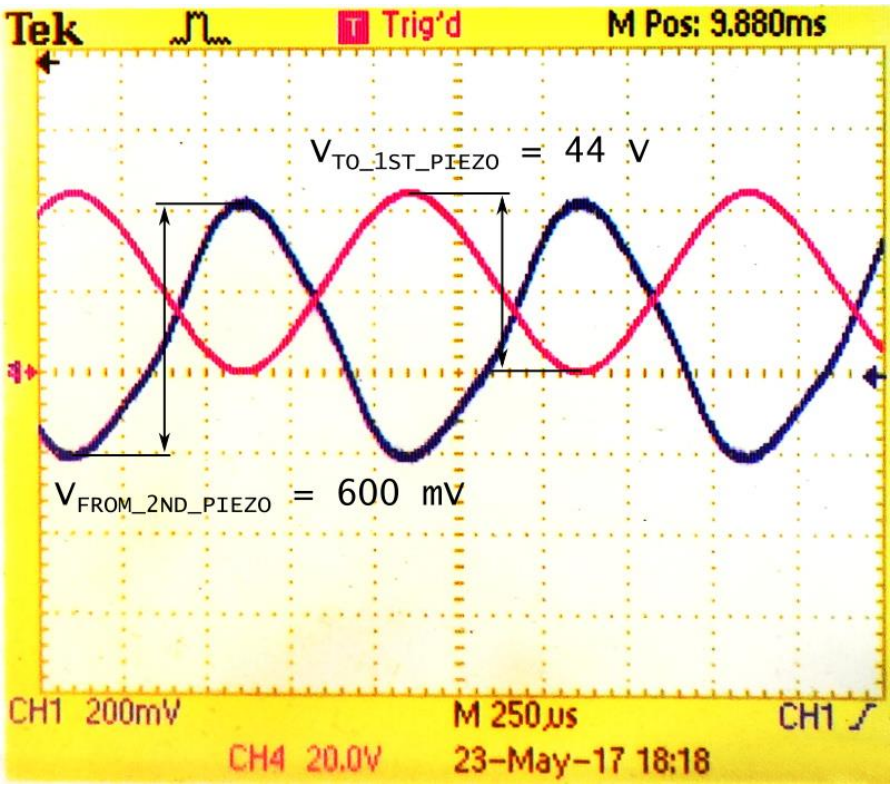

Figure 13 Signal amplitude measured on piezo driver and piezo sensor

As all the tests in the DMCS laboratory were completed successfully the next set of tests was scheduled with the actual cooled-down accelerating cavity.

4.2. Tests at Freia laboratory

The tests at Freia laboratory were performed from 19.04.2017 to 21.04.2017 with the spoke cavity installed in a cryostat. The cross-section of spoke cavity is presented in Figure 14.

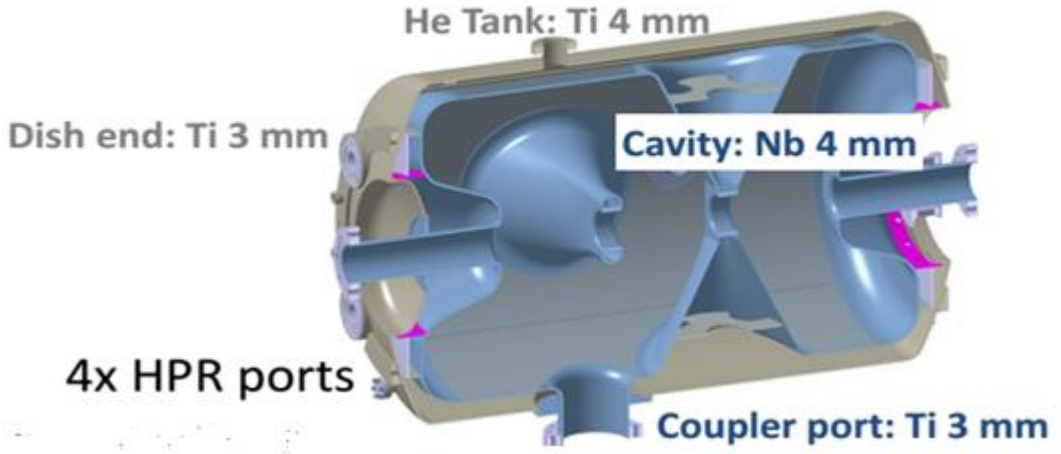

Figure 14 Cross-section of the spoke cavity

The cavity was equipped with a stepper motor and two piezoelements for the cavity tuning.

The piezoelement on the left side in Figure 15 was a Noliac NAC 2022 H50-C01. The temperature of the piezo was measured by the sensor TT02x. Before the tests have started, it was 18.76 K and went up to 62.36 K maximum after the piezo excitation tests. The piezo capacitance has been measured before the tests have started and amounted to 3.14 µF (temperature 18.76 K).

The piezoelement on the right side in Figure 15 was a PI PICMA P-888.91. The temperature of the piezo was measured by the sensor TT03x and has grown from 26.47 K before the tests have started to 33.20 K after the tests. The piezo capacitance before the tests have started was equal to 5.18 µF (temperature 26.47 K).
The specification of piezoelements from Noliac and PI used during the tests at Freia laboratory is summarised in Table 5. The Noliac NAC 2022 H30-C01 piezo actuator of medium- and high-beta cavities was added for comparison.

Table 5 Piezo stack specification

Piezo type	Noliac NAC 2022 H30-C01	Noliac NAC 2022 H50-C01	PI PICMA P-888.91
Dimensions	10 x 10 x 30 mm	10 x 10 x 50 mm	10 x 10 x 36 mm
Cell material	NCE51F	NCE51F	PIC252
Number of cells	15	25	
Capacitance (room temperature)	6.6 µF ±15%	9.5 µF ±15%	13 µF ±20%
Capacitance (cryo temperature, 20 K)	TBD	3.14 µF[3]	5.18 µF[2]
Max. free stroke	49.5 µm	79.2 µm	32 µm
Blocking stroke in cryo temp.	3 µm	5 µm	TBD
Blocking force max.	4200 N	4200 N	3800 N
Max. operating voltage	200 V	200 V	-20 to 120 V
Max. operating temperature	150°C	150°C	150°C
Unloaded resonance frequency	248 kHz – 11 kHz	248 kHz – 11 kHz	40 kHz
Comment	DMCS laboratory	Freia laboratory	Freia laboratory

The tests were performed with the following MTCA.4 crate configuration:

- 12-slot MicroTCA.4 chassis manufactured by Schroff
- NAT-PHYS Module Carrier Hub
- Kontron CPU in slot 1,
- Piezo driver prototype was installed in slot 12, composed of:
    - AMC carrier module (component #1 in Figure 7).
    - High voltage power supply with DC/DC converter (component #2 in Figure 7).
    - Single D-class power amplifier (component #3 in Figure 7).

[3] Measured with Fluke 123 scope meter.

The configuration of hardware components used during the tests at Freia facility is presented in Figure 16. The Noliac piezo (piezo #1) was connected to Piezo driver #1 output and it was used as an actuator, whereas the PI (piezo #2) device connected to digitizer input operated in sensor configuration.
The piezo driver was connected with the cryostat with the Dataflex Cable, dual 2x0.25 mm^2 twisted pair cable. The cable resistance (both directions in total) was R = 4.7 Ohm, which gives as estimate ca. 35 m of cable length.

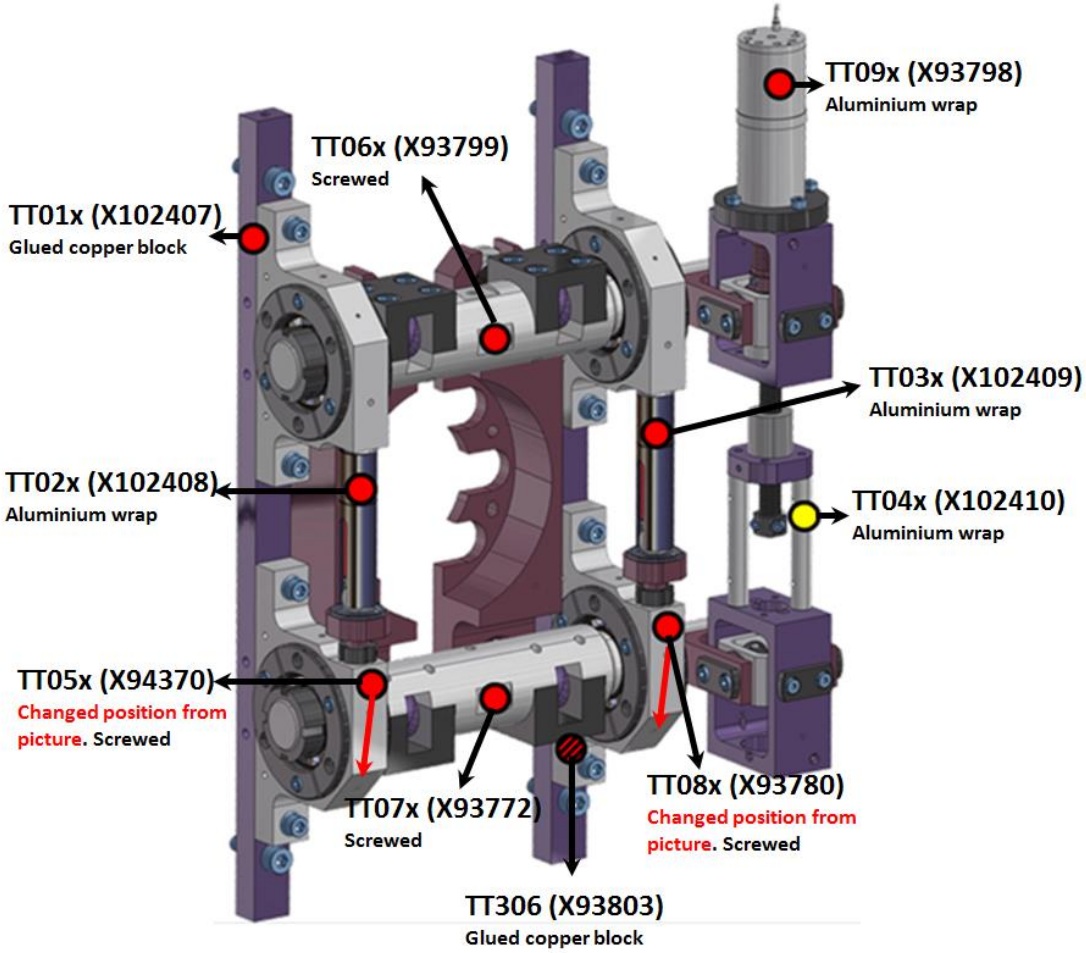

Figure 15 Schematic diagram of piezo actuators, motor and temperature sensor mount – Cold Tuning System (CTS).

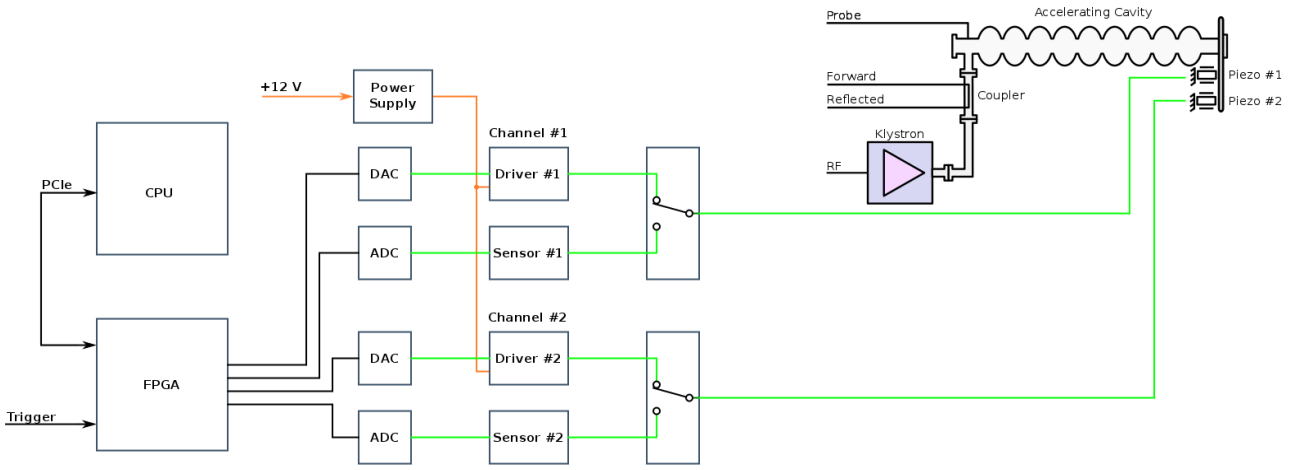

Figure 16 The hardware setup used during tests at Freia facility

Next, the driver performance has been evaluated in various configurations of the piezo actuators. Two main test types were performed operating the device in continuous-wave and pulsed mode.
The CW tests were performed for 1 kHz frequency in two variants:

- Both piezos connected in parallel to a single driver
  - We were able to achieve the output voltage amplitude of 132 V_{pp} before reaching the protection limit.
- Two drivers driving separate piezos
  - We were able to achieve the output voltage amplitude of 128 V_{pp} before reaching the current limit in case of Noliac NAC 2022 H50-C01.
  - We were able to achieve the output voltage amplitude of 120 V_{pp} before reaching the current limit in case of PI PICMA P-888.91.

The pulsed-mode tests were performed in conditions that are closer to future operation of ESS accelerator: 10 pulses of 1 kHz sine wave signal with repetition rate of 14 Hz. Pulsed-mode tests were performed in two variants:

- Both piezos connected in parallel to a single driver
  - We were able to achieve the maximum of 180 V_{pp} amplitude; the driver was not disabled by protection circuit.
- Both piezos connected to two piezo driver modules (module 3 and 4 as presented in Figure *7*):
  - We were able to achieve the maximum of 180 V_{pp} amplitude on both piezo actuators; none of the drivers was disabled by protection circuit.

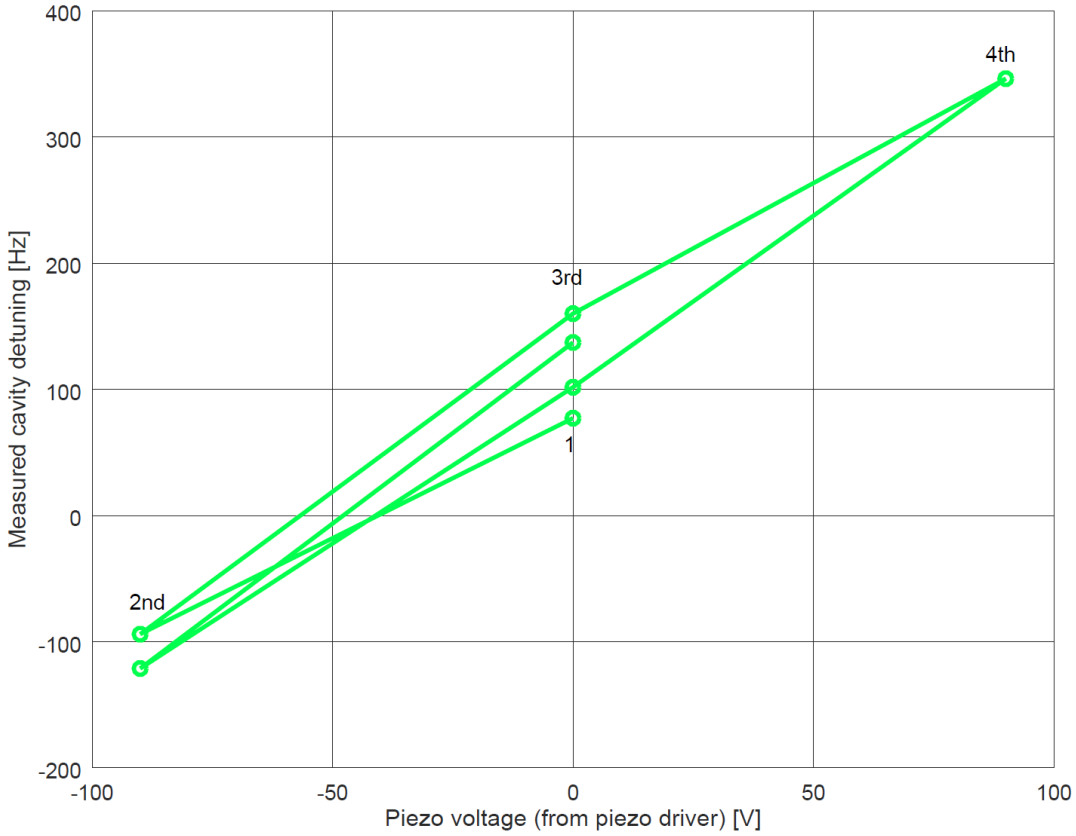

Figure 17 Cavity detuning vs piezo excitation voltage

Finally, the cavity detuning versus the excitation voltage of piezo driver has been measured for two components operating in parallel as actuators (see Figure 17). We achieved cavity frequency change for maximum voltage change from -90 V to +90 V at the level of 460 Hz.

Summary and conclusions from the tests at Freia facility

The tested prototype of the amplifier allows to control both: Noliac NAC 2022 H50-C01 and PI PICMA P-888.91 actuators, connected in parallel (total capacitance in cryo temp 8.32 µF) with maximum amplitude 132 Vpp and 1 kHz frequency in CW mode. The current consumption from 12 V payload power was reaching 5.6 Amps during the tests. The heat dissipation during the operation was estimated to ~7 Watts, the driver temperature was 35 ºC. This corresponds very well to measurements performed at TUL-DMCS laboratory (see Figure 11).

Both piezo actuators were operated with maximum 180 Vpp amplitude and 1 kHz frequency in pulsed mode of ESS accelerator-like conditions (repetition rate 14 Hz). A single PCD was able to drive the piezo actuators with 10 sinusoidal pulses that fulfils with excess the specification defined in table Table 1. The current consumption from 12 V payload power was reaching 8 Amps during the tests. The heat dissipation during the operation was estimated to ~10 Watts, the driver temperature was 40 ºC. Similar results were obtained for two piezo amplifiers driving both, PI and Noliac piezo elements. The drivers were able to operate with maximum amplitude of output signal.

The designed piezo driver prototype is definitely able to drive the medium- and high-beta cavities

NAC 2022 H30-C01 piezo actuator with maximum amplitude even in CW mode. In such configuration the dissipated power on the RTM device should be less than 26 Watts for both channels. The power available in a single AMC slot of MicroTCA.4 chassis (80 W) seems to be enough to supply dual channel piezo driver.

The designed driver prototype should also drive the spoke cavity piezo actuators: Noliac NAC2022-H90-A01 (capacitance in cryo temp 5.8 µF) and PI PICMA P-888.91 (total capacitance in cryo temp 10 µF) in pulsed mode operation. Both piezo elements have a similar capacitance to the tandem of piezo actuators tested at Freia facility. However, this configuration was not tested with real piezo actuators and therefore requires more measurements and confirmed parameters of piezo actuators (the capacitance in cryo temp is unknown and was estimated).

In summary, it can be conclude that the measurements at Freia facility proves that the designed amplifier prototype fulfils the required specification.

5. Proposed final design of Piezo Control Device

The Piezo Control Device should smoothly fit on an RTM card template, as shown in Figure 18. The module is connected to AMC module, providing it with power, IPMI management and payload control signals. The boards communicate through a Zone3 interface.

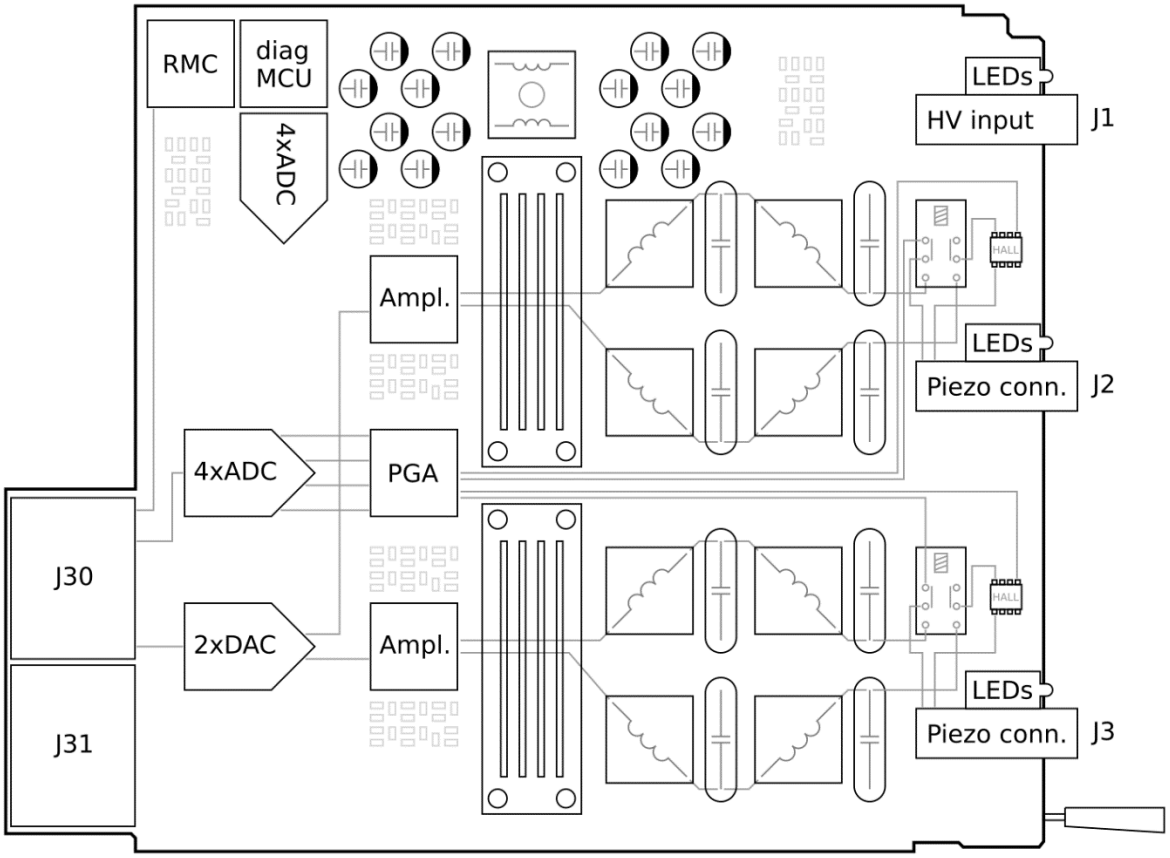

Figure 18 The final design of Piezo Control Device

The control signals from the AMC module are supplied to a dual DAC circuit, which drives two piezo actuators output channels. Each channel is composed of the high-efficiency D-class full-bridge power amplifier driving the output through 4th order low-pass passive filter and relay. The relay is used for switching between sensor and actuator modes, independently for each channel. In the sensor mode, the voltage from piezo is provided to an ADC circuit through a Programmable-Gain Amplifier (PGA). The ADC is also monitoring the output current by means of a Hall-effect-based current sensor.

The output current and output voltage of the power driver are also monitored by a dedicated protection and diagnostic processor. This circuit has control over the enable signal of power amplifiers and over the aforementioned relays. Its aim is twofold: to protect the piezo actuator from damage and the operator from electric shock. It safely disables the output channel upon detecting cable disconnection, short-circuit or driving waveform exceeding safe limits in several tens of milliseconds.

The PCD module is equipped with RTM Module Controller (RMC) in order to enhance the driver reliability, availability and improve its serviceability. The crucial parameters of the device (temperatures and power supply voltages) are constantly monitored by an RTM Module Controller (RMC),

responsible for the module health monitoring. When the parameters are out of range the RMC controller generated events and waring. When the parameters reach critical levels the Module Carrier Hub IPMI (Intelligent Platform Management Interface) controller could disable the module and signal failure. The hot-swap functionality simplifies and improve device servicing and inspecting according to Intelligent Platform Management of MicroTCA and AdvancedTCA systems. It will also interface the protection circuit for reporting its state over the IPMI mechanism.

The module will use the Management (+3.3 V) and Payload (+12 V) voltages provided by the AMC module via Zone 3 connector. The AMC module should provide min. 30 W on payload power as defined in MicroTCA.4 specification [4]. The RMC needs 50 mA on management power. The RMC will be connected via I2C management bus with Module Management Controller installed on AMC. The extended version of RMC will be applied for the piezo driver health monitoring and management [4].

Most systems of the PCD are powered from the voltages produced from 12 V Payload Power and 3.3 V Management Power received through J30 connector. The power amplifier stage is, however powered with ±50 V that has to be delivered by an external power supply. The board is equipped with a high-voltage filter reducing EMI.

5.1. Interfaces and front-panel indicators

The PCD has all required by MicroTCA.4 components. The front of PCD will include:

- Hot-plug handler.
- Blue, green and red indicators requested by the MicroTCA.4 standard.
- External high-voltage power supply connector.
- Connectors for two piezo devices.

The RTM PCD module will be connected to AMC device using the Zone 3 connector as defined in the MicroTCA.4 specification. All signals defined in MicroTCA.4 specification will be connected to Zone 3 J30/J31 connectors.

5.1.1. Connectors

The Piezo Driver will use 3 connectors available on the front-panel:

- J1 - HV input Lemo EXG.0B.307.HLN.
- J2, J3 - Piezo connector Lemo EXP.0S.304.HLN.

The detailed signal assignment of power supply connectors is presented in

Table 6, whereas the signals of piezo devices are described in Table 7.
The piezo actuator plug should include a 4.7 kΩ±5% resistor between pins 3 and 4. This resistor is required for proper identification of connected cable and provides a safety interlock. Unplugged or disconnected cable, wrong resistance, open or shortcut connector pins automatically disable the high-voltage power amplifier and therefore disable high voltage on connectors J2 or J3. This protects the operator against electric shock. In addition, the whole piezo driver will be covered and shielded with a steel housing.

Table 6 Signals of J1 power supply connector

Connector pin	Description	Electrical Specification	Direction
1	High voltage +	Max. 60 VDC, 1 A	In
2	GND	Ground, 2 A	
3	High voltage -	Max. 60 VDC, 1 A	In
4	SMBus - SDA	LVTTL 3.3 V	In-Out, Open Drain
5	SMBus - SCL	LVTTL 3.3 V	Out, Open Drain
6	SMBus - Alert	LVTTL 3.3 V	In
7	SMBus - GND	Ground	

System Management Bus (SMBus) is required for the enhanced diagnostics of external power supply module according to ESS RAMI requirements.

Table 7 Signals of J2 and J3 piezo connectors

Connector pin	Description	Electrical Specification	Direction
1	Driver output +	Max. 200 VDC, 1 A	Out
2	Driver output -	Max. 200 VDC, 1 A	Out
3	Plug ID	LVTTL 3.3 V	In
4	Gnd	Ground	

The J30 and J31 signals should follow the D1.2 Digital Class Zone 3 pin recommendations proposed by TUL-DMCS and DESY institutes[4], however the GTP high-speed lines will be not used.

The payload components of the PCD require two signals levels:

- Differential LVDS 2.5 V.
- Single ended LVCMOS 2.5 V.

A suitable termination is required for all LVDS signals receivers on both AMC and RTM devices. The PCD device will use the P30_IO and P31_IO signals as defied in the Zone 3 recommendation starting from J30 A5 signals.
The AMC carrier should support the differential and single ended clock signals connected to FPGA device. The signals will be mainly connected to SPI busses driving the DAC and ADC devices.
The list of signals connected to Zone 3 connectors is presented in Table 8. The detailed signals assignment will be decided during PCB routing. The list of signals could be extended during the final design of the device and therefore 20 digitals signals are reserved for further extension.

Table 8 Signals of J30 and J31 RTM connectors

ID	Signal Name	Description	Electrical Specification	Direction
	Piezo driver (DAC) channel 1			
1	**Piezo1_DAC_CSn**	Serial Interface Chip Select of DAC 1	LVCMOS 2.5 V	In
2	**Piezo1_DAC_SCLK**	Serial Interface Clock Input of DAC 1	LVCMOS 2.5 V	In

[4] Zone 3 Pin Assignment is available on http://mtca.desy.de/resources/zone_3_recommendation/index_eng.html.

3	**Piezo1_DAC_DIN**	Serial Interface Data Input of DAC 1	LVCMOS 2.5 V	In
4	**Piezo1_DAC_CLRn**	Asynchronous Clear Input of DAC 1	LVCMOS 2.5 V	In
5	**Piezo1_Enable**	Enable channel 1 of power driver	LVCMOS 2.5 V	In
6	**Piezo1_Good**	Piezo driver 1 good signal	LVCMOS 2.5 V	Out
	Piezo driver (DAC) channel 2			
7	**Piezo2_DAC_CSn**	Serial Interface Chip Select of DAC 2	LVCMOS 2.5 V	In
8	**Piezo2_DAC_SCLK**	Serial Interface Clock Input of DAC 2	LVCMOS 2.5 V	In
9	**Piezo2_DAC_DIN**	Serial Interface Data Input of DAC 2	LVCMOS 2.5 V	In
10	**D Piezo2_DAC_CLRn**	Asynchronous Clear Input of DAC 2	LVCMOS 2.5 V	In
11	**Piezo2_Enable**	Enable channel 2 of power driver	LVCMOS 2.5 V	In
12	**Piezo2_Good**	Piezo driver 2 good signal	LVCMOS 2.5 V	Out
	Piezo sensor (ADC) channel 1 and 2			
13	**Piezo_ADC_SCK**	Serial Data Clock Input	LVDS 2.5 V	In
14	**Piezo_ADC_SEN1_SDO**	LVDS Serial Data Output Channel 1	LVDS 2.5 V	Out
15	**Piezo_ADC_SEN2_SDO**	LVDS Serial Data Output Channel 2	LVDS 2.5 V	Out
16	**Piezo_ADC_ACT1_SDO**	LVDS Serial Data Output Channel 3	LVDS 2.5 V	Out
17	**Piezo_ADC_ACT2_SDO**	LVDS Serial Data Output Channel 4	LVDS 2.5 V	Out
18	**Piezo_ADC_CLKOUT**	Serial Data Clock Output	LVDS 2.5 V	Out
19	**Piezo_ADC_CNVn**	Start conversion	LVCMOS 2.5 V	Out
20	**Piezo_ADC_LVDS_EN**	Enable LVDS Interface	LVCMOS 2.5 V	In
21	**Piezo_ADC_DDR_EN**	Enable Double Data Rate Interface	LVCMOS 2.5 V	In
	Piezo sensor gain for channel 1 and 2			
22	**Piezo_ADC_SEN1_GAIN0**	Set piezo sensor 1 gain, bit 0	LVCMOS 2.5 V	In
23	**Piezo_ADC_SEN1_GAIN1**	Set piezo sensor 1 gain, bit 1	LVCMOS 2.5 V	In
24	**Piezo_ADC_SEN2_GAIN0**	Set piezo sensor 2 gain, bit 0	LVCMOS 2.5 V	In
25	**Piezo_ADC_SEN2_GAIN1**	Set piezo sensor 2 gain, bit 1	LVCMOS 2.5 V	In
26	**Piezo_ADC_GAIN_CS1**	Set piezo sensor 1 gain chip select	LVCMOS 2.5 V	In
27	**Piezo_ADC_GAIN_CS2**	Set piezo sensor 2 gain chip select	LVCMOS 2.5 V	In
	Diagnostic controller bus			
28	**Diagnostic bus 0..7**	FPGA to diagnostic controller 8 bit bus (SPI + 4x IO)	LVCMOS 2.5 V	In/Out
	Extension bus			
29	**Extension_Signals 0..19**	Signals reserved for future extension	LVDS 2.5 V / LVCMOS 2.5 V	In/Out

5.1.2. Indicators

The PCD will use 3 indicators as required by the MicroTCA.4 specification, see Table 9.

Table 9 IPMI indicators

LED indicator	Description
Blue	Hot-plug activity
Green	Proper operation
Red	Hardware problem detected

Both channels of piezo drivers will 4 indications presenting the mode of operation and possible channel failure as presented in Table 10.

Table 10 Piezo driver indicators for piezo driver channel 1 and 2

LED indicator	Description
Yellow	Channel in sensor mode operation
Green	Channel in actuator mode operation
Orange	High power/temperature operation
Red	Channel failure

6. External power supply module

During the laboratory tests at the DMCS and at Freia the piezo driver prototype, implemented as AMC card, was powered from the MicroTCA Payload Power (+12 V).

According to ESS requirements the PCD will be implemented in form of RTM module. The RTM device compliant with MicroTCA.4 could consume and dissipate maximum 30 Watts in the chassis. The maximum RTM dissipated power is mainly limited by the chassis redundant cooling system and the Payload Power supply delivered by AMC module [1].

A few various decisions was made to maximize the piezo driver power and still design MicroTCA.4 compatible module:

- High efficiency D-class amplifiers will be used to drive the piezo actuators.
- Piezo driver will be supplied from external power supply module installed outside the MicroTC.4 chassis.
- The design of the piezo driver will be optimised to assure high-efficiency and low power consumption. Selected high-efficiency and high-quality components need to be applied to design the piezo driver module.

The applied D-class amplifier requires bipolar, stabilised power supply ±55V ±10%. A suitable power supply device is required to provide continuous and reliable power supply, high reliability, availability, and serviceability (RAS).

Three solutions for providing the external supply voltage to the PCD were proposed as illustrated in Figure 19. These solutions are based on various power supply modules:

1. Commercially available laboratory power supply.
2. Custom solution based on industrial 19” power supply
3. Custom solution based on 19” power supply with additional health monitoring (temperatures and voltages).

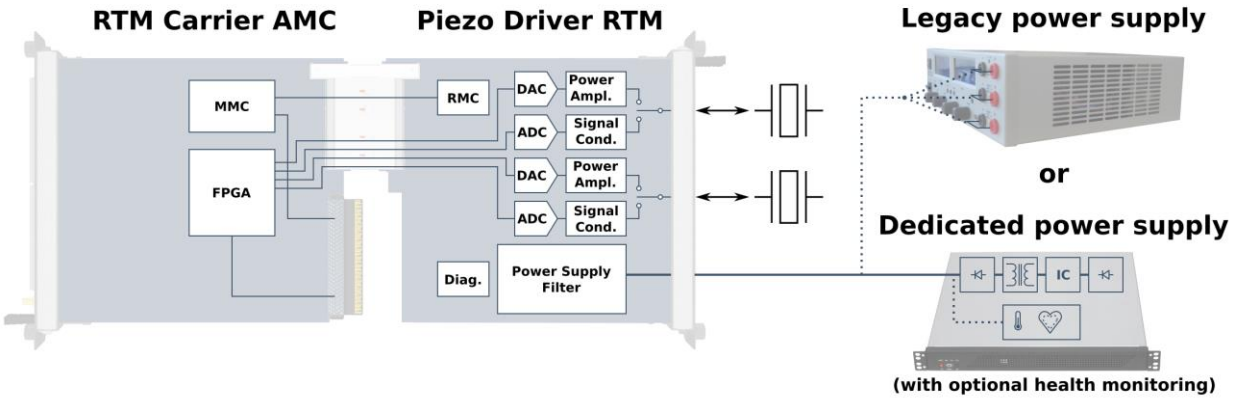

Figure 19 Foreseen schemes of external power delivery to Piezo Control Device

The first option use a standard laboratory power supply. This is the cheapest option, however provides the lowest level of RAS. This supply is not suitable for continuous operation. User could easily change the voltage and therefore damage the piezo driver module.

The second option could use an industrial high-reliability power supply and therefore assure long

availability. Its availability could be further enhanced using an additional health monitoring system in similar way to AdvancedTCA and MicroTCA systems. The system could monitor the crucial parameters (e.g. temperature, fan speed, power supply voltages, currents, etc.) and provide alarms when parameters are out of range. The system could be integrated with the IPMI management controller of MicroTCA.4 chassis. Parameters could be read and processed by the Module Carrier Hub. Reading the health management sensors and proper reaction to the events will allow to predict potential failures before they happen.

7. Control and Monitoring Software

TUL-DMCS (as a part of PEG) will design, manufacture, and evaluate the PCD modules. The whole software components required for PCS, including FPGA firmware, should be provide by ESS.
TUL-DMCS will provide the firmware for Module Management Controller (MMC) and RTM Management Controller (RMC) processors.

8. Manufacturing and Testing

Currently, the first piezo driver prototype was built and successfully tested in laboratory conditions. The second prototype (revision A) is under development. More tests are planned for the second revision of the piezo driver prototype. In particular, a cryo-module evaluation in cryogenic temperature are planned:

- Tests with elliptical medium-beta cavity equipped with dual Noliac NAC 2022 H30 actuators.
- Tests with spoke cavity equipped with 90 mm actuators, i.e. Noliac NAC2022-H90-A01 or PI PICMA P-888.91.

The detailed schedule for tests with cryostat will be agreed with ESS.

8.1. Planned schedule for piezo drivers production.

The detailed schedule including piezo driver design, hardware components procurement, production, testing, and delivery is presented below. The schedule starts from T0 date October 1st 2016 as defined in Schedule AIK 8.2 [1]. Five Milestones were defined for piezo driver: M8, M15, M24, M29, M34 and M35.

The mass production of medium-beta piezo driver modules will be preceded with preproduction. First, 10 modules will be manufactured. The preproduction phase should verify the quality of mass production devices but it is not supposed to correct any design or functional problems. Three randomly selected modules will be carefully verified and analyzed in laboratory conditions. All ten modules will be tested with developed automated test-stand and test-report for each module will be generated. The production of remaining 26 modules will be released as soon as modules pass laboratory and automated tests. Finally, all 36 modules will be delivered to NCBJ in month T0+25, three months before the Milestone M24 “Delivery of M-Beta units to ESS ERIC Lund”.

Revision B of the second prototype will be produced and carefully tested before the mass production for high-beta cavities piezo drivers. The revision B will include corrections and solve all problems that will be reported for revision A. It is not planned to release a preproduction phase before the final production of high-beta and spare modules (Milestones M34 and M35, see schedule below). The mass production of both high-beta and spare modules will be done in parallel.

Schedule for procurement, manufacturing, testing and delivery

Development or production phase	No of PCD mod	Schedule	Est. Delivery Date
First prot. design			
First prot. production	2		
First prot. testing			Jul'17
Second prot. design Rev. A			
Second prot. production Rev. A	5		
Second prot. testing Rev. A			Mar'18
Preproduction			
Preproduction testing	10		
Proc. and production for M-beta			
Testing of medium-beta			
Delivery of medium-beta	36		Oct'18
Second prot. design Rev. B			
Second prot. production Rev. B	5		
Second prot. testing Rev. B			Mar'20
Proc. and production for H-beta			
Testing of high-beta			
Delivery of high-beta	42		Oct'20
Proc. and prod. of spare modules			
Testing of spare modules			
Delivery of spare modules	40		Jan'21
Milestone		M8, M15, M24, M29, M34, M35	

8.2. Testing and quality assurance

Only operational, tested, and error-free PCD devices can be sent to our partners and further integrated with LLRF system. Therefore, each module have to be thoroughly checked for problems related to assembly faults, firmware discrepancies and other possible damages. For the purpose of quality control, each module will be provided with a unique serial number and its status and maintenance history will be tracked in a dedicated database. Before releasing the module for installation, and after each non-trivial rework, the module shall be examined for faults. Such examination shall be concluded with preparation of a detailed test report stating if the module is operational.

The prototypes and randomly selected samples from mass production will be tested manually, by qualified DMCS personnel. The tests shall include:

- RTM management controller
- Payload power
- Piezo channel direction selector, disable signal of the power amplifier
- ADC converter and signal conditioning (with function generator)
- DAC converter (with oscilloscope)
- Power amplifier without load, then with capacitor
- Piezo protection circuit (tests for overvoltage, overcurrent)

The manual tests shall be able to detect a vast majority of the possible failures, including not only assembly problems but also those related to the design itself. These are however very time-consuming.

In the pre-production, when the construction becomes mature, there will be no longer need for such a detailed test procedure – faults of some sub-systems will be detected during tests of the higher-level systems dependent on them. Simplification of the test procedure will enable automation of the process, which will significantly reduce its completion time. As the PCD boards can operate both as drivers and as measurement units, it is possible to test operation of one module using another, well tested, one. A help of only a simple passive test load circuit connected between their front-panel interfaces is needed (capacitive load and attenuator).

The test procedure will start with powering the module with the management power and programming the protection microcontroller. Then, the board will be installed in chassis (on the back of RTM carrier AMC) and connected to the test network. Next, the test scripts will be executed to automatically evaluate operation of RMC, channel direction switching, analogue input and output paths and finally the piezo protection circuity. The test-stand software will provide a concise report stating what was tested and informing of any deviations from the expected operation.

The following tests will be performed by the automated test-stand:

1. Tests of pulsed-mode operation – 2 channels, 5 pulses of 1 kHz sine wave, 14 Hz repetition rate, 10 uF load, 180 Vpp, 4 Ohm cable resistance, verification with the oscilloscope
2. Tests of data acquisition from piezo sensor – using signal generator and suitable conditioning circuit
3. Verification of current readout via Zone 3
4. Verification of correct operation of temperature, current and voltage measurement readout via IPMI

5. Verification of the correct operation of piezo protection circuit
6. Tests of cable removal safety interlock
7. Tests of Zone3 piezo driver disable signal

The scope of additional tests will be defined after the evaluation of complete LLRF system production version.

8.3. Acceptance tests

The acceptance tests will be performed after the LLRF system integration phase at NCBJ and are out of the scope of this document.

8.4. Team qualifications

In the following table, we indicate with a tick mark (✔) whether a team member is experienced in a given field. Each column corresponds to one kind of experience.

Mapping of columns to the experience is as follows:

Q1. Experience in design and development of complex control and diagnostic systems and related software technologies;
Q2. Experience in industrial control;
Q3. Experience in participating to a large and distributed software project involving industry and research labs;
Q4. Experience in PXI/PXIe, MTCA.4 and ATCA based systems;
Q5. Experience in industrial computer form factors derived from the PCI-Express specification;
Q6. Experience in electronics, signal conditioning and EMC;
Q7. Experience in CAD design tools;
Q8. Experience in FPGA programming;
Q9. Experience in IPMI standard and MMC firmware development;
Q10. Experience in Linux operating system;
Q11. Experience in high-level software development (C, C++, Java, Python programming languages);
Q12. Experience in the EPICS environment;
Q13. Experience in real-time operating systems (RT Linux, RTEMS, FreeRTOS, VxWorks, QNX);
Q14. Experience in formal test methodology;
Q15. Experience in providing high quality technical documentation;
Q16. Experience in version control systems (SVN, Git)
Q17. Experience in project management tools (Redmine, Jira)
Q18. Experience in tools for bug tracking and continuous integration (Bugzilla, Jenkins)
Q19. Ability to interpret technical documents;
Q20. Ability to work together with ESS team and other related contractors;
Q21. Ability to work within the multi-cultural environment of the ESS project;
Q22. Complete command (oral, writing, reading) of English.

Team qualifications matrix

	Q1	Q2	Q3	Q4	Q5	Q6	Q7	Q8	Q9	Q10	Q11	Q12	Q13	Q14	Q15	Q16	Q17	Q18	Q19	Q20	Q21	Q22
Andrzej Napieralski	✔	✔	✔	✔	✔	✔				✔				✔	✔		✔		✔	✔	✔	✔
Dariusz Makowski	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔			✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
Grzegorz Jabłoński	✔	✔	✔	✔	✔	✔		✔		✔			✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
Aleksander Mielczarek	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔			✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
Piotr Perek	✔	✔	✔	✔	✔				✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
Paweł Plewiński		✔	✔	✔	✔				✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔	✔
Aleksander Szubert		✔	✔	✔	✔	✔	✔		✔	✔			✔	✔	✔	✔	✔	✔	✔	✔	✔	✔

9. System Integration and Installation

The PCD module will be installed in the MicroTCA.4 chassis and connected to AMC carrier module via Zone 3 connector. In addition, the module will require twisted-pair shielded cables with Lemo FFA.0S.304 plugs for the connection with piezo actuators installed a cryo-module and external ±55 V±10%, min. 1.5 Amps power supply connected via cable with Lemo FGG.0B.307 plug.
The Lemo FFA.0S.304 plug should include the interlock protection resistor as described in chapter 5.1.1.

The Lemo plugs, cables and external 19” power supply are out of the scope of TUL-DMCS deliverable within existing in-kind agreement.

The integration of piezo driver modules and installation of LLRF systems will be performed at NCBJ. TUL-DMCS will be involved in development of specification for integration and final tests of the piezo driver during the integration. TUL-DMCS will evaluate the acceptance protocols of installed piezo drivers at ESS and will help to solve problems during the final Site Acceptance Tests.

10. Quality plan and risk analysis

The quality plan will provided for the complete PEG In-Kind contribution (LLRF system for elliptical cavities) [2].

Risk analysis is constantly being performed for piezo driver and it is available in document [3].

Three main identified risks are presented below:

1. Undefined or imprecise requirements for piezo driver (piezo capacitance, operation conditions, i.e. piezo temperature, cable length)
    a. Problem: Difficult to estimate driver power
    b. Countermeasure: Collect and clarify precise requirements, overestimate driver parameters, test with in real conditions in cryostat
2. Unknown excitation signal and piezo control algorithm (signal shape, frequency, energy)
    a. Problem: Difficult to estimate driver power
    b. Countermeasure: Overestimate driver parameters, test with various excitation signals, use higher number of pulses for the signal
3. Lack of cooling in rear side of MicroTCA.4 chassis (RTM device)
    a. Problem: max. power dissipated on RTM in MicroTCA.4 limited to 30 W
    b. Countermeasure: Change PCS architecture (external power supply), high efficiency design, high quality component.

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