



Description:	This document describes the requirements for the Cavity Simulator		
	designed for the tests of the ESS LLRF control system		
Title:	Cavity Simulator Specification		

Authors:	Maciej Grzegrzółka
Co Authors:	Igor Rutkowski
Version:	1.01
Date:	30.05.2017

1. General description

The Cavity simulator is a device used for development and testing of M-Beta and H-Beta LLRF control systems used at the ESS facility in Lund (Sweden). It is also used for the testing of the LLRF control systems components after their installation in the ESS Klystron Gallery.

This device emulates the behavior of a RF cavity coming from the klystron and super conducting cavity based on the output signals coming from the LLRF control system.

The main part of the device is a high performance FPGA processing board connected to a DAC/ADC module. This module is equipped with a set of data converters and a dedicated RF frontend.

The device is controlled remotely by an external PC.

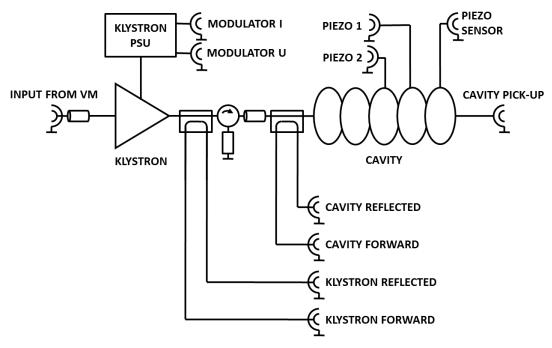
2. Functional specification

2.1. Functionality

The device is used to emulate the accelerating cavity together with a klystron RF power amplifier. Based on the input signals (vector modulator and piezo) coming from the LLRF control system the device simulates following signals

- Klystron input
- Klystron forward
- Klystron reflected
- Cavity forward
- Cavity reflected
- Cavity pick-up
- Klystron PSU modulator I/U
- Piezo Sensor

The block diagram of simulated system is presented below:



This device is simulating following effects:

- Cavity behavior
- Cavity detuning
- Piezo compensation
- Lorentz force detuning
- Beam current

- Microphonics
- Quench
- Mechanical modes
- Coupler heating
- Ponderomotive effect
- Klystron non-linearity
- Klystron PSU modulator influence

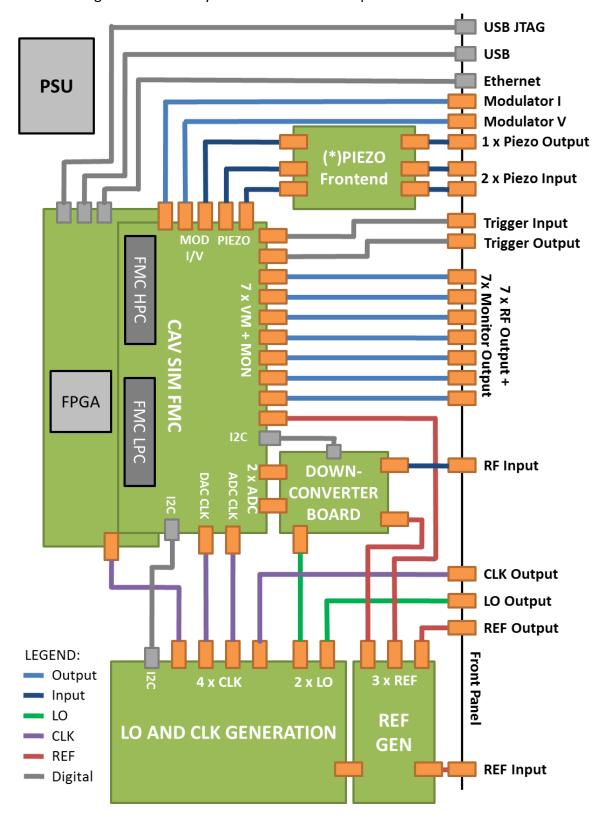
The most important parameters of the simulation can be set on-line by the control software.

The software tools for integration of the device with other systems, like e.g. LLRF system test stand, are provided. Their functionality is further described in section 4.

The internal reference signal generator is also provided inside the device.

2.2. Block diagram

The block diagram of the cavity simulator hardware is presented below.



2.3. Control Interfaces

Name	Connector Type	Description
USB	USB B	Cavity Simulator USB control interface
USB JTAG	USB B	FPGA JTAG USB connector
Ethernet	RJ45	Cavity Simulator Ethernet control interface

2.4. Analog Outputs

Name	Connector	Level	Description
	Туре		
LO out	SMA (50Ω)	0 – 5 dBm	LO signal outputs
CLK out	SMA (50Ω)	0 – 5 dBm	LO signal outputs
REF out	SMA (50Ω)	0 – 5 dBm	CLK signal outputs
CAV out	SMA (50Ω)	0 – 15 dBm	Cavity pick-up signal
CAV_FOR out	SMA (50Ω)	0 – 15 dBm	Cavity forward signal
CAV_RFL out	SMA (50Ω)	0 – 15 dBm	Cavity reflected signal
KLY_IN out	SMA (50Ω)	0 – 15 dBm	Klystron input signal
KLY_OUT out	SMA (50Ω)	0 – 15 dBm	Klystron output signal output
KLY_REF out	SMA (50Ω)	0 – 15 dBm	Klystron reflected signal output
CAV monitor out	SMA (50Ω)	-10 – 5 dBm	Cavity pick-up signal monitoring output
CAV_FOR monitor out	SMA (50Ω)	-10 – 5 dBm	Cavity forward signal monitoring output
CAV_RFL monitor out	SMA (50Ω)	-10 – 5 dBm	Cavity reflected signal monitoring
O/W_IW E Monitor out			output
KLY_IN monitor out	SMA (50Ω)	-10 – 5 dBm	Klystron input signal monitoring output
KLY_OUT monitor out	SMA (50Ω)	-10 – 5 dBm	Klystron output signal monitoring output
KLY_REF monitor out	SMA (50Ω)	-10 – 5 dBm	Klystron reflected signal monitoring
TRET_INET INIONITION OUT	SIVIA (SULL)		output
Trigger out	SMA (50 Ω)	0 – 15 dBm	Synchronization signal output
MOD_I out	SMA (50Ω)	± 1 V	Modulator I output
MOD_V out	SMA (50Ω)	± 1 V	Modulator V output
Piezo out	Lemo	± 1 V	Piezo sensor output

2.5. Analog inputs

Name	Connector Type	Level	Description
REF in	SMA (50Ω)	5 – 15 dBm	Main Reference input
VM in	SMA (50Ω)	0 – 15 dBm	Input from the vector modulator
Trigger in	SMA (50 Ω)	0 – 15 dBm	Synchronization signal input
Piezo IN 1	Lemo	± 100 V	Piezo input 1
Piezo IN 2	Lemo	± 100 V	Piezo input 2

3. Other requirements

Name	Value
Reference signal frequency	704 MHz
Clock signal frequency	50 – 120 MHz
LO signal frequency	20 – 80 MHz
Supply Voltage	230 V AC
Power Consumption	< 250 W
Chassis	2U 19"

4. Software

Two software tools are provided to control the cavity simulator:

- Standalone application
- API for integration with other systems

4.1. Standalone application

The standalone application give the user the ability to control the device through graphical user interface. The application will support Microsoft Windows and Linux x86 operating systems.

4.2. API

The Cavity Simulator API is a tool dedicated for integration in more complex system where automated control over the device is needed. This tool allows the user to easily integrate the device inside his test system.

The detailed description of this tools, including list of methods and parameters, will be presented in another document, prepared after the first prototype of the Cavity Simulator is presented.