PDRs of LLRF parts: LO-generation

Igor Rutkowski

Warsaw University of Technology

30.05.2017

Table of Contents

Introduction

Introduction

- Field detection at ESS: downconversion to intermediate frequency, sampling, and conversion to digital.
- Low-phase noise clock and heterodyne/local oscillator (LO) signals needed.
- MTCA.4 platform.
- Clock and LO generation on RTM.
- One board feeds one system located in the same crate and three other neighboring systems.

Frequencies

Reference: 704.42 MHz

Frequency ratios

- Clock to reference = $\frac{1}{6}$ (117.403(3) MHz)
- LO to reference = $\frac{29}{28}$ or $\frac{23}{22}$ (729.58 or 736.44 MHz)

Frequency synthesizers classification

- Direct Analog
- Direct Digital
- Indirect Digital

DDS: Binary frequency tuning word

LO Synthesis and Distribution

Requirements

- Frequency: Reference+(25.16 or 32.02) MHz
- Number of outputs: 4 (+1 monitoring)
- Output power: +15 dBm ±1 dB
- Output return loss: <-14 dB
- Phase noise (revised)

Offset (Hz)	Phase noise $\left(\frac{dBc}{\sqrt{(Hz)}}\right)$
10	-90
100	-110
1k	-125
10k	-140
100 k	-149
1M	-152
10 M	-154

PLL Selections

Non-electrical Considerations

- mechanical vibrations present
- physical dimension constraints

Integrated silicon VCOs preferred

PLL Optimization

LMX2592: very good normalized noise floor, integral and fractional divider.

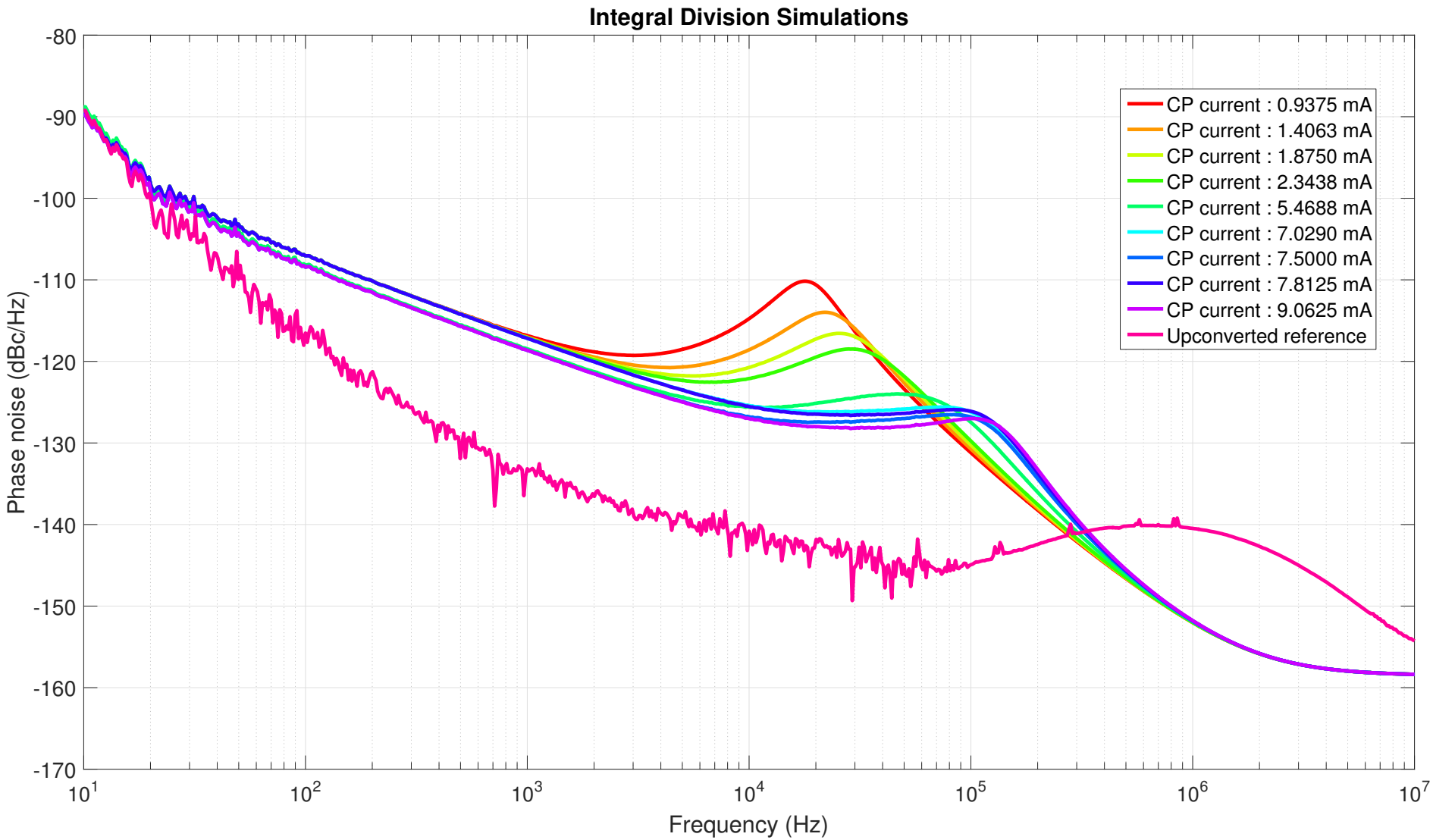
$$PLL_{flat} = PLL_{FOM} + 20 * log_{10}(\frac{f_{VCO}}{f_{pd}}) + 10 * log_{10}(\frac{f_{pd}}{1Hz})$$

$$PLL_{flicker}(f_{offset}) = PLL_{flickernorm} + 20 * log_{10}(\frac{f_{VCO}}{1GHz}) - 10 * log_{10}(\frac{f_{offset}}{10kHz})$$

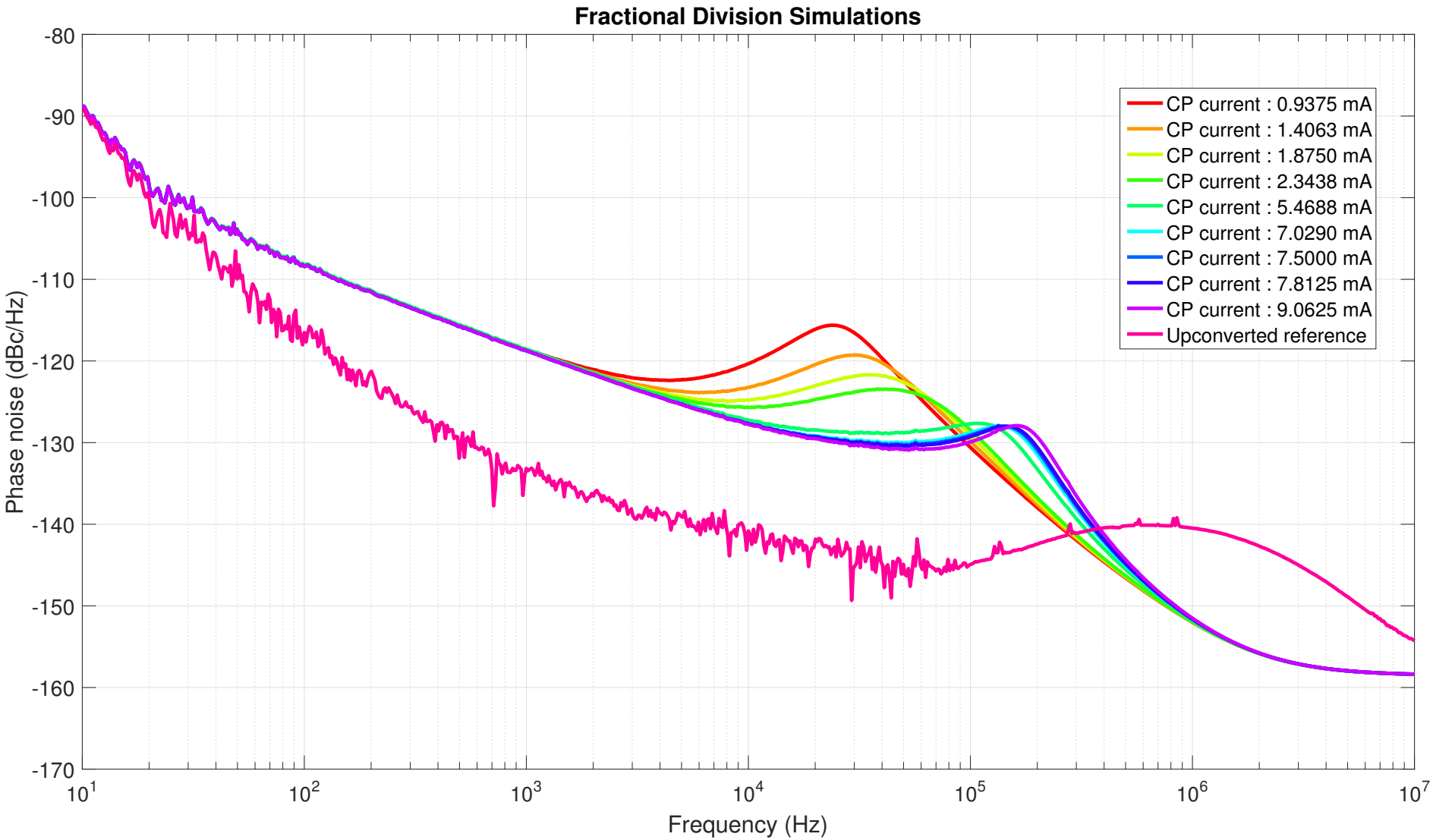
Frequencies of both VCO and phase detector should be high.

Simulations and measurements for 704 MHz to 726 MHz.

PLL Simulations



PLL Simulations (cont.)

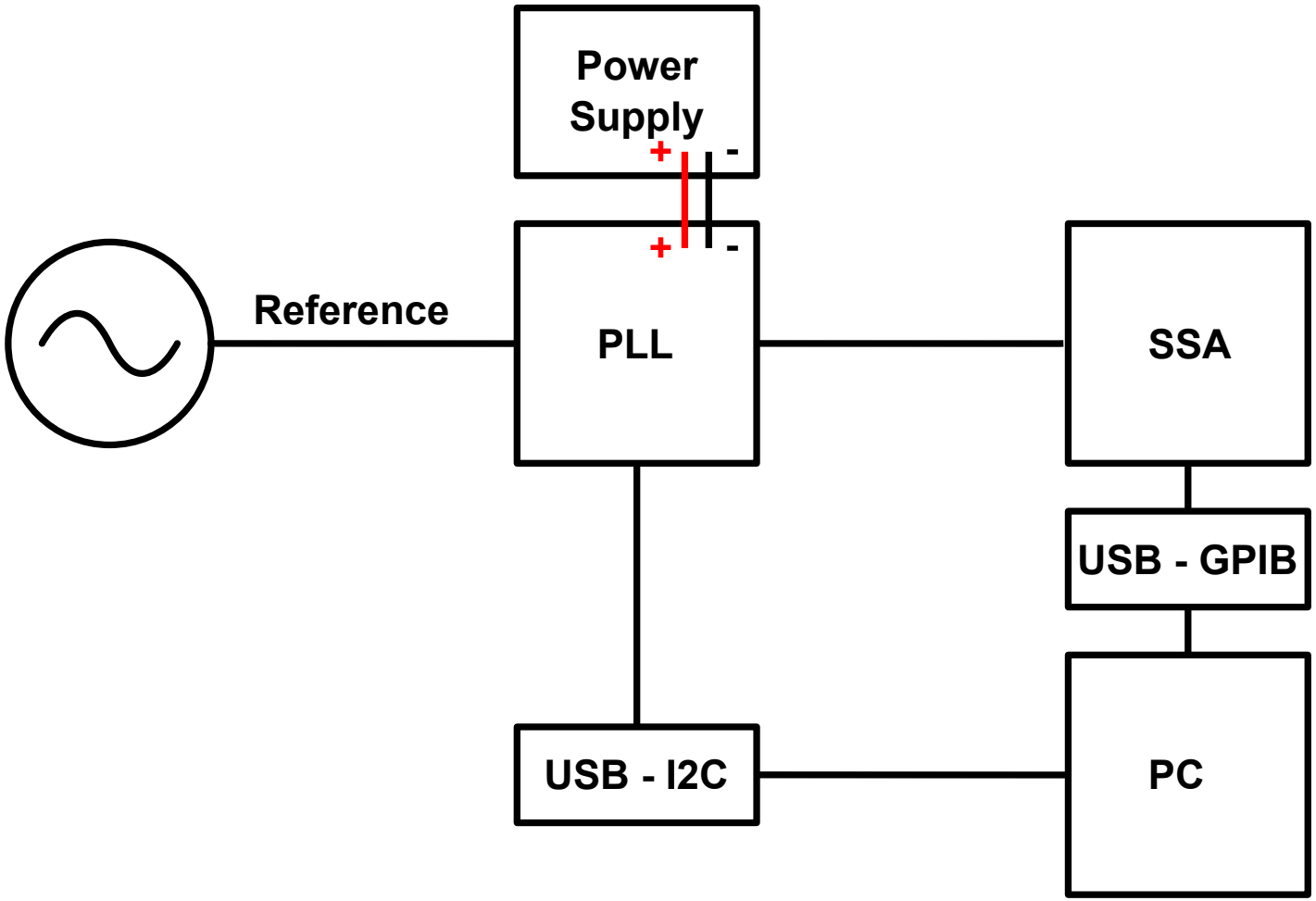


PLL Simulations (cont.)

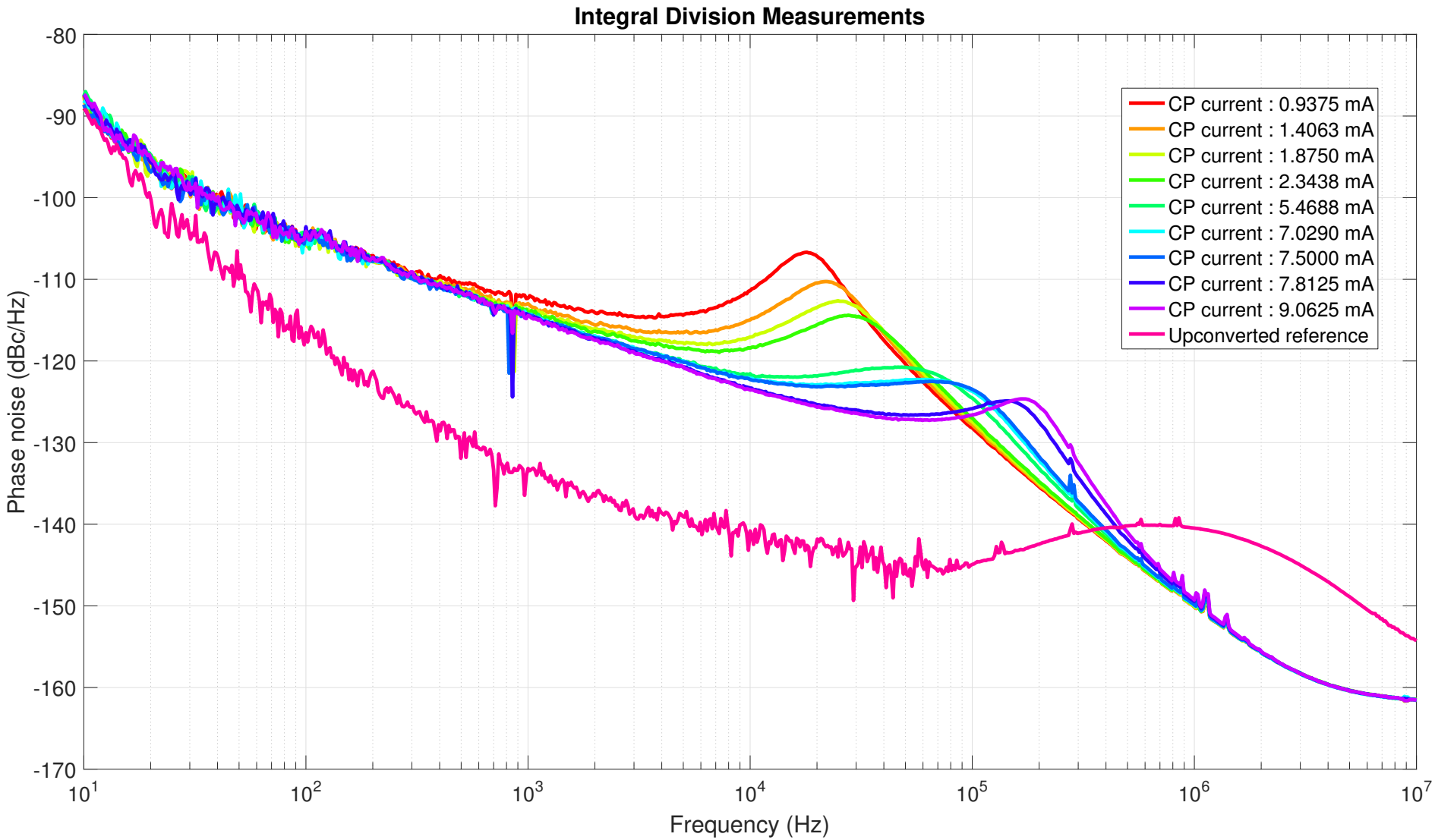
Simulated absolute jitter of two PLL configurations in each frequency decade. The charge pump current was select to minimize the total jitter (in the 10 Hz 10 MHz band).

Jitter (fs)	Start Offset	10	100	1k	10k	100 k	1 M	10
Config	End Offset	100	1k	10k	100 k	1 M	10 M	10 M
Int Div	9.0625 mA	25.7	17.5	18.4	38.5	40.1	12.8	67.5
Frac Div	7.029 mA	27.7	17.4	17.8	31.3	42.4	12.8	65.8

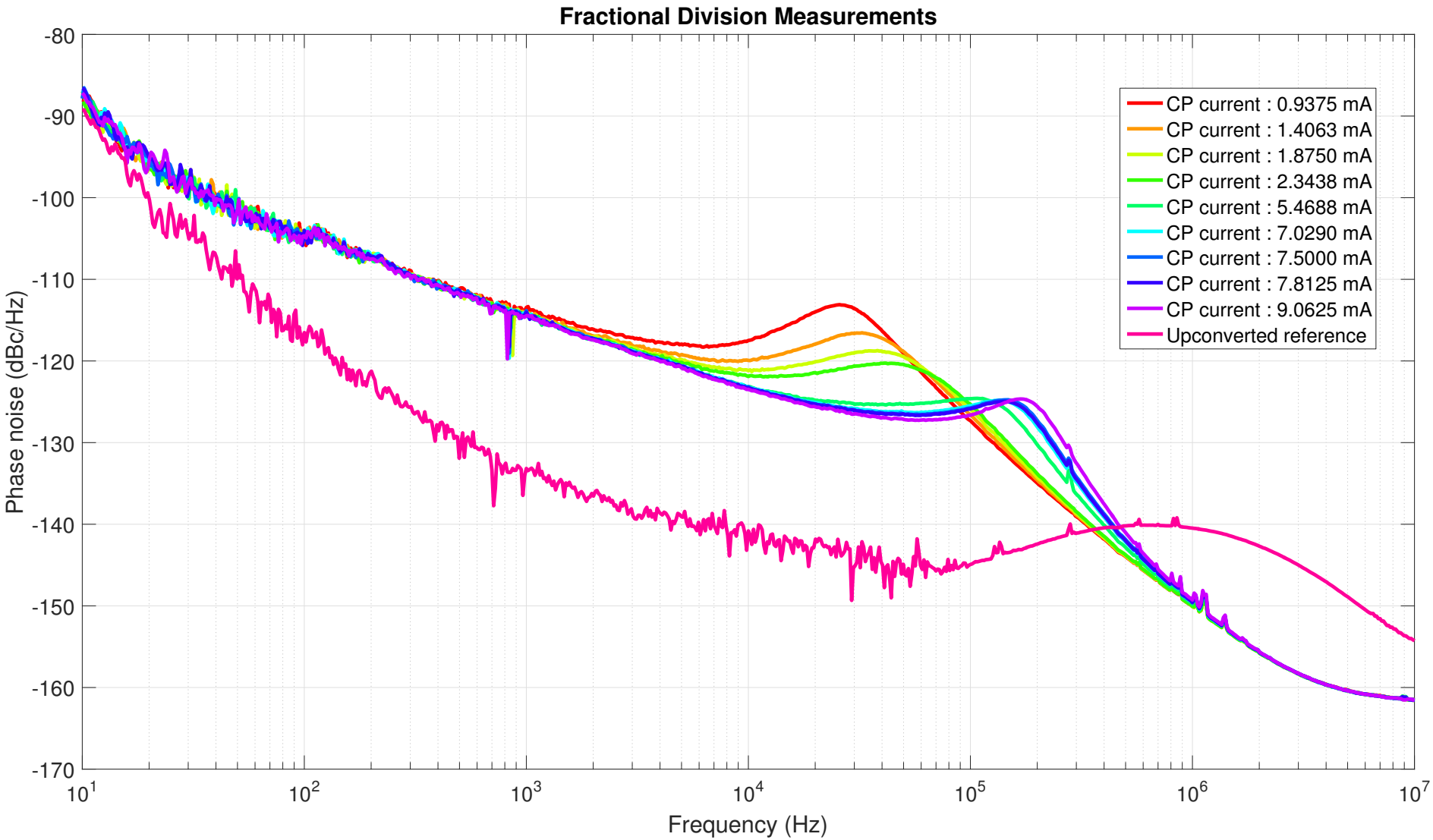
PLL Measurements Setup



PLL Measurements



PLL Measurements (cont.)

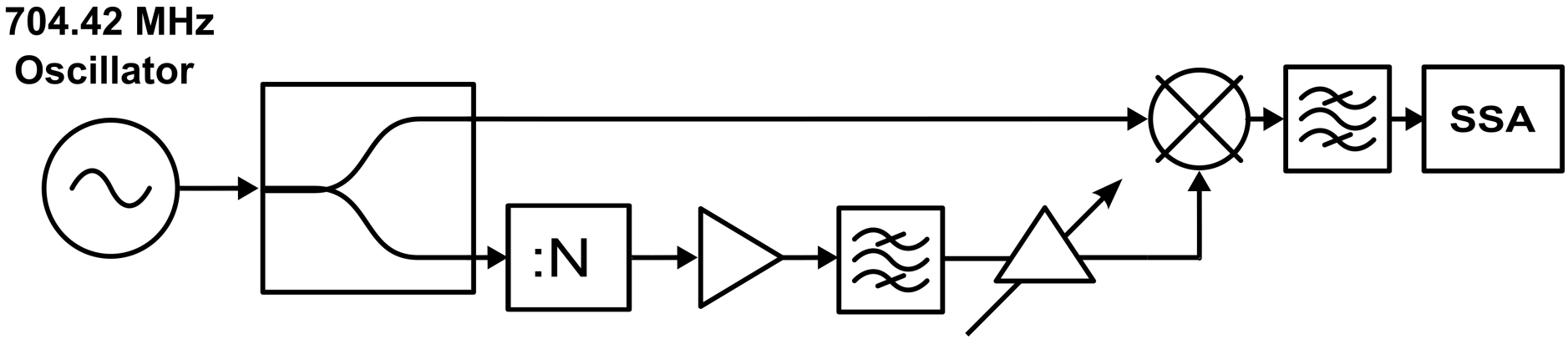


PLL Measurements (cont.)

Measured absolute jitter of two PLL configurations in each frequency decade. The charge pump current was select to minimize the total jitter (in the 10 Hz 10 MHz band).

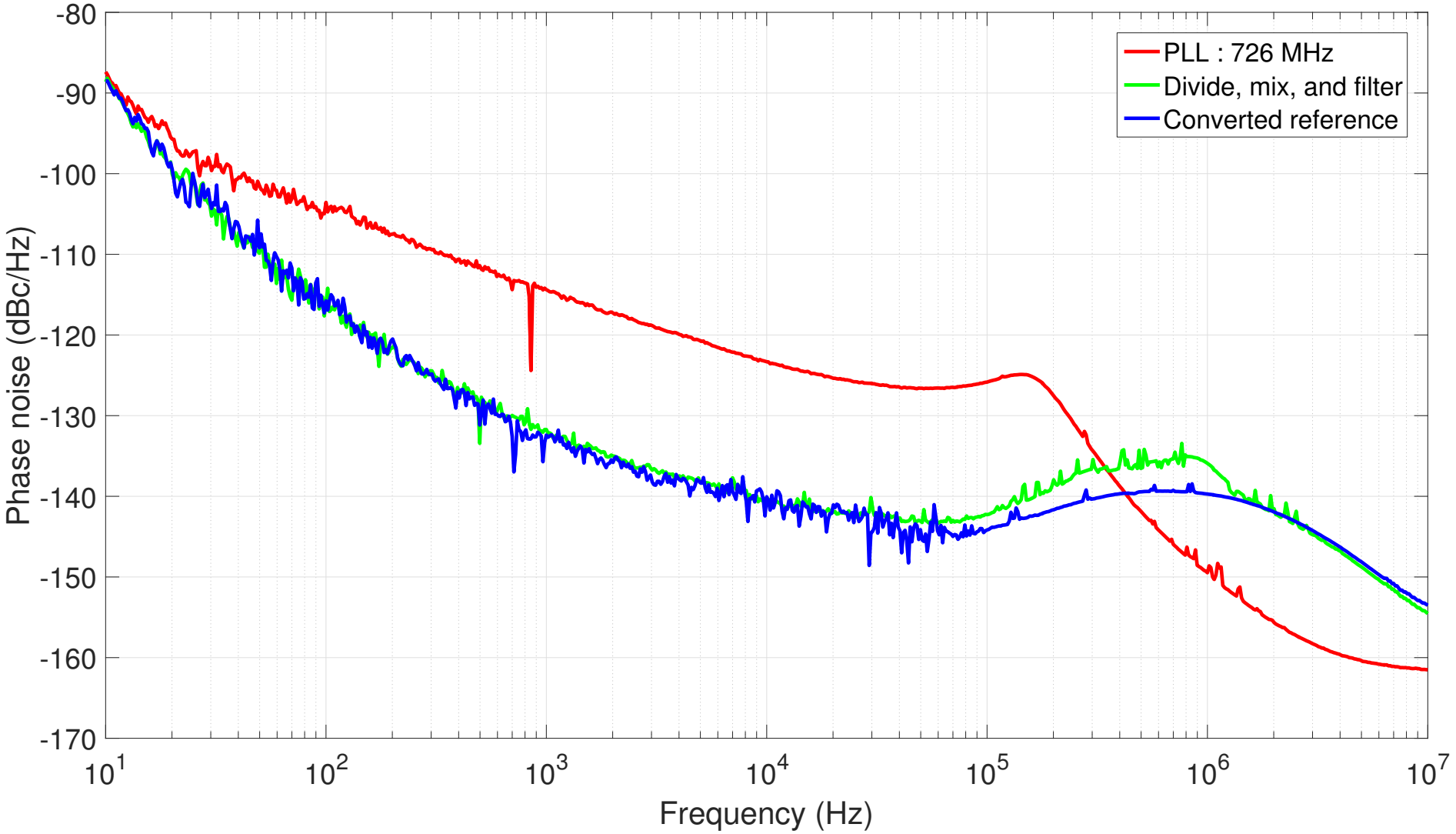
Jitter (fs)	Start Offset	10	100	1k	10k	100 k	1 M	10
Config	End Offset	100	1k	10k	100 k	1 M	10 M	10 M
Int Div	7.8125 mA	34.8	28.0	29.6	46.5	63.2	11.6	95.7
Frac Div	7.8125 mA	35.8	28.0	29.7	46.4	62.3	11.6	95.6

Direct Analog Scheme Preliminary Evaluation Setup



Component name	Manufacturer and model
Oscillator	Holzworth HSX9004A
Frequency divider	Analog Devices AD9515
IF Signal Amplifier	TriQuint AH202F
LO Band-pass filter	K&L D5BT-750/1500-5-N/N-GRI
Mixer	MiniCircuits HJK-272H
Signal Spectrum Analyzer	Agilent E5052B

LO Synthesis Scheme Comparison



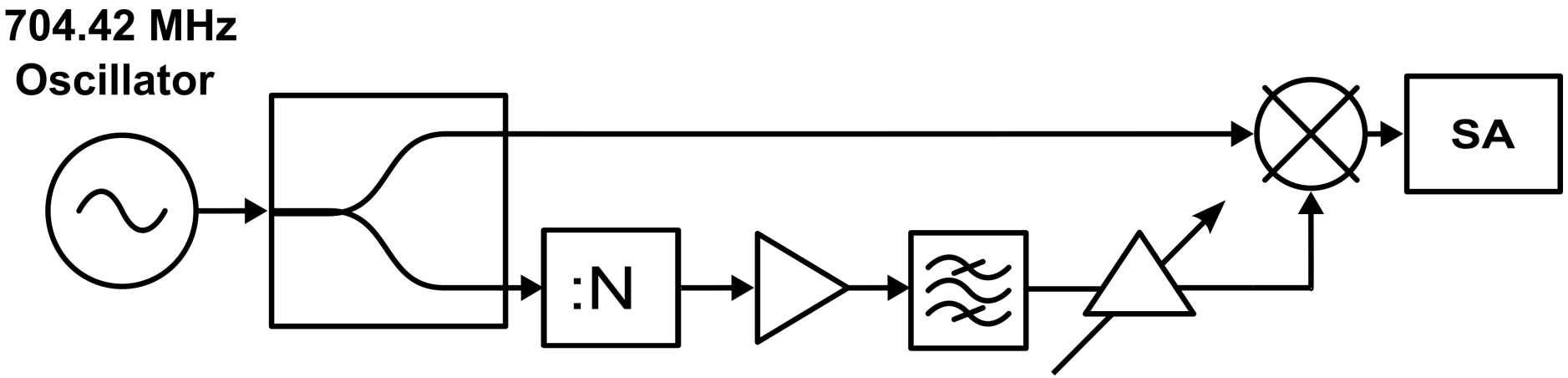
Mixer Selection

Criteria

- Spectral characteristics.
- Isolation.
- Power level.

ADE-R5LH+ selected due to high isolation.
Nominal power level: +10 dBm.

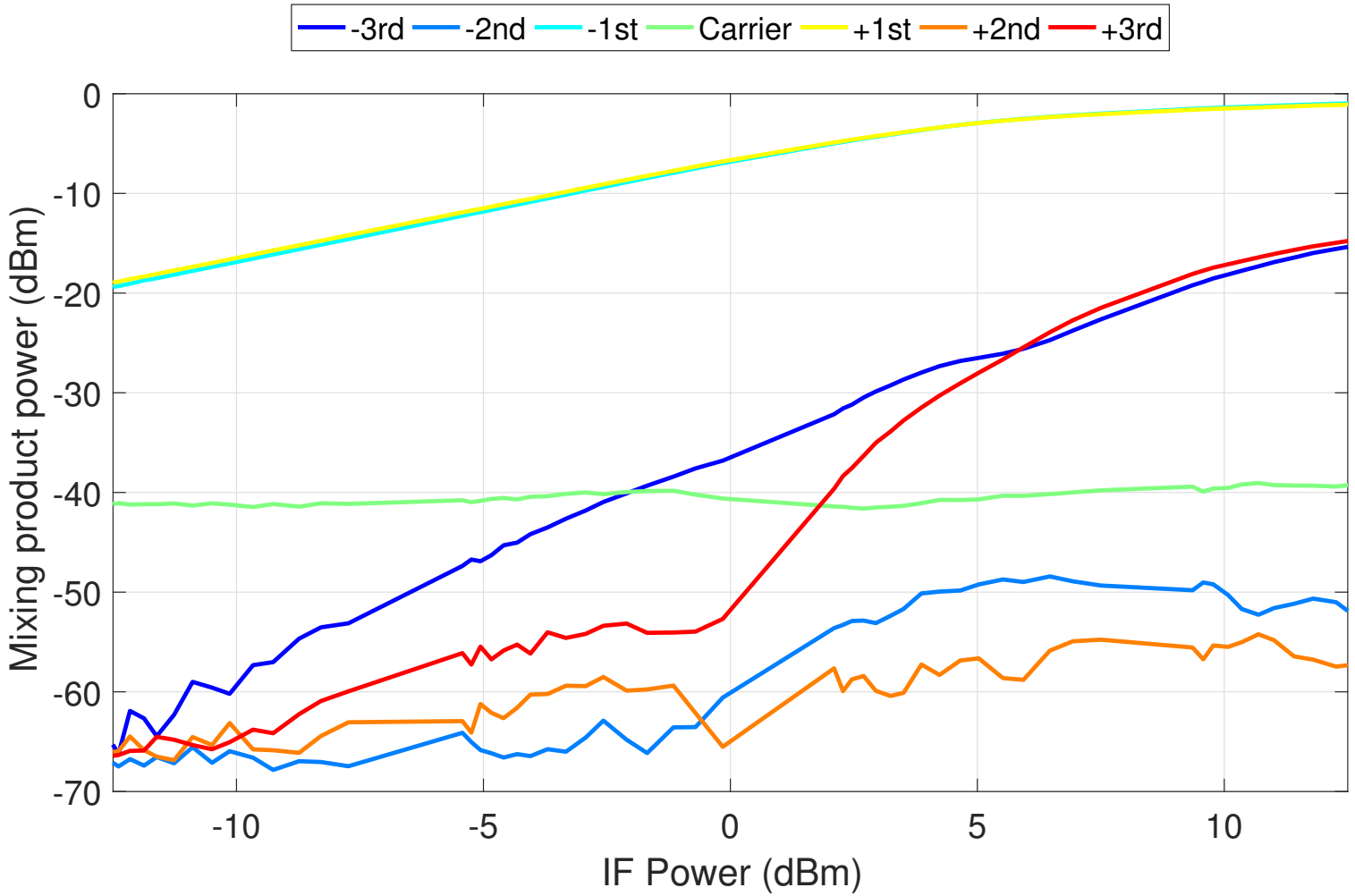
Mixers Power Spectrum Test Setup



Component name	Manufacturer and model
Oscillator	Agilent E8257D
Frequency divider	Analog Devices AD9515
IF Signal Amplifier	TriQuint AH202F
IF Band-pass filter	MiniCircuits SXBP-29+
LO Band-pass filter	K&L D5BT-750/1500-5-N/N-GRI
Programmable attenuator	Analog Devices HMC472ALP4E
Mixer	ADE-R5LH+
Spectrum Analyzer	Agilent N9030A PXA

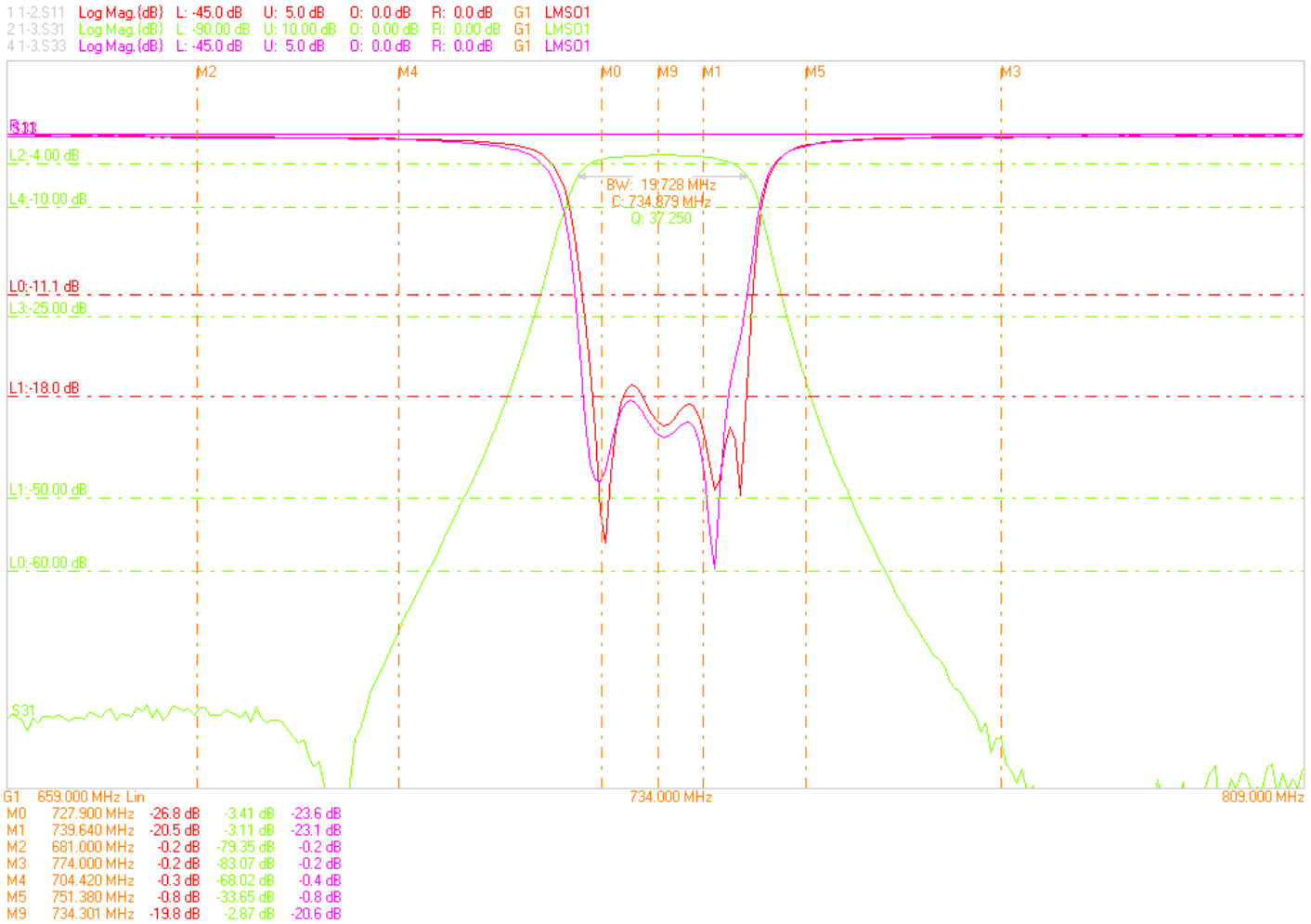
Mixers Power Spectrum

Spectral components at the mixers output. LO Power = +8.1 dBm, IF = 32.02 MHz.

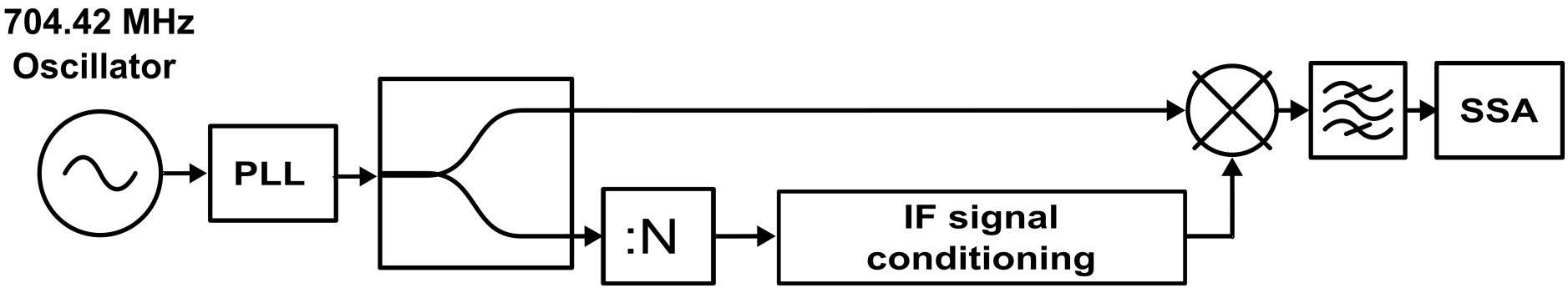


Band-pass Filter

Start Frequency (MHz)	598.76	633.98	669.20	704.42	751.38	774.86
Stop Frequency (MHz)	633.98	657.46	680.94	704.42	774.86	810.08
Min. attenuation (dB)	50	10	60	25	10	50



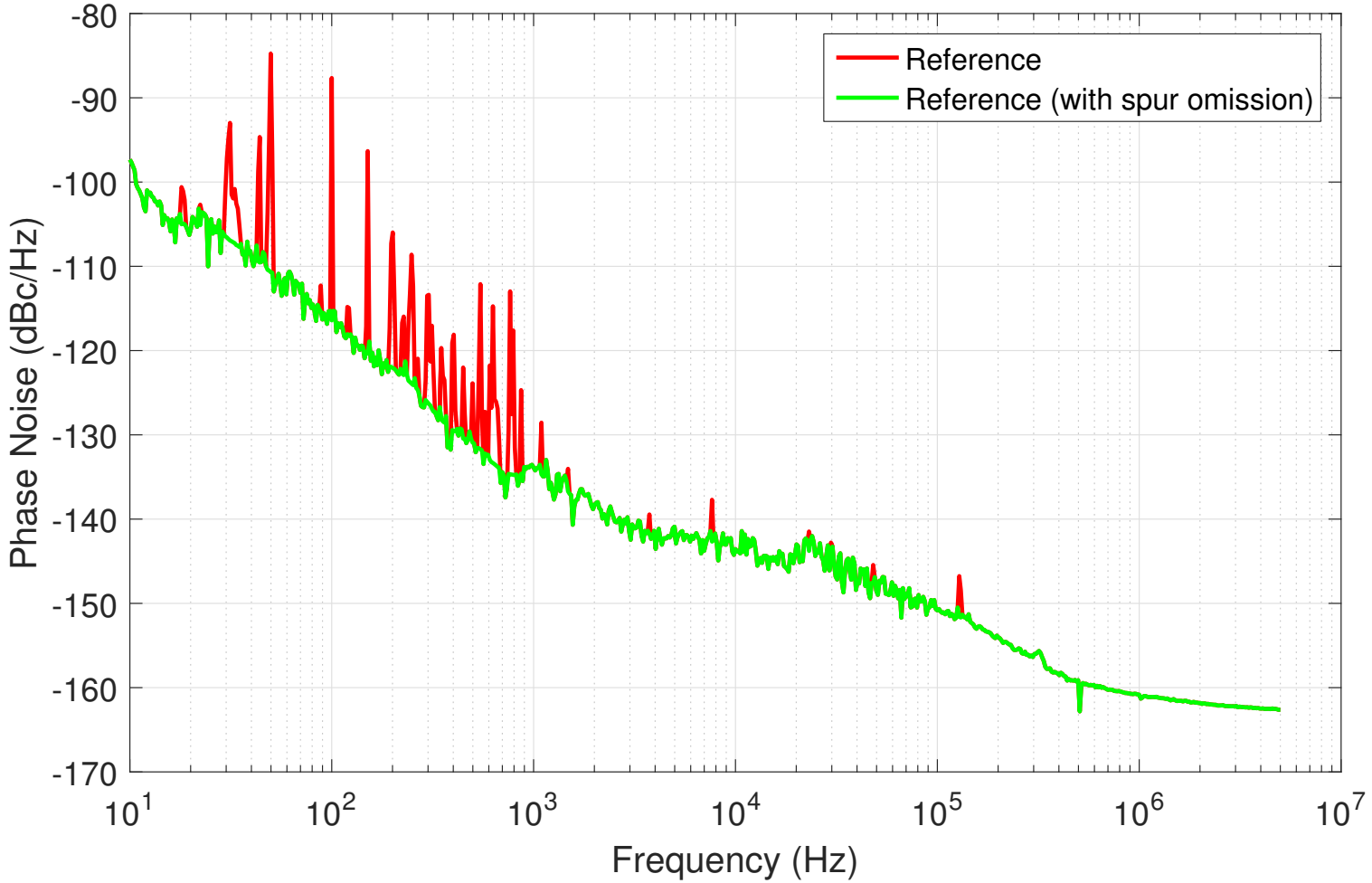
LO and IF Phase Noise Measurement Setup



Component name	Manufacturer and model
Oscillator	Agilent E8257D
Frequency divider	Analog Devices AD9515 or AD9508
IF Signal Amplifier	TriQuint AH202F
LO Band-pass filter	K&L D5BT-750/1500-5-N/N-GRI
Mixer	MiniCircuits ADE-R5LH+
Signal Spectrum Analyzer	Agilent E5052B

Reference for Phase Noise Measurements

Measured phase noise spectrum (with and without spur omission) of the designed PLL-based reference synthesizer.



IF Divider

High division ratio requiered : 22 or 28.

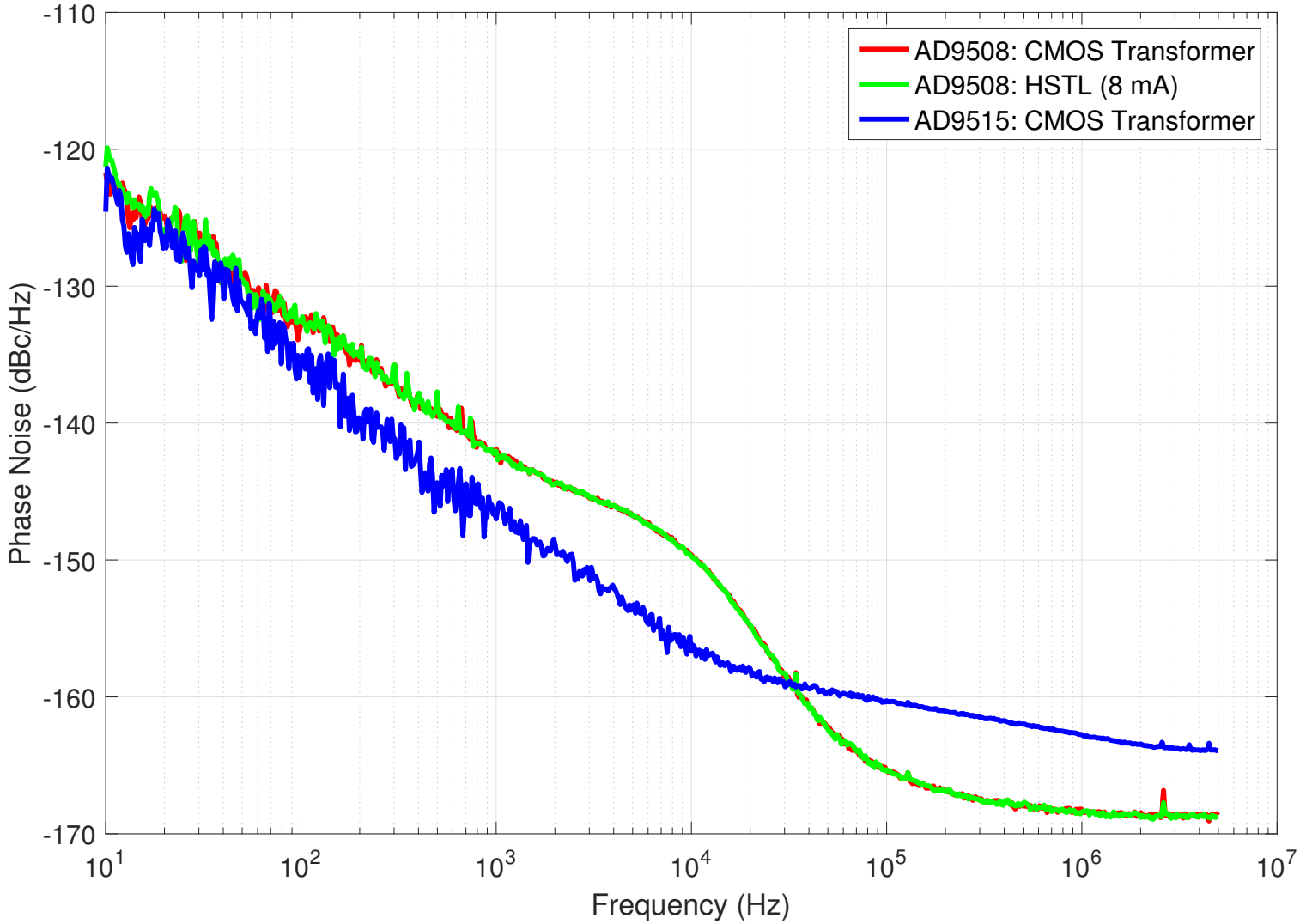
Considered devices

- AD95XX by Analog Devices
- Signaling standards: CMOS, HSTL, LVPECL, and LVDS
- Two types of dividers: 1-32 and 1-1024
- Representative models: AD9508 and AD9515

AD9508 selected because of lower total jitter in the 10 Hz - 5 MHz band (see the following slides).

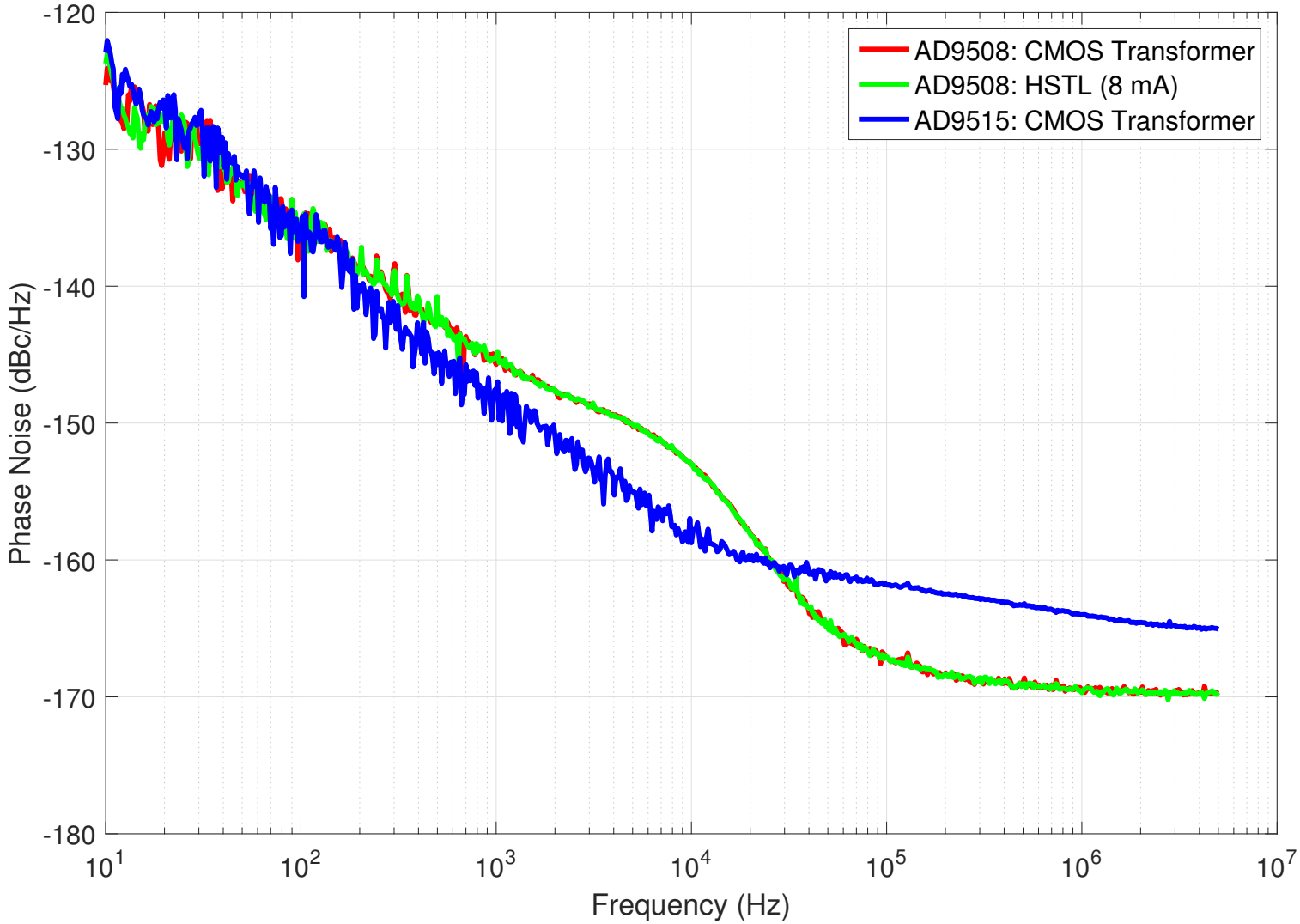
IF Divider PN Comparison

Divide-by-22



IF Divider PN Comparison (cont.)

Divide-by-28



IF Amplifier

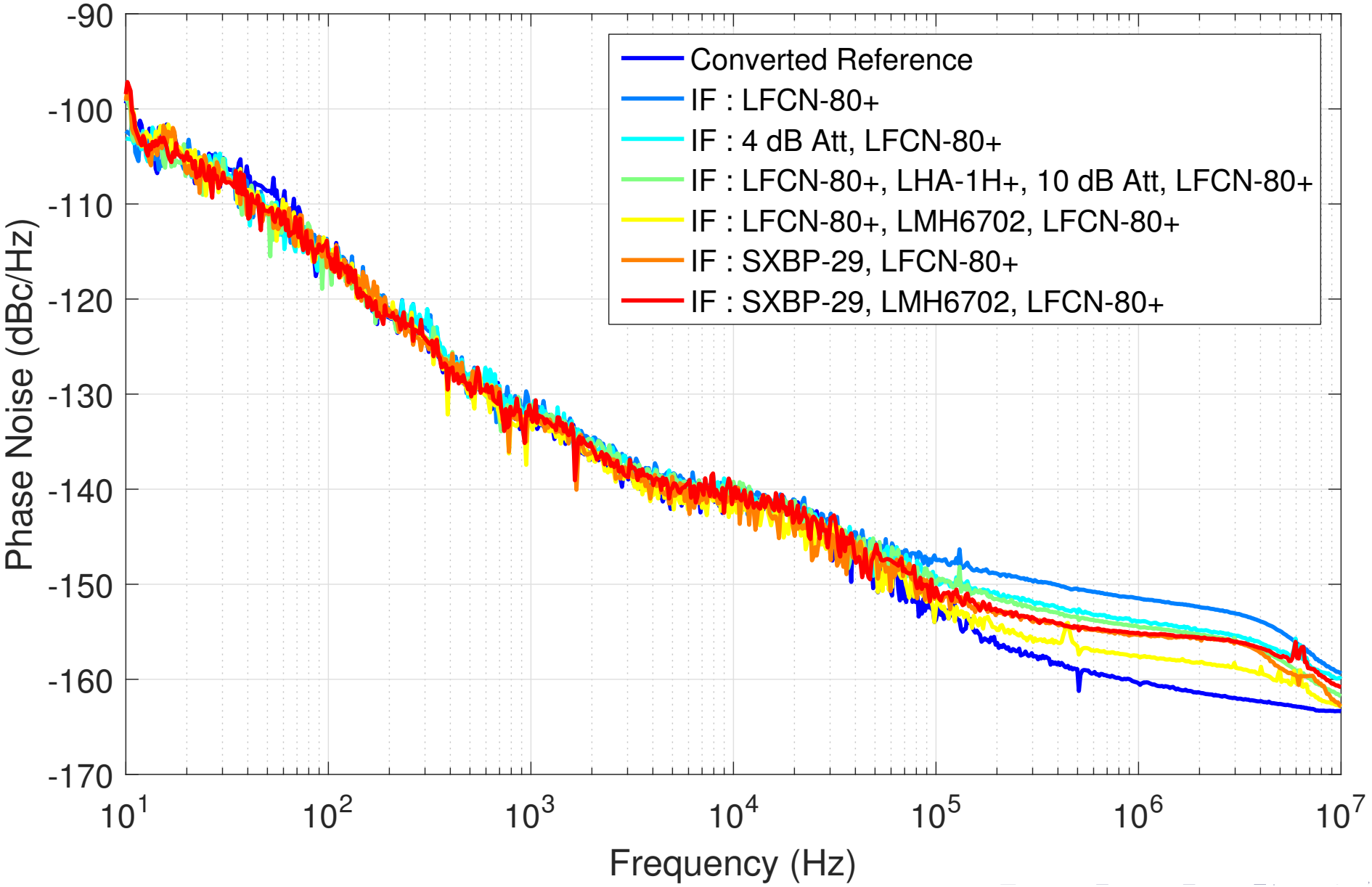
AD9508 output power: +7.5 dBm, desired power: +12 dBm

Characteristics

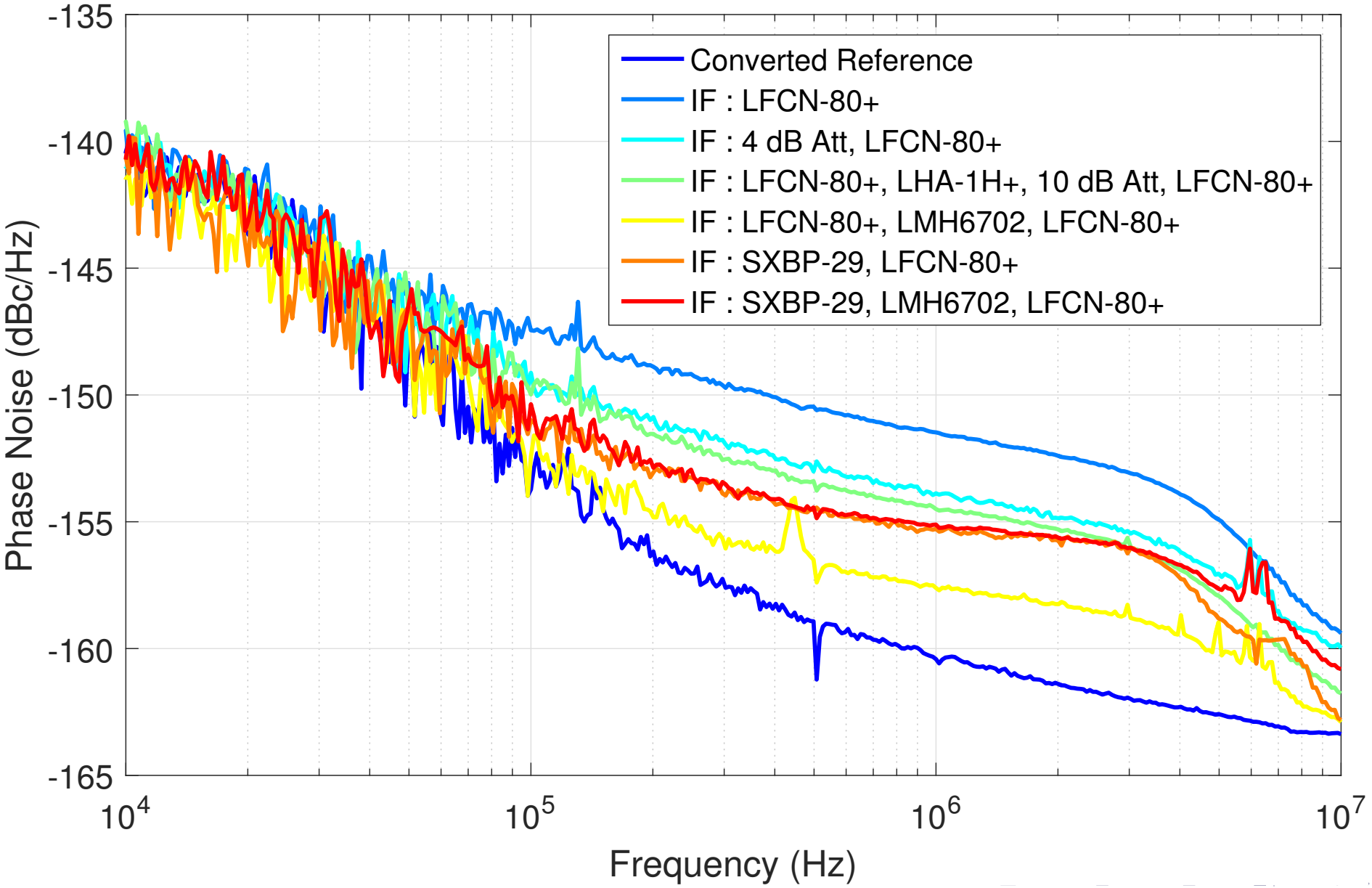
- Low gain (+5 dB)
- Low noise

Integrated wideband amplifiers considered, but performed poorly. The LMH6702 operational amplifier selected due to best PN performance (see the following slides).

IF (32.02 MHz) Amplifier PN Comparison



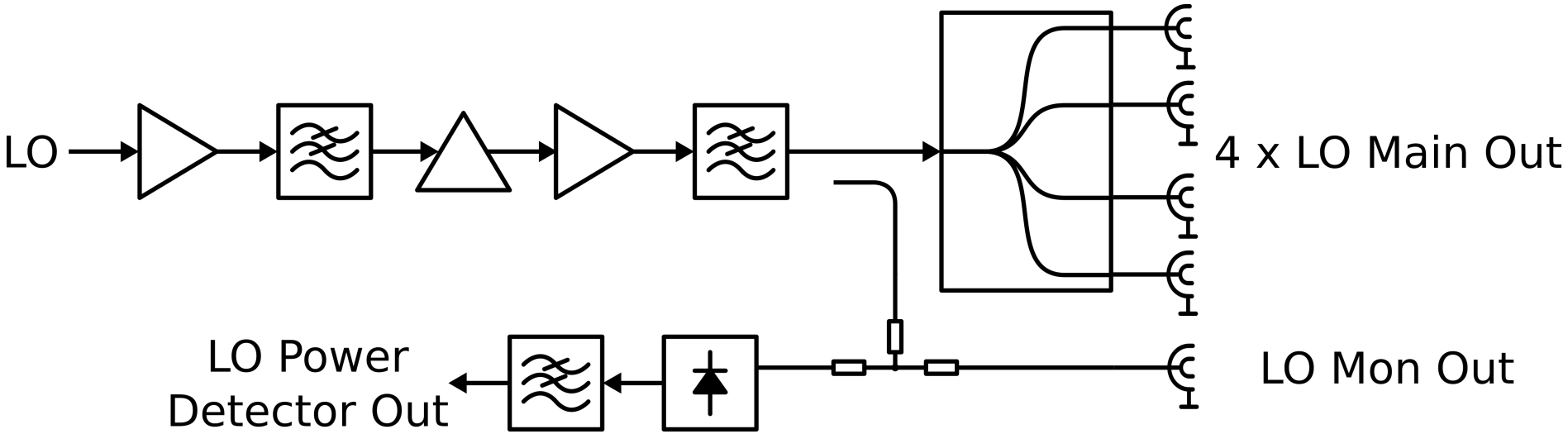
IF (32.02 MHz) Amplifier PN Comparison (zoom-in)



LO Signal Distribution

- Filter's output power: -5 dBm.
- Board's output power: 4 x +15 dBm.
- Total power (inc. losses): +23 dBm.
- Popular medium-power integrated amplifiers: insufficient gain and maximum output power.
- Two stage amplifier proposed.
- Coupler, low-pass filter, and power splitter selected.

Block diagram of LO Signal Distribution



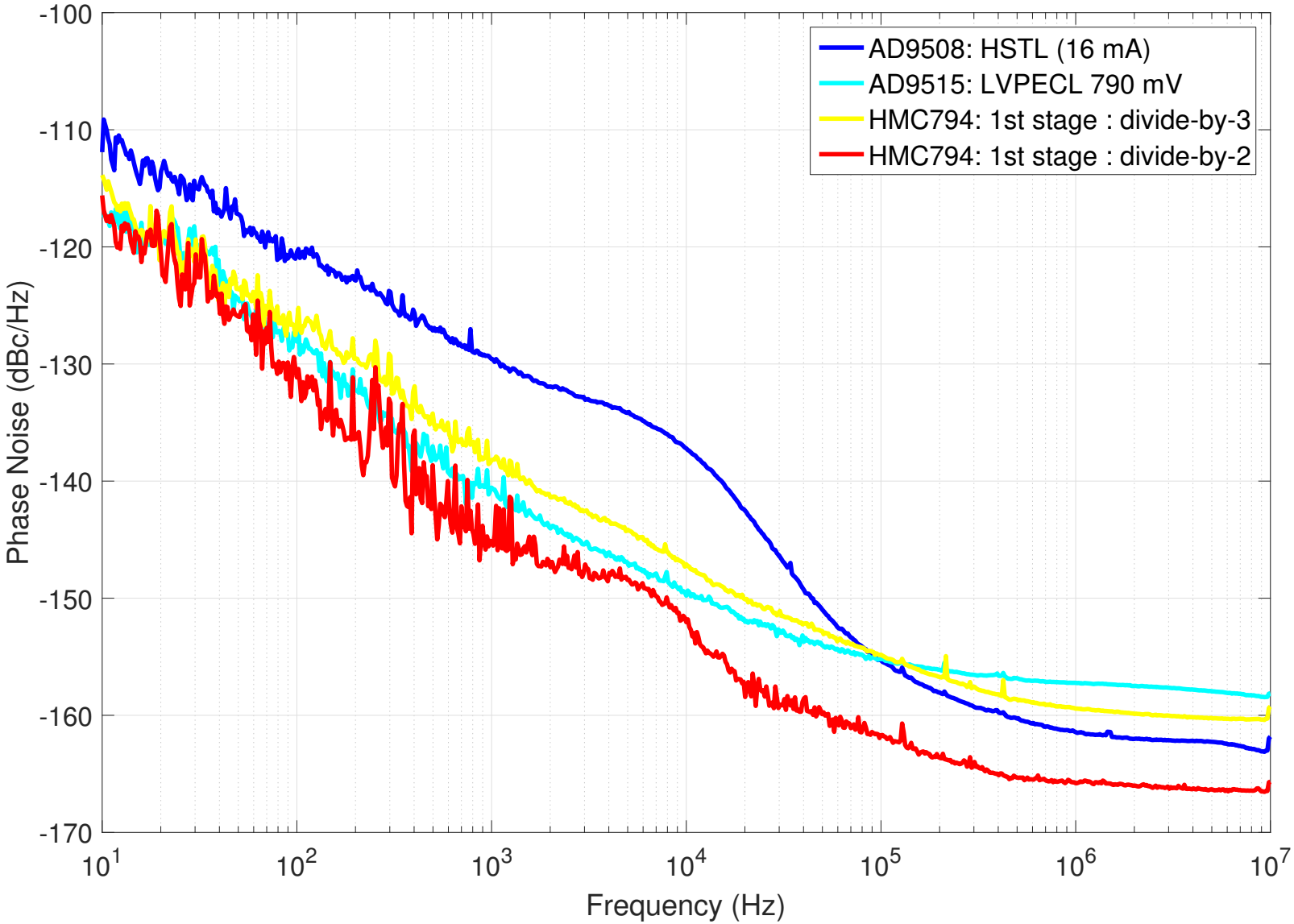
Clock Frequency Synthesis and Distribution

Requirements

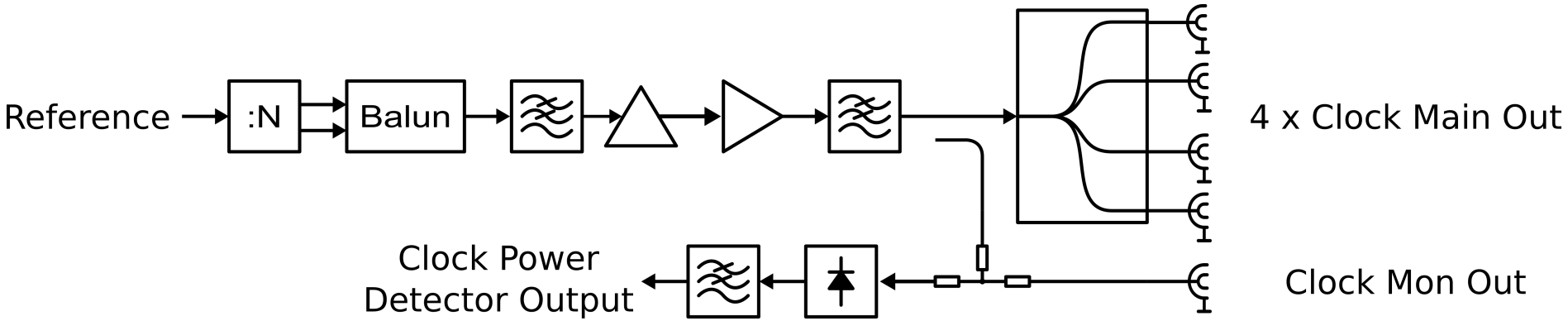
- Frequency: 117.403(3) MHz
- Number of outputs: 4 (+ 1 monitoring)
- Output power (each): +15 dBm ±1 dB
- Output return loss: <-14 dB
- Sine wave
- Phase noise (revised)

Offset (Hz)	Phase noise ($\frac{dBc}{\sqrt{(Hz)}}$)
10	-106
100	-120
1k	-134
10k	-145
100 k	-151
1M	-151
10 M	-153

Comparison of Frequency Dividers for Clock



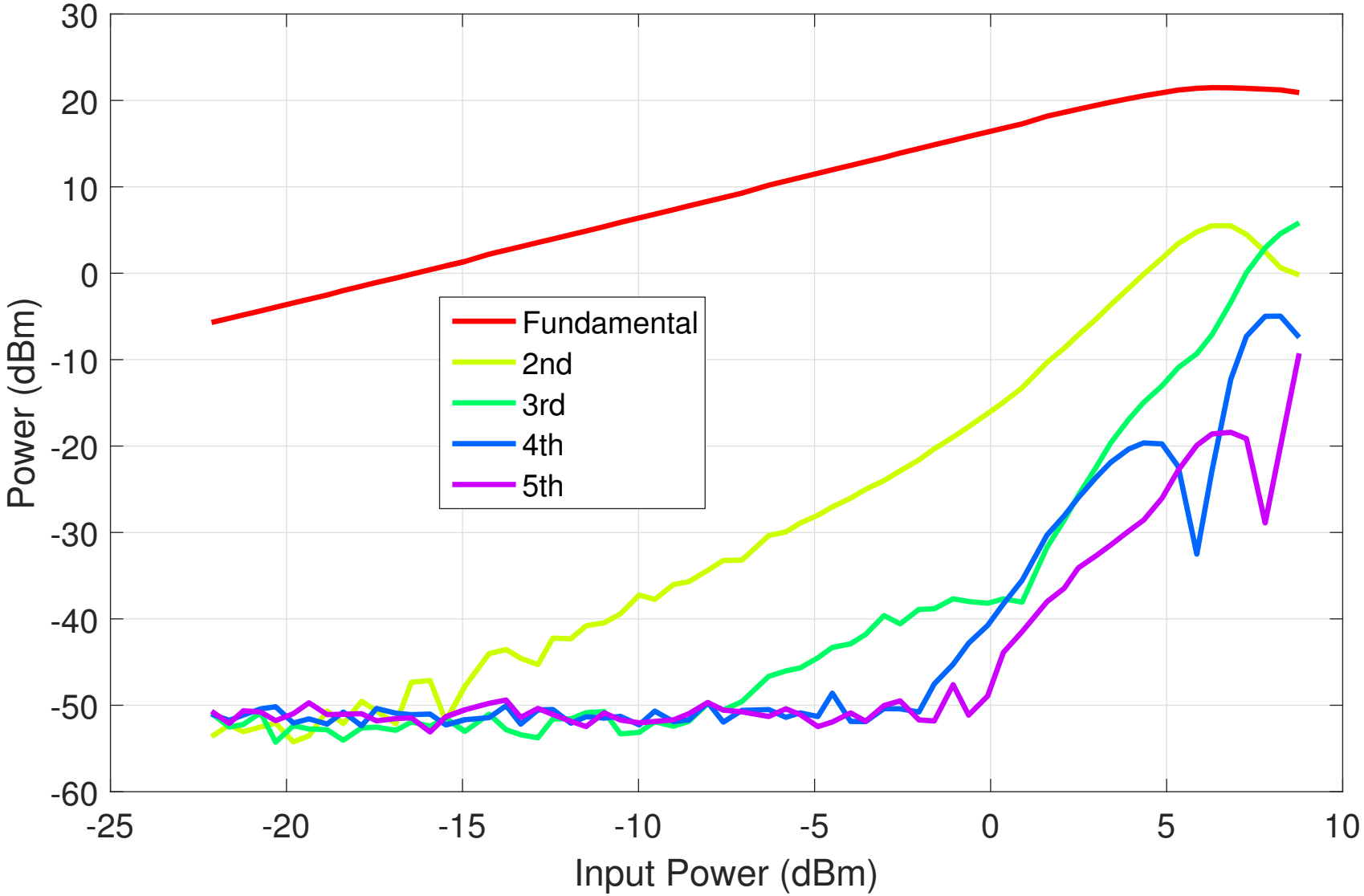
Clock Signal Distribution



- Dividers' output power: +10 dBm.
- Board's output power: 4 x +15 dBm.
- Total power (inc. losses): +22 dBm.
- Coupler, low-pass filter, and power splitter selected.
- Amplifier selection criteria: spectrum and phase noise

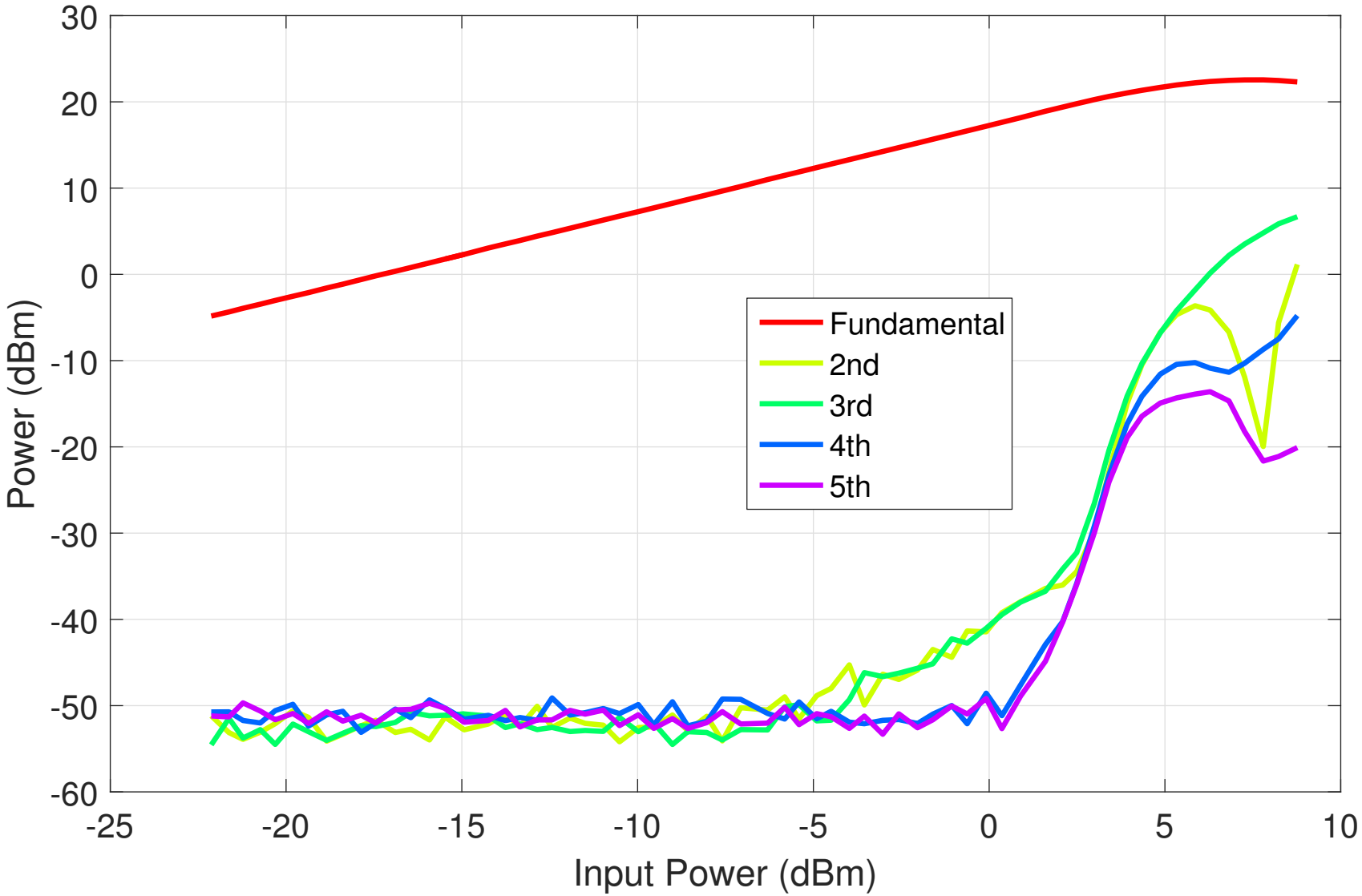
Spectrum at Clock Signal Amplifier's Output

ADL5530

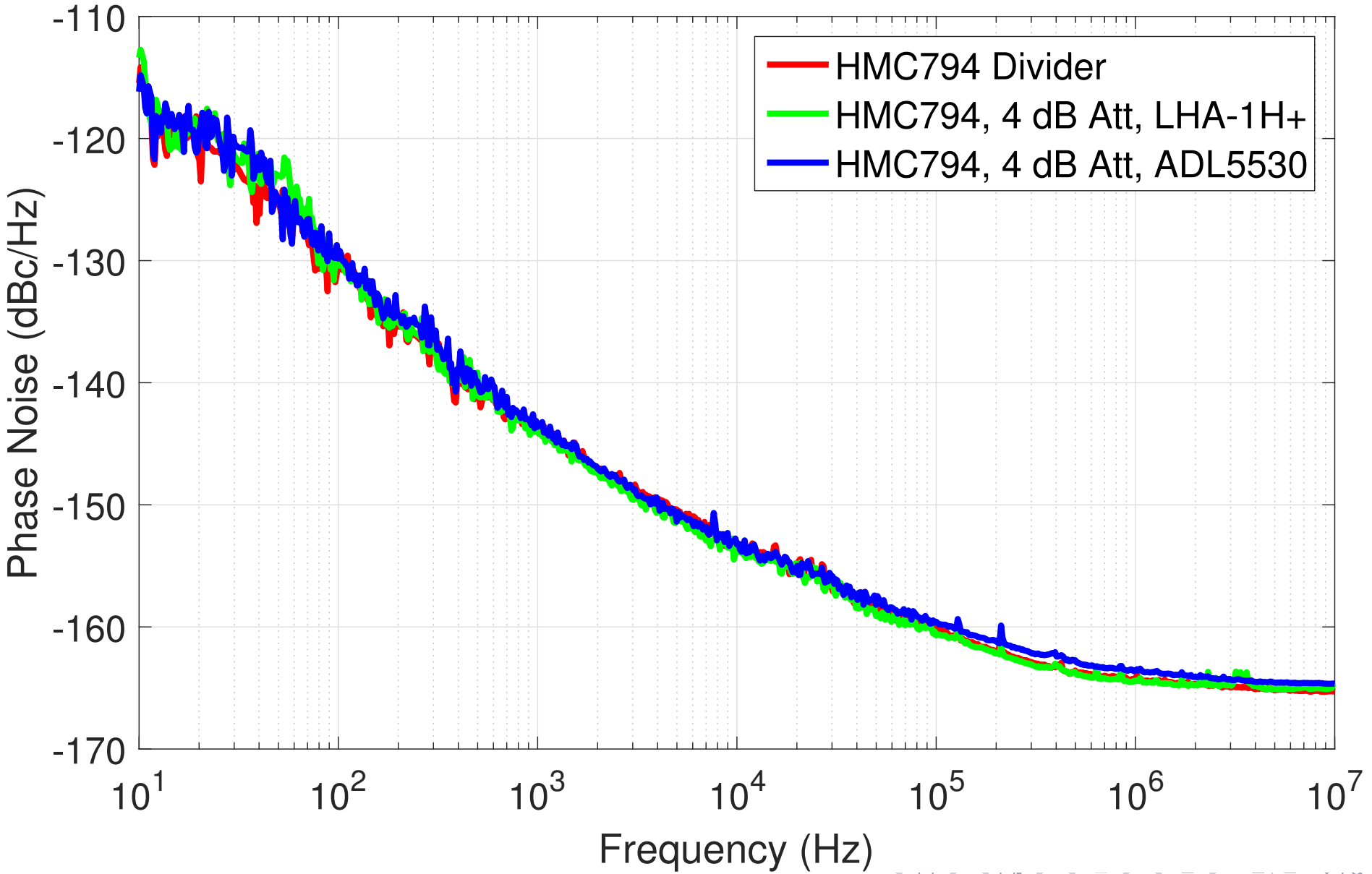


Spectrum at Clock Signal Amplifier's Output

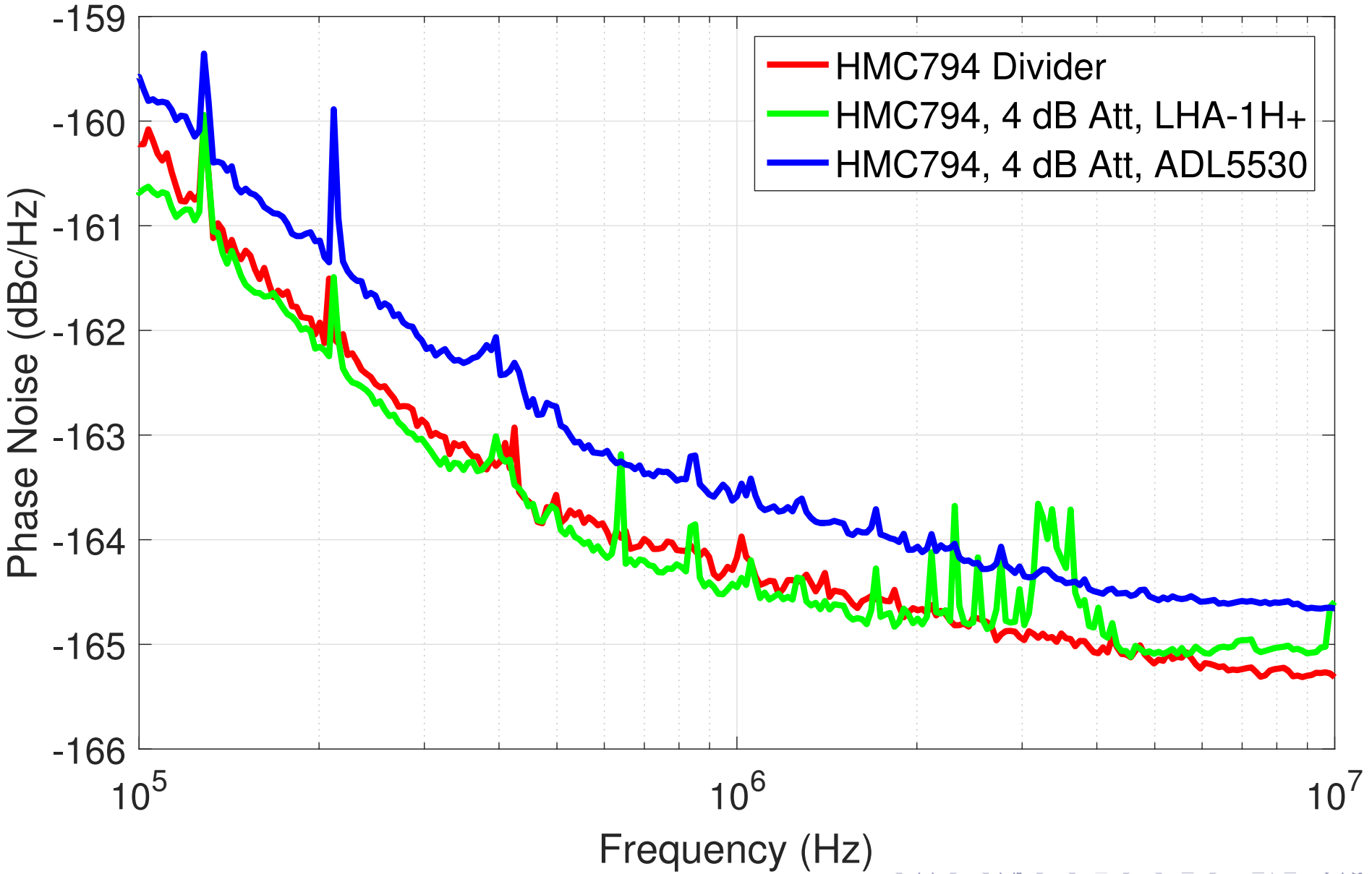
LHA-1H+



Clock Signal Amplifier PN Comparison



Clock Signal Amplifier PN Comparison (zoom-in)

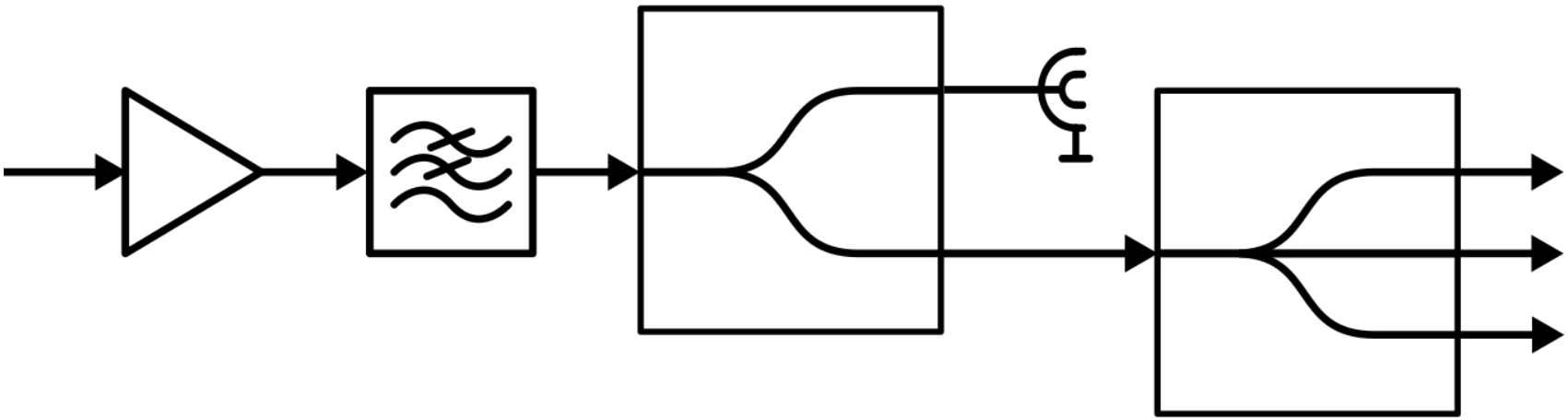


Other circuits

Reference Distribution

- Input power: +1 dBm to +5 dBm.
- Total power (inc. losses): +18 dBm.

Name	Power
Reference out	13 dBm ±1 dB
Mixer's input	+7 dBm to +13 dBm (+8 dBm preferred)
IF Frequency divider	-5 dBm to +10 dBm
CLK Frequency divider	>-1 dBm to +10



Power Diagnostic

- Power of clock and LO signals measured for diagnostic purposes.
- Maximum absolute error: 1 dB.
- Read-out resolution: 0.05 dB.
- Only small changes in normal operation.
- Sine wave shape with small harmonics.

AD8314 logarithmic power detector selected. ADC with 10.3 ENOB needed.

Digital Circuit and Communication Interface

- Communication with an AMC module using two three row ADF Zone 3 connectors.
- Pin assignment complaint with the DESY ZONE3 Digital Class D1.0 recommendation.
- Zone3 signaling: LVDS, LVCMOS 2.5V, or open collector 2.5 V.
- On-board ICs: CMOS/TTL 5V, 3.3 V open collector, LVCMOS 3.3V.
- Level converters or a PLD.
- MachXO2 PLD selected.
- SPI protocol with LVDS signaling.

MTCA.4 Management

Mandatory

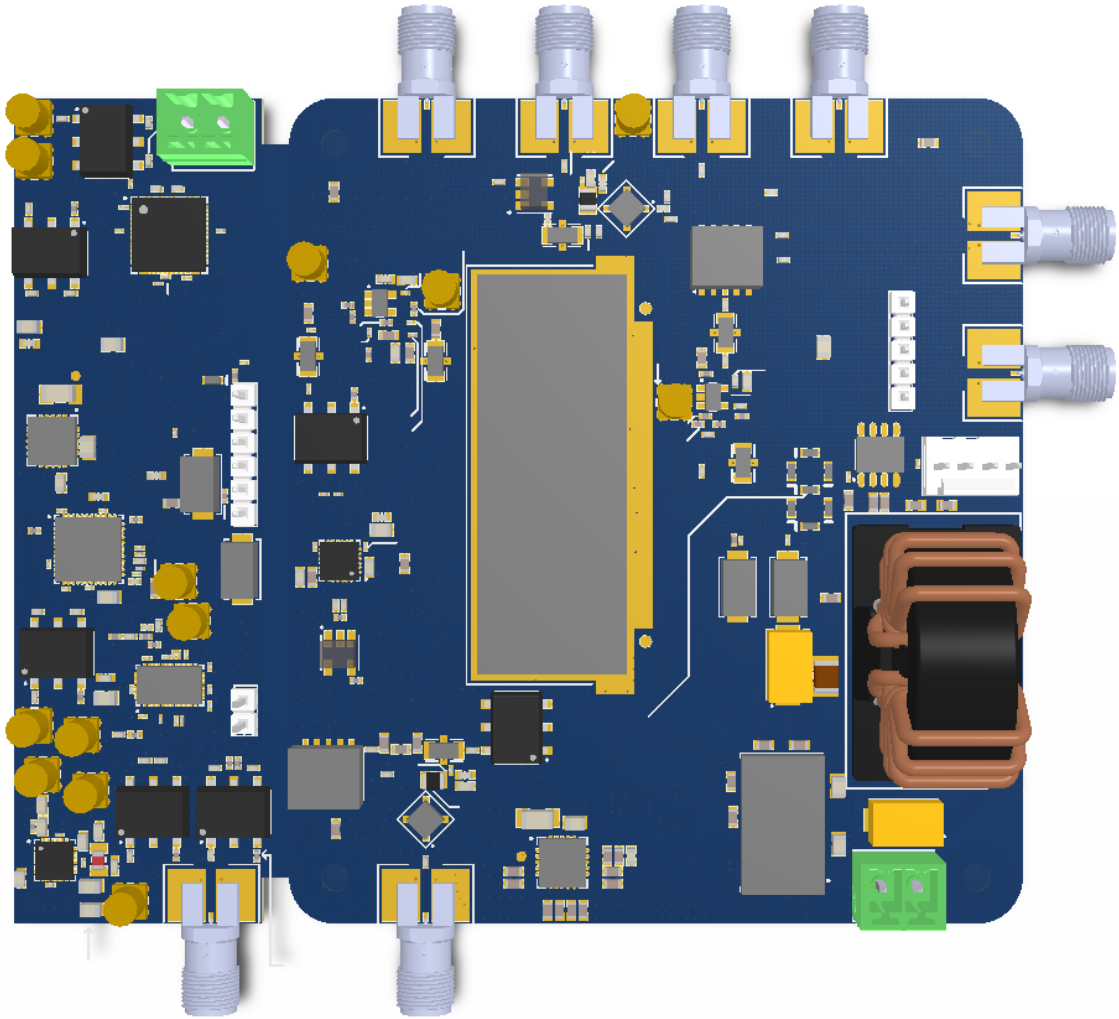
- IO expander (includes reset and power good).
- EEPROM with FRU info.

Temperature monitoring added.

Design Status and Schedule/Plans

Status

The first prototype is ready for production. Schematics and pcb design can be reused for RTM.



Plans

Activity	Start	End
First prototype: production and assembly	05-06-2017	31-07-2017
First prototype: measurements	31-07-2017	04-09-2017
RTM prototype: design	05-06-2017	06-11-2017
RTM prototype: CDR	13-11-2017	13-11-2017
RTM prototype: production and assembly	20-11-2017	15-01-2018
RTM prototype: measurements	15-01-2018	26-02-2018
M-Beta RTM: design	20-11-2017	26-03-2018
M-Beta RTM: production, assembly, testing	02-04-2018	17-12-2018
Test stand preparation	05-06-2017	30-04-2018

PDRs of LLRF parts: LO-generation

Igor Rutkowski

Warsaw University of Technology

30.05.2017