# RTM Carrier
# Preliminary Design Review

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ESS LLRF Preliminary Design Review, Lund

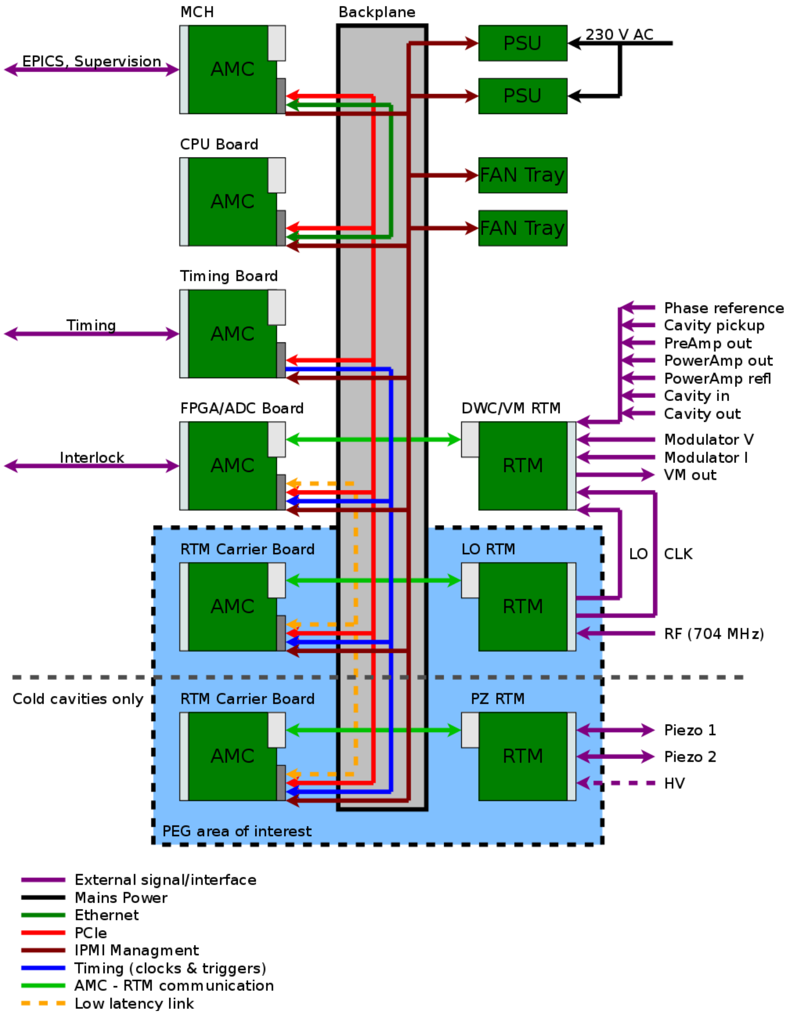
# Agenda

- Basic Concept
- Requirements
- FPGA
- FPGA Configuration
- Board Interfaces
- Clock distribution
- Power distribution
- Board management
- Memory
- Manufacturing and verification
- Quality plan
- Schedule
- Risk analysis
- Status

# ESS LLRF System and RTM Carrier

In the ESS LLRF System, the AMC board for supporting the RTMs shall provide minimal functionality that allows RTMs to operate, The general required functionality of the board is following:

- Communication with the RTM via ZONE 3
- Providing power to the RTM units
- Communication with the other devices using PCI-Express on the MTCA.4 backplane
- Data processing in the FPGA
- Fulfilling all the requirements for the AMC board defined in the MTCA.4 standard



# Board Interfaces

- MTCA.4 ZONE 3 – I/O communication with the RTM
- MTCA.4 Backplane connectivity:
  - PCI-Express on AMC ports 4-7
  - Low-Latency Links for direct board-to-board communication, AMC ports 12-15
  - MLVDS clocks, triggers and interlocks on AMC ports 17-20
  - Telecom clocks (TCLKA, TCLKB)
  - MTCA.4 management signals (IPMB, Geographical Address, PS0#, PS1#, ENABLE#, AMC JTAG)
- Front panel:
  - External clock input
  - External; clock output
  - Diagnostic connectors
- Custom/on-baord interfaces:
  - Xilinx JTAG connector for FPGA programming
  - JTAG Connector for MMC MCU

# RTM Carrier Requirements

1) Provide proper voltages (12V, 3.3V) for the RTM
   a) Provide as large as possible amount of power for the RTM (especially for piezo driver)
   b) Provide as high as possible current for specified time after start-up (in-rush current) for the RTM (especially for RTM)
2) Provide data transfer between MTCA.4 backplane and the RTM
   a) Zone 3 I/O configuration compatible with DESY D1.0 Recommendation
      i. All pins on the Zone 3 connector shall be connected to the FPGA
   b) Provide FPGA resources for implementing RTM-specific data exchange algorithms (SPI communication with the RTM, etc.)
   c) Provide access to RTM resources via the PCIe interface on the the MTCA backplane (ports 4-7)
   d) Provide connectivity between RTM and MTCA.4 extensions (MLVDS, ports 17-20)
      i. Provide clocks and triggers from the MTCA.4 backplane to the RTM
      ii. Provide interlock signals from the MTCA backplane to the RTM
      Iii. Provide interlock signals from the RTM to the MTCA backplane
3) Provide MTCA management for the RTM
   a) Provide I2C connection from the MMC
   b) Provide support for accessing RTM management resources via I2C: (MTCA required LEDs, Hot-Swap handle, sensors, etc.)
   c) Represent the RTM resources (identification, sensors) in the IPMI records to the MCH
   d) Provide power control for the RTM
   e) Provide standard sensors on the AMC board

# RTM Carrier Requirements

4) Provide clocks signals interconnect

  a) Provide MTCA clocks (TCLKA, TCLKB) for the RTM and for the FPGA

  b) Provide External clock source for the RTM and for the FPGA

  c) Provide on-board programmable clock generator for the RTM and for the FPGA

  d) Provide RTM clock for the FPGA

  e) Provide External clock output for monitoring selected on-board clock

  f) Provide local (non-programmable, always enabled) clock for the FPGA

  g) Provide dedicated clock infrastructure for PCIe interface

5) Provide diagnostics and support for out-of-crate board debugging

  a) Provide external power supply connector (12V, optionally 3.3V management power)

  b) Dual channel USB-Serial interface to FPGA and MMC

    i. Provide possibility to supply the management power (3.3V MP from the USB connector)

  c) LEDs on the front panel

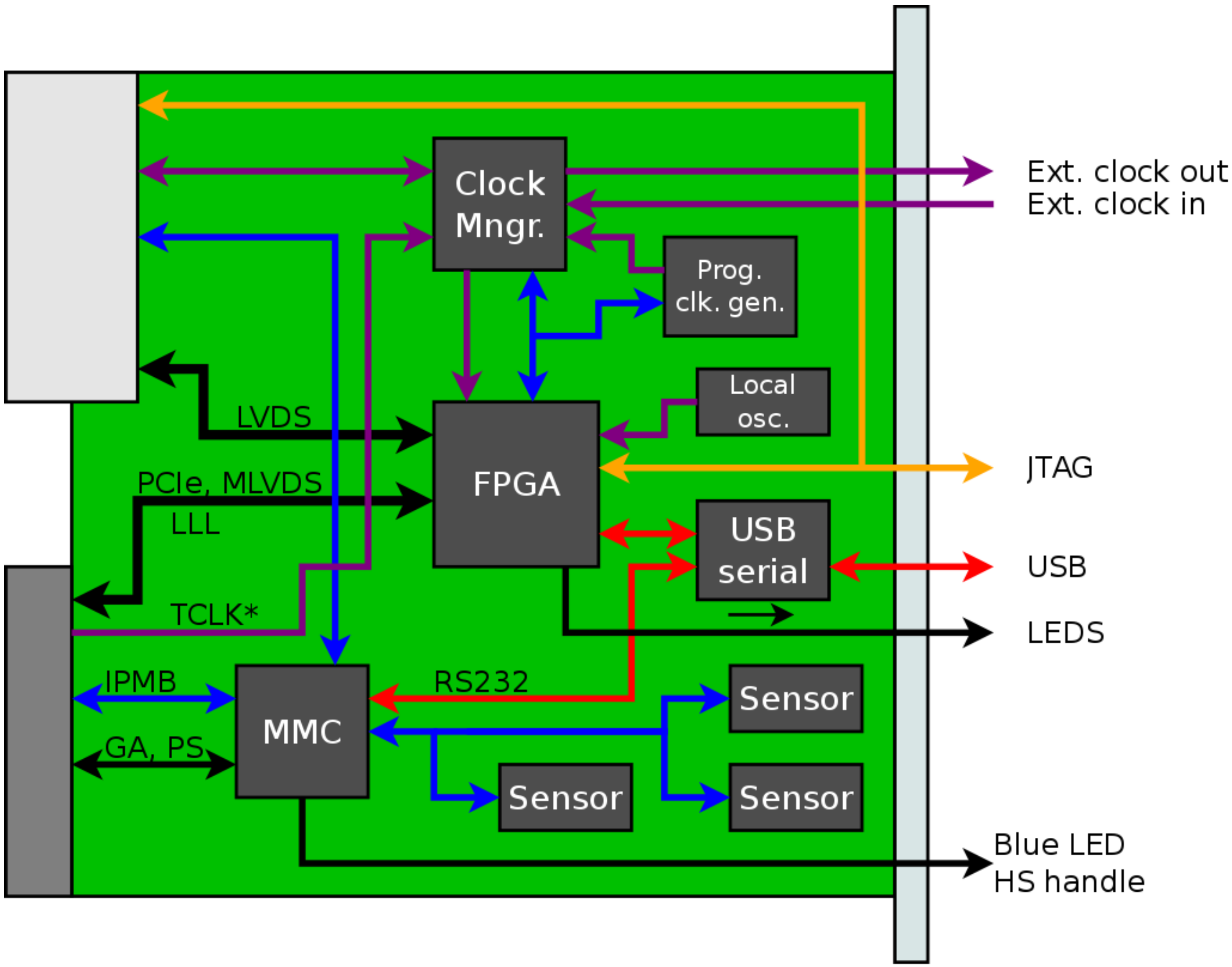
  d) JTAG interface for FPGA and for the RTM

6) Board should be low cost

  a) Price goal to be below 1000 Euro in mass production

7) Board should use latest low cost FPGA device

# RTM Carrier block diagram



# FPGA

The core component of the board is FPGA device. In this project, **Xilinx Artix-7** device has been chosen. This decision was made due to the following reasons:

**Vendor**: Xilinx devices are used widely in accelerator control, as well as in other areas of experimental physics. Those devices was used in X-FEL LLRF system, they are proven to be reliable, and PEG member has experience with this technology – PCB design for Xilinx FPGA, software tools knowledge for FPGA programming, etc.

**Gigabit transceivers** (MGT, RocketIO) – Providing support for PCI-Express and Low-Latency Links requires gigabit transceivers, because of this other FPGA families, such as Spartan-7 can not be used.

**Low Cost** – Artix-7 is a Xilinx low cost FPGA device with gigabit transceivers

**Latest architecture** – Artix-7 is a part of Xilinx 7-th Generation FPGA devices ("7 Series"), and in contrast with 6-generation and older devices, it is supported by most recent Xilinx development tools – **Vivado**.

# FPGA

In the described project, **FGG484/FBG484** footprint for the FPGA has been chosen.

This footprint allows assembly of the following devices:

| Part Number | Logic Cells | Slices | CLB Flip-Flops | Total Block RAM (Kb) | DSP Slices | Max. single ended IOs (6.6 Gb/s GTPs) |
|---|---|---|---|---|---|---|
| XC7A15T | 16,640 | 2,600 | 20,800 | 900 | 45 | 250 (4) |
| XC7A35T | 33,280 | 5,200 | 41,600 | 1800 | 90 | 250 (4) |
| XC7A50T | 52,160 | 8,150 | 65,200 | 2700 | 120 | 250 (4) |
| XC7A75T | 75,520 | 11,800 | 94,400 | 3780 | 180 | 285 (4) |
| XC7A100T | 101,440 | 15,850 | 126,800 | 4860 | 240 | 285 (4) |
| XC7A200T | 215,360 | 33,650 | 269,200 | 13140 | 740 | 285 (4) |

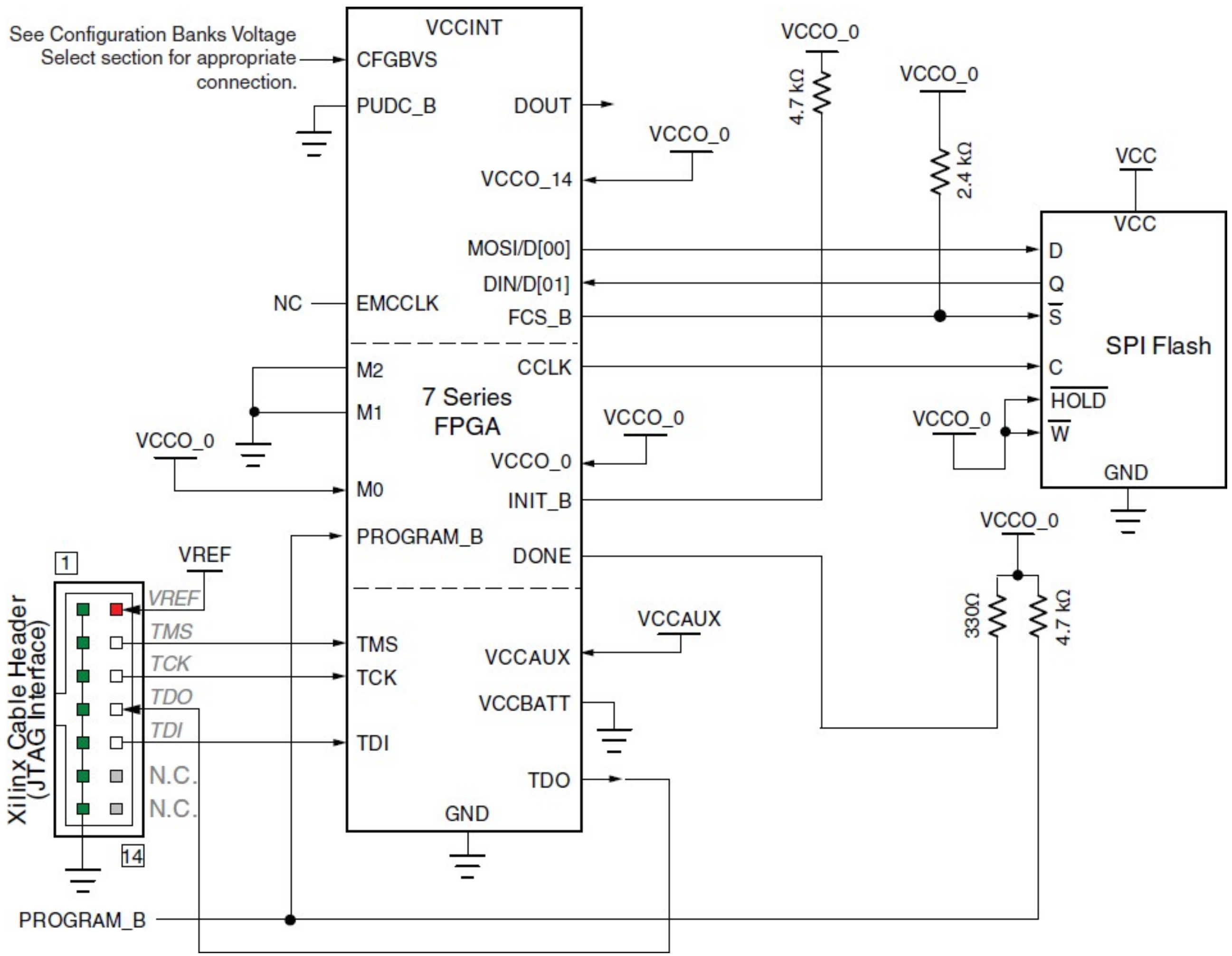
# FPGA Configuration

FPGA configuration process will be controlled by the Module Managment Controller (MMC).

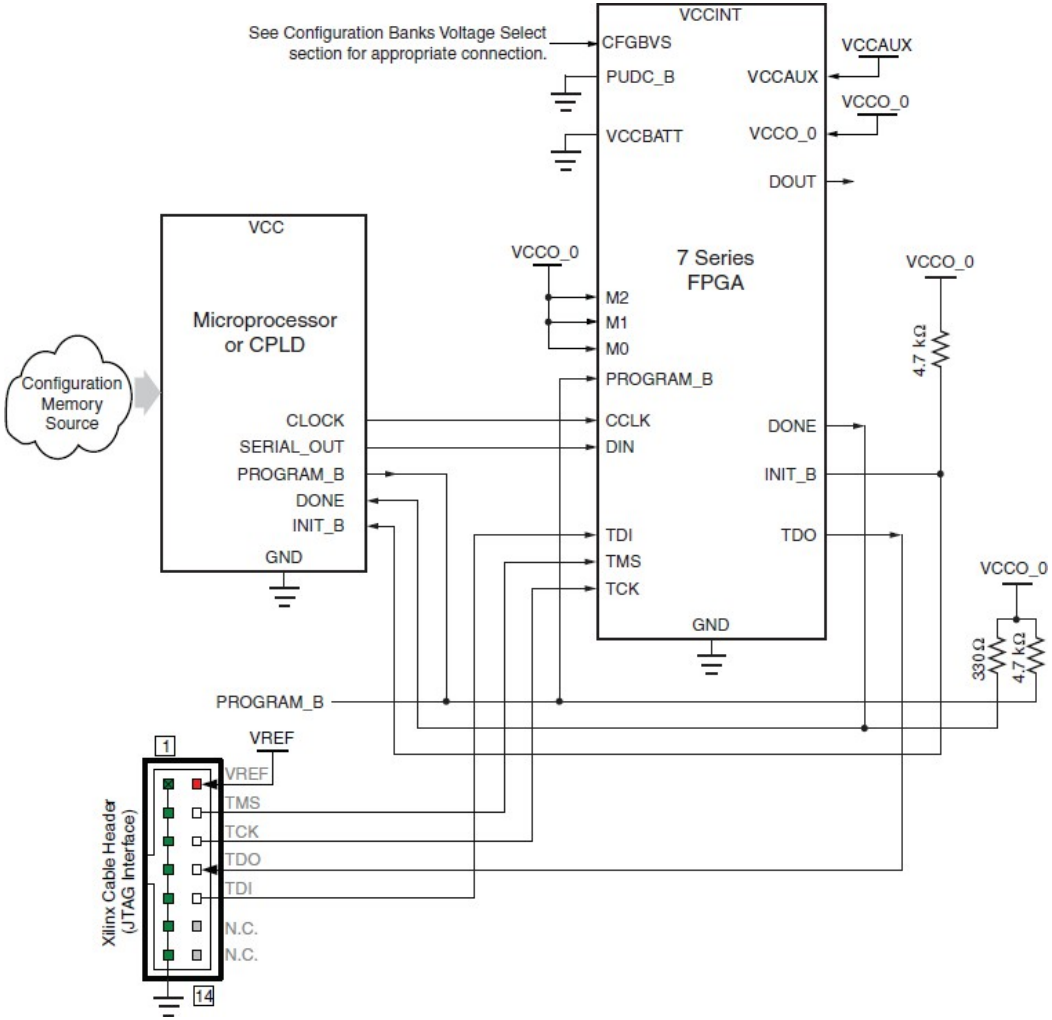
The following configuration modes are foreseen to be used:

- Master SPI – FPGA loads firmware from SPI flash by itself
- Slave Serial – MMC can disable SPI Flash ans push bitstream to FPGA
- JTAG – fail-safe configuration mode using external programming cable

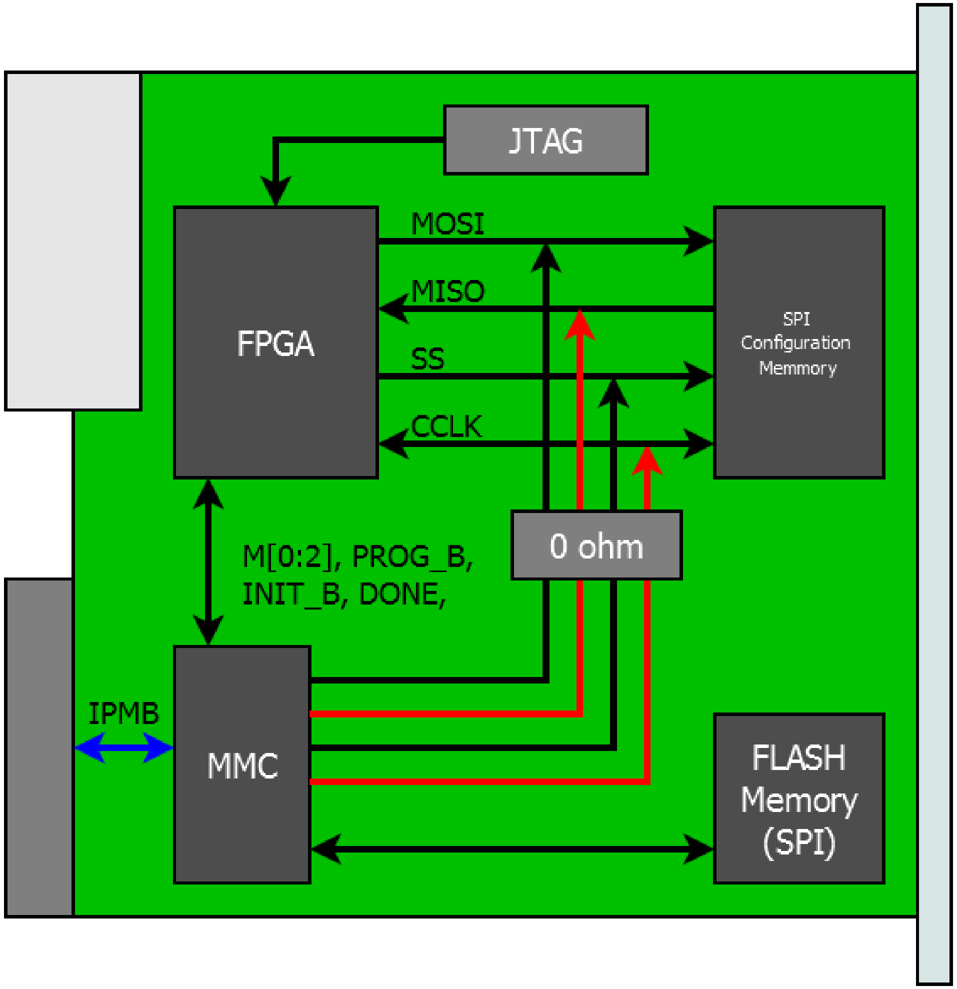
# FPGA Configuration (Master SPI)



# FPGA Configuration (Slave Serial)



# FPGA Configuration – block diagram



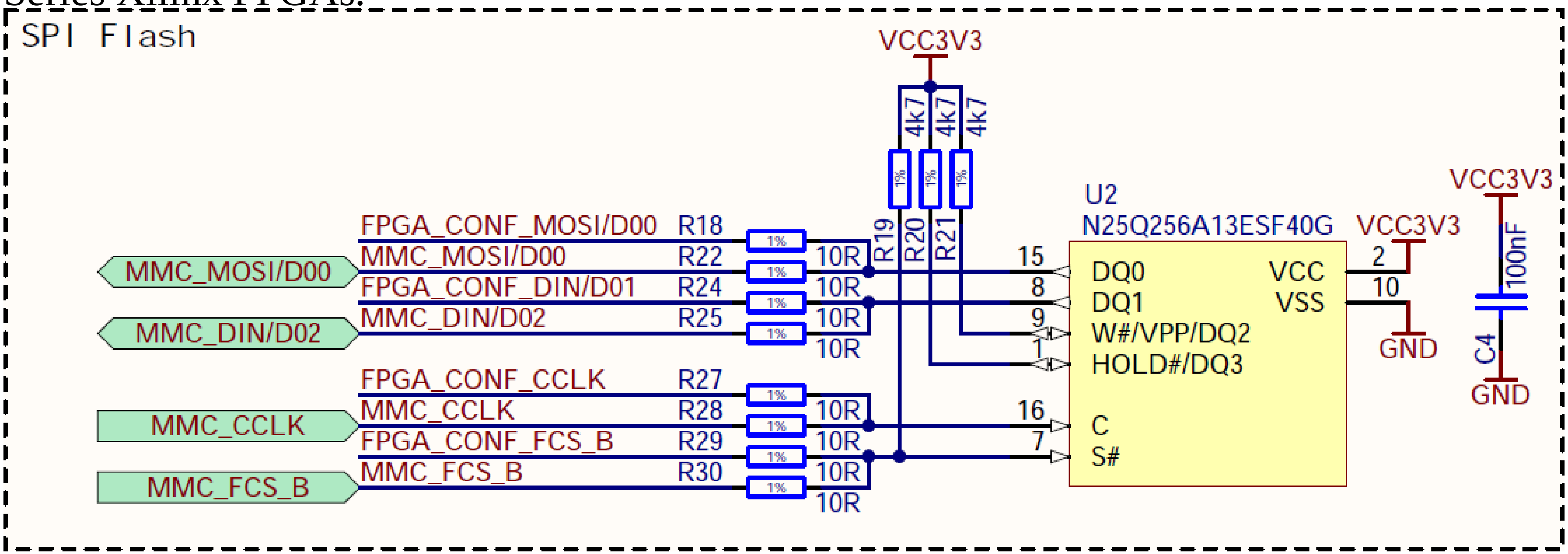
# FPGA Configuration

Proposed solution use minimal resources (PCB routing) to achieve following goals:

- Allow FPGA to load bitstream directly from SPI flash memory (configuration mode preferred by Vendor)
- Allow FPGA to update by itself the SPI flash during runtime;  this allows “remote firmware upgrade” using user data transfer interface – PCI-Express.
- Allow MMC to load bitstream directly to FPGA; MMC may handle several firmware revisions, and select which one shall be used. This also provides the “remote firmware update” via MMC feature
- Allow MMC to update SPI flash
- Allow MMC to readback the SPI flash

# FPGA Configuration – SPI Flash

As a SPI flash memory **N25Q256A13ESF40G**, has been selected. This is commonly used memory for Xilinx FPGAs configuration, and this particular device allows to keep bitstream for biggest Artrix-7 supported by RTM Carrier. This memory is supported by both ISE and Vivado development tools, and it is compatible witch serial configuration modes of the 7-Series Xilinx FPGAs.



# FPGA Configuration – JTAG

For development and in case of FPGA troubleshooting, JTAG configuration mode is provided. Describes desing has two JTAG slave devices:

- FPGA device
- RTM Interface

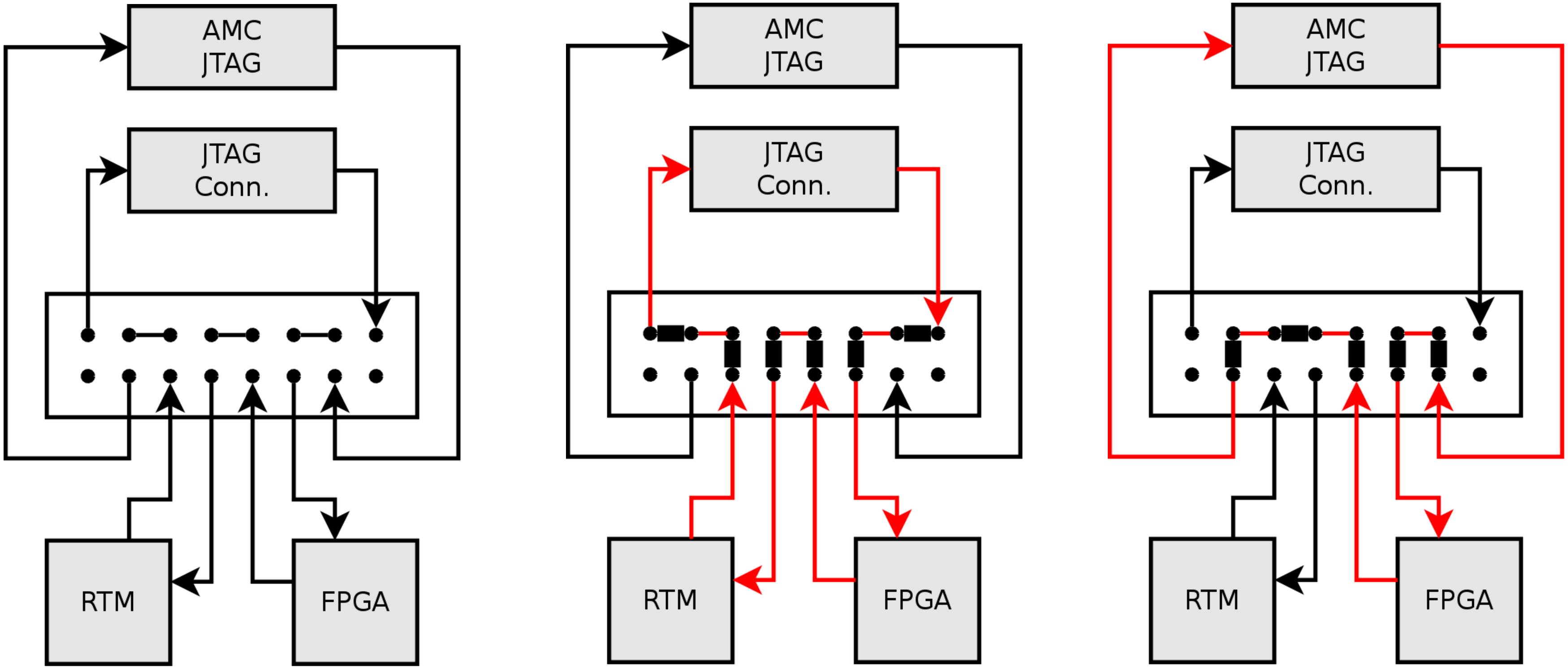
and two JTAG master interfaces:

- Xilinx JTAG Connector
- AMC JTAG interface

MMC device will not be included in the chain and will have own JTAG connector

# FPGA Configuration – JTAG

For simplicity and robustness, JTAG will be configured by jumpers:



# Board Interfaces – PCI Express

**PCI-Express**

Selected FPGA devices family has 4 MGT interfaces, and due to requirement of having support for Low-Latency Links (LLL), not all MGT can be used for PCI-Express. As a compromise, 2 MGTs has been assigned for PCI-Express, and 2 for LLL, resulting in having PCI-Express x2 (Gen2) on the AMC ports 4 and 5.

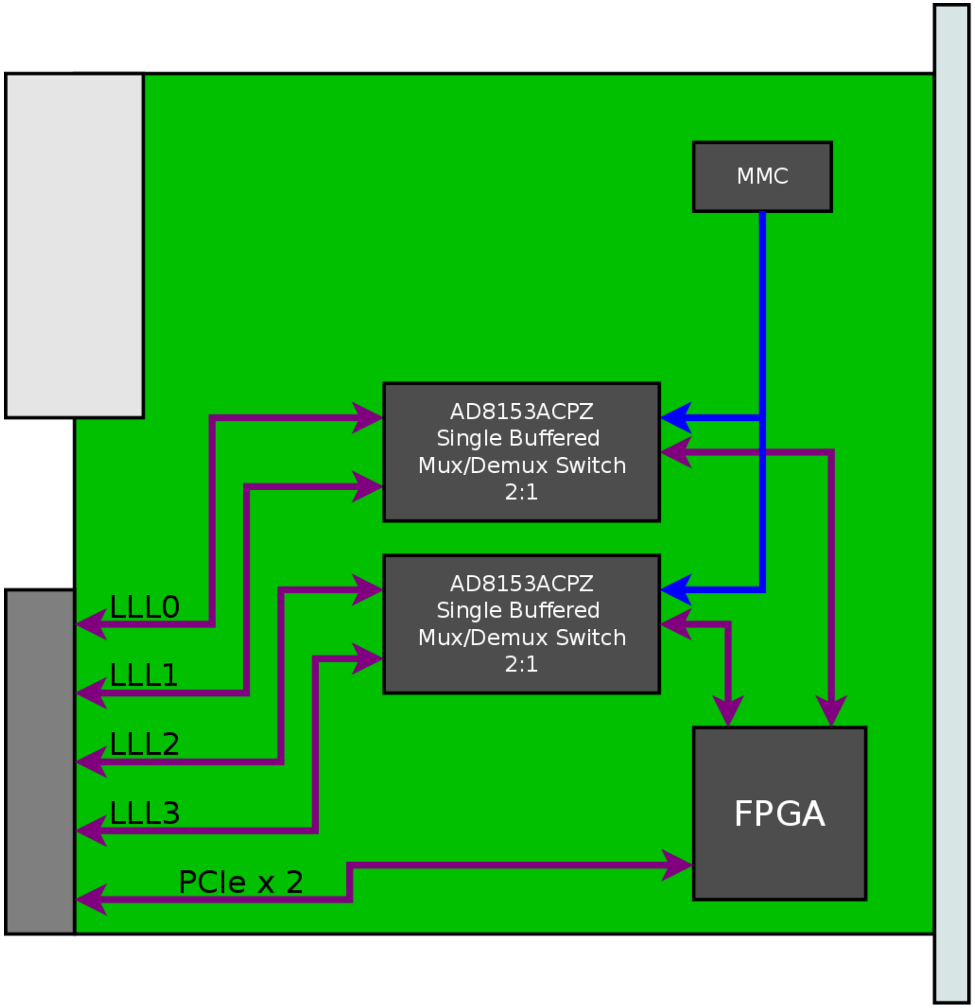
# Board Interfaces – Low Latency Links

**Low-Latencty Links (LLL)**

This interface is for fast board-to-board communication over the MTCA backplane. As it was mentioned above, 2 (of 4) MGTs has been assigned to LLL. Board to board communication has been foreseen on AMC ports 12-15. But to the limitation of MGT amount (2), all for ports are covered using two 2:1 switches, having 12 or 13 on one MGT, and 14 or 15 on another MGT. Communication parameters strictly depends on the FPGA configuration, and it must be compatible with other device in the crate.

Device chosen as a LLL switch is **AD8153ACPZ**, it is I2C controlled single mux/demux for gigabit links. Using these two switches allows to have all LLL connected to FPGA without soldering and desoldering zero-ohm resistors.

# Board Interfaces – Low Latency Links



# Board Interfaces – MTCA.4 Zone 3

**MTCA.4 Zone 3**

This is interface for communication with RTMs, in described design zone 3 will be implemented according to DESY D1.0 recommendation. Zone 3 connector will be fully covered, providing 96 LVDS pairs and supporting clock signals.

# Board Interfaces – MLVDS

**MLVDS**

This will provide general purpose clock, trigger or interlock signals on AMC ports 17-20. Each signal can operate in both direction, board can read or drive it on the MTCA backplane. For implementation of MLVDS bus, DS91M040TSQE/NOPB devices has been used, which was the cheapest quad MLVDS transceiver, which performance is compatible with MTCA standard.

# Board Interfaces – Clocks

**Telecom clocks (TCLKA, TCLKB)**

Board will use available on the MTCA backplane telecom clocks, TCLKA and TCLKB. These signals will be routed through the clocking cross-switches, that they can be delivered to RTM and FPGA.

**Clock input and output**

Board will provide external TTL clock input and TTL clock output on the front panel.

# Board Interfaces – MTCA.4 Managment

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**MTCA.4 management signals**

Except data transfer interfaces such as PCI-Express, board will support management signals available on the MTCA backplane, such as: IPMB, Geographical Address, PS0#, PS1#, ENABLE#, and AMC JTAG.

# Board Interfaces – Debug

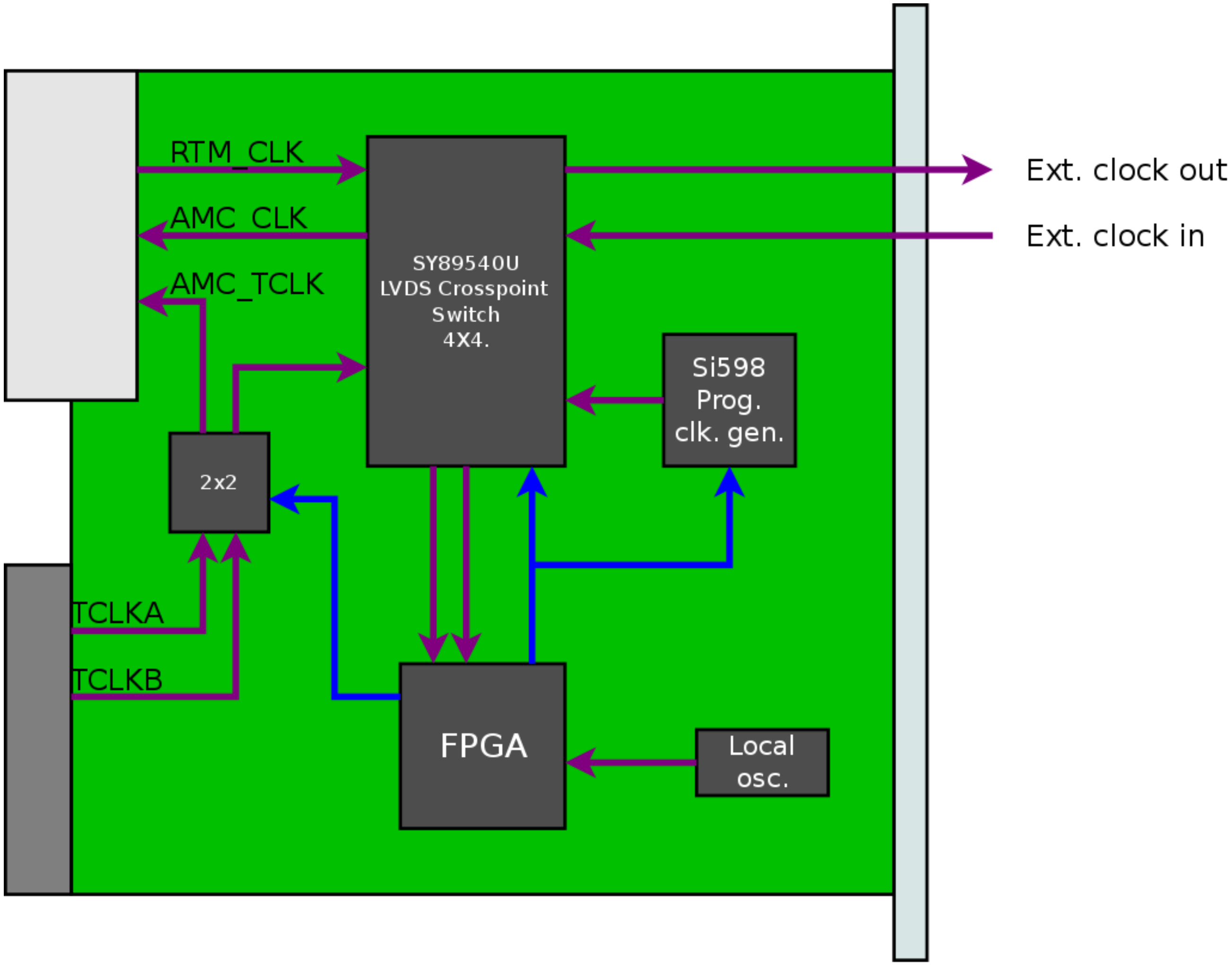
**Debug interfaces**

For the purpose of board diagnostics, it will be equipped in several debug interfaces. Board will have dual USB-Serial connector, where one channel will be connected to the MMC system serial port, and other channel will be connected to the FPGA providing user the ability to create simple communication interface, which is not dependent on other infrastructure, especially MTCA. It can be useful for accessing FPGA in case of MTCA communication problems.

Except the USB transceiver for serial ports, there will be another micro USB connector on the front panel, which will be the USB interface of the MMC. This second interface may utilize the additional functionality availale in MMC, such as acting as dedicated USB device, like processor programming interface, etc.

Also board will have on PCB dedicated JTAG connectors, Xilinx JTAG connector for FPGA programming and supporting RTM JTAG chain (if any), and MMC MCU dedicated JTAG Connector.

# Clock distribution



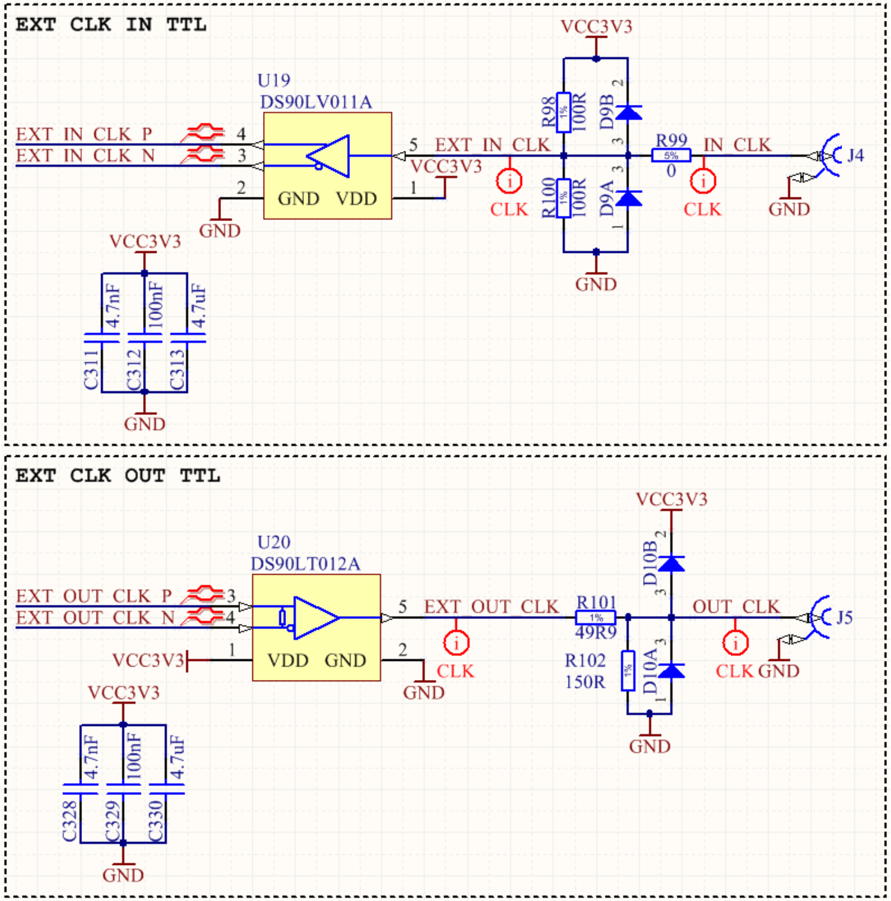
# Clock distribution

Features of presented solution:

- Clock from RTM can be delivered to the FPGA and to front panel clock output
- External clock can be delivered to FPGA and to RTM
- Each of 4x4 cross-point switch input can be routed to 3 destinations: FPGA clock capable pin, external output via lvds-to-ttl buffer, or RTM clock input.
- Both telecom clocks can be delivered to FPGA and RTM via 2x2 cross-switch, but one signal cannot go to both receivers - TCLKA may go to RTM and TCLKB to FPGA (through cross-switch), or TCLKB may go to RTM and TCLKA to FPGA (through cross-switch)
- There is programmable clock generator, to have flexible clock source
- FPGA has local always enabled clock source, to bootstrap and configure the rest of clocking infrastructure, such as cross switch or programmable clock generator

# Clock distribution

External Clock input and output buffers



# Clock distribution

Main clock infrastructure components:

- **DS25CP152 -** small footprint 2x2 LVDS cross-point switch designed for backplane acquiring signals, it has low additive jitter (max. up to 1 ps), which allows to use this device as clock switch
- **SY89540U -** small footprint 4x4 LVDS cross-point switch designed for high data rates with good channel-to-channel crosstalk performance, it has very low additive jitter (<0.1 ps), which allows to use this device as clock switch
- **LMK61E2BBA-SIAT -** programmable LVDS oscillator witch internal EEPROM. This device has internal power conditioning that provide excellent PSRR. Output frequency is in range from 10 MHz to 900 MHz, footprint is compatible with well known SI598, but this device is much cheaper and has better availability.
- **CFPS-39IB 50.0MHZ -** 50 MHz single ended locked frequency oscillator

# Power distribution

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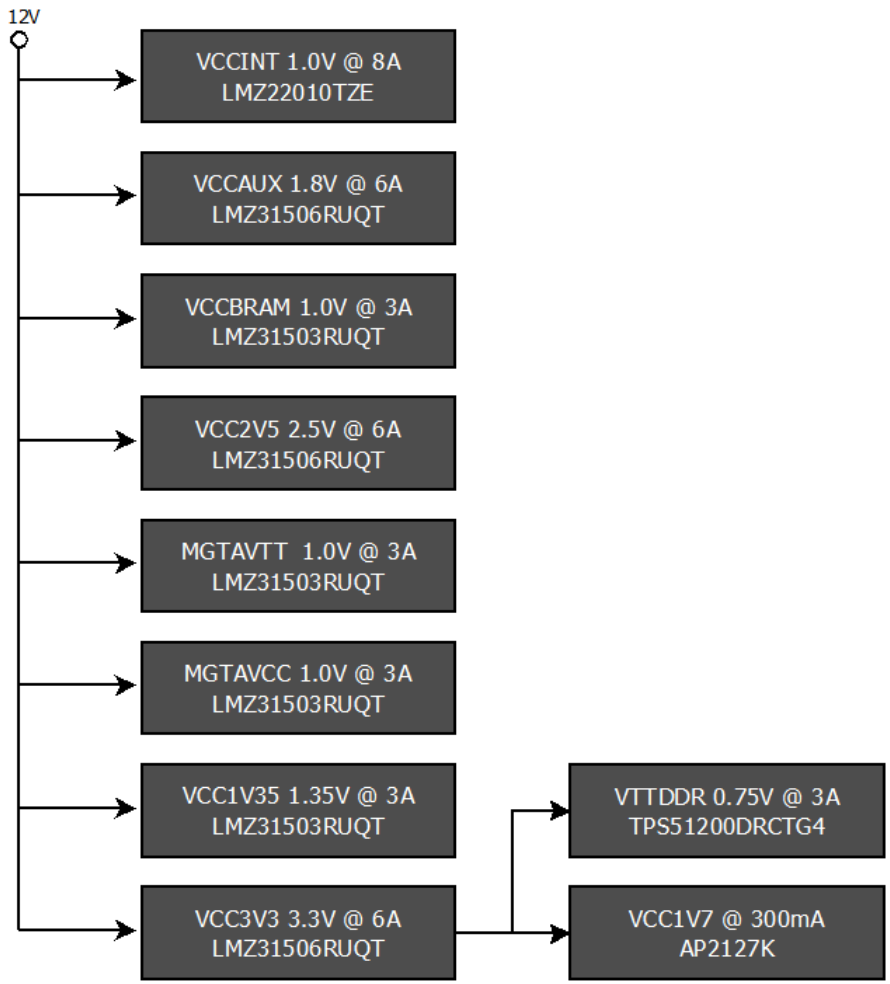
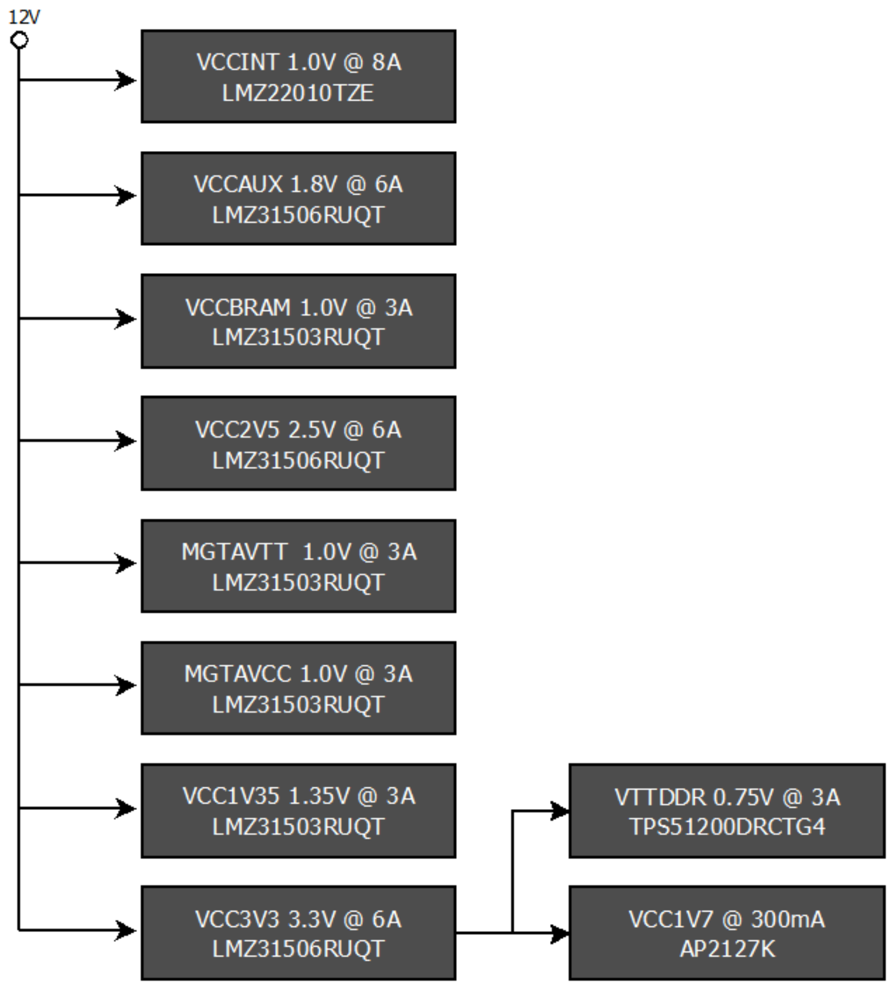
- For RTM Carrier, family of SIMPLESwitcher devices produced by Texas Instruments (TI) has been chosen.
- These are power modules with integrated shielded inductors that simplified PCB design and has low EMC emission.
- Three type of switchers, with output current of 8, 6 and 3 A, are used in design.
- In addition, according to Xilinx documentation, MGT power supplies MGTAVTT and MGTAVCC should have own supplies.

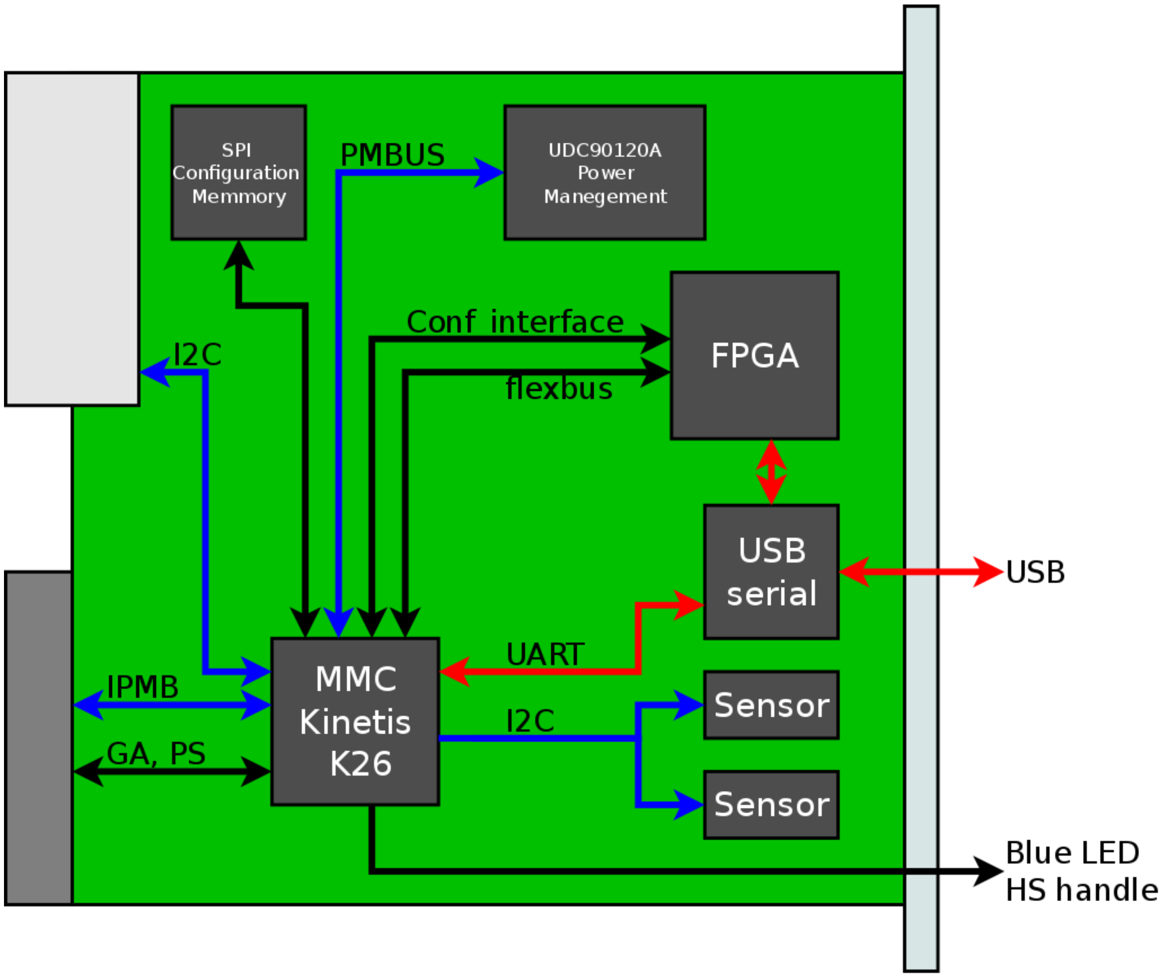


# Power distribution

- Each specific FPGA power has own power supply that allows to implement maximum device resources utilization for biggest bga484 Artix-7 device.
- FPGAs banks needs 3 types of supplies:
  - 2V5 for LVDS_25 that are compatible with ZONE3 specification,
  - 3V3 for bank connected to FPGAs peripherals, JTAG, and configuration memory
  - 1V35 for bank connected to DDR3 memory, which allows to implement SSTL I/O standard needed for DDR memory communication



# Board Managment



# Board Managment

- Kinetis K-26 ARM microcontroller (**MK26FN2M0VLQ18**) has been selected as a MMC device
- It has four I2C interfaces, USB interface that allows to implement serial device, low current consumption, 256KB of RAM memory, 2MB Flash memory and ADC with build in voltage reference (for on-board voltages monitoring)
- To simplify board operation, and avoid potential problems with MMC software controlled power start-up sequencing, a hardware power sequencer was placed on the board
- For RTM power control **TPS2459** device has been chosen. This is hot-plug controller for AMC, with digitally controlled inrush current and over-current protection. It has I2C interface, and it is possible to set current limits by software directly from MMC.

# Board Managment

- Except described devices, RTM carrier will be equipped in following management components:
  - 2x I2C on-board temperature sensors **MAX6626RMTT**
  - 1x I2C Temperature sensor **SA56004EDP** for readout of FPGA internal temperature sensor
  - 1x EEPROM memory **24AA025E48T-I/OT** (typically for board identification data)
  - 1x SPI Flash **N25Q256A13ESF40G**, foreseen for additional FPGA firmware storage
- Board will have also USB-serial converter for communication with MMC serial port and/or FPGA.

# Memory

- RTM Carrier will have DDR3 memory of capacity 8Gb (1GB – one gigabyte).
- Memory will be implemented using single **MT41K1G8SN-125:A** device.
- It has internal organization 1Gx8,
- This memory has 8-bit data bus width, because this is only way to implement DDR3 interface utilizing single FPGA bank of Artix-7 (but is not a problem since it can run with frequency of 300 MHz or more)
- Devices of this family are supported by latest Vivado design software
- Availability of this memory on the market has been confirmed.

# Manufacturing and verification

Planned test and measurements:

- Visual inspection, if there is no visible damage, if there is no missing components, if soldering looks good, if there are no external bodies that may cause short, etc. - if there is nothing suspicious
- Check with ohmmeter resistance between GND and major power nets (if there is no short)
- Power-on the board with the management power
- Check standby management power consumption on the power supply - if it is in the expected range;
- Check visually if LEDs expected to be active are illuminating.
- Check management power voltage level with multimeter
- Connect MMC programmer and load test firmware for MMC

# Manufacturing and verification

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Planned test and measurements (cont.1):

- Measure management power consumption with loaded test firmware
- Check if result of MMC test firmware operation is as expected
- Power on the payload power;
- Check standby payload power consumption on the power supply - if it is in the expected range
- Check visually if LEDs expected to be active are illuminating.
- Check voltages derived from payload power if they are correct
- Connect the FPGA programmer and load test FPGA firmware

# Manufacturing and verification

Planned test and measurements (cont.2):

- Measure payload power consumption with loaded test firmware
- Check if result of FPGA test firmware operation is as expected
- Load operational MMC code on the board
- Power-off the board
- Place board in the MTCA crate
- Power on the crate
- Check if board was properly initialized

# Manufacturing and verification

Planned test and measurements (cont.3):

- Load test firmeare 2 to FPGA,
- Check connectivity with the CPU via PCIe
- Check connectivity with RTM
- Check the connectivity with test boards using LLL
- Check triggering and receiving signal via MLVDS bus

# Quality plan

**Quality assurance of the RTM Carrier PCB project is based on:**

- Continuous in parallel project (schismatics, PCB and libraries) review by other PCB design engineers, skillful in the used technologies, such as Xilinx FPGA.
- Drawing schematics using consistent conventions, such as naming convention, drawing style, etc.
- Project files are stored in Subversion version control (SVN) system repository on the server. This helps in tracking changes, guarantees always safe “step-back” option to the latest correct design version, and provides a form of backup – project is places always in at least 2 places: on engineer’s computer (actual working copy) and on the server (last committed version with all history of changes). Regardless of this, server with SVN repository is backed-up independently by itself.

# Schedule

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Actual agreement defines following schedule concerning the RTM Carrier:

| Phase | Beginning | End |
| --- | --- | --- |
| Design of the first prototype | 01-01-2017 | 01-08-2017 |
| Design of the M-Beta prototype | 01-10-2017 | 01-04-2018 |
| Design of the H-Beta prototype | 01-10-2019 | 01-04-2020 |

# Risk analysis

| Event | Cause | Impact | Treatment plan |
| --- | --- | --- | --- |
| Late change of requirements | Insufficient data during requirements analysis | Late modules delivery. | Use as good as possible estimated requirements, if final ones are not available and build first prototype, expecting that for the next iteration(s), final requirements will be provided. |
| Delay in prototype design | Insufficient manpower | Delay in board delivery, increased cost | Increase manpower, find new employees |
| Prototype doesn't meet the requirements | Bad board concept | Delay in board delivery, increased cost | - Identify the reason of the problem<br>- Correct the board concept and selected technology<br>- Correct the prototype design - perform one more design iteration |

# Risk analysis

| Event | Cause | Impact | Treatment plan |
|---|---|---|---|
| Problems with components avaiablility | Long time between concept of the board and implementation/assembly | Delay in board delivery, increased cost | - Wait for components if unavailability is temporary<br>- Try to order missing components, even if they are much more expensive<br>- Try to find matching replacement components if possible<br>- Consider which board functionality depends on the missing components and if this is acceptable<br>- look for functional walk-around of the missing feature if possible<br>- Redesign the board, to avoid using missing components |
| Broken components soldered on prototype | Problems with manufacturing technology, bad/broken components ordered, components stored/handled n the wrong way or Insufficient quality control. | Delay in board delivery, increased cost | - Identify affected units<br>- Order required amount of good components<br>- replace bad components |

# Risk analysis

| Event | Cause | Impact | Treatment plan |
|---|---|---|---|
| Broken components soldered on M-Beta version | Problems with manufacturing technology, bad/broken components ordered, components stored/handled n the wrong way or Insufficient quality control. | Delay in board delivery, increased cost | - Identify affected units<br>- Order required amount of good components<br>- replace bad components<br>- send repair team to ESS if affected units has been already shipped |
| Broken components soldered on H-Beta version | Problems with manufacturing technology, bad/broken components ordered, components stored/handled n the wrong way or Insufficient quality control. | Delay in board delivery, increased cost | - Identify affected units<br>- Order required amount of good components<br>- replace bad components<br>- send repair team to ESS if affected units has been already shipped |
| Not detected design mistake in final version | - Insufficient quality control<br>- error in test-stand, which covered described mistake<br>- Error in board testing software, which covered this mistake | Increased cost of maintenance. Decreased performance. Reduced functionality. | - Identify mistake severity<br>- Identify functionalities disabled by this mistake<br>- Consider if this mistake could be acceptable (in contrast to full redesign and reproduction cost)<br>- Perform board redesign and fabrication of all boards if there is no other way |

# Actual Status

First prototype is at the stage of PCB design, schematics are finished – only minor changes are done while PCB layout is done. First prototype is going to be delivered on time.

# The End

Thank You for Your Attention !