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EUROPEAN SPALLATION SOURCE

PDR for Cavity Simulator

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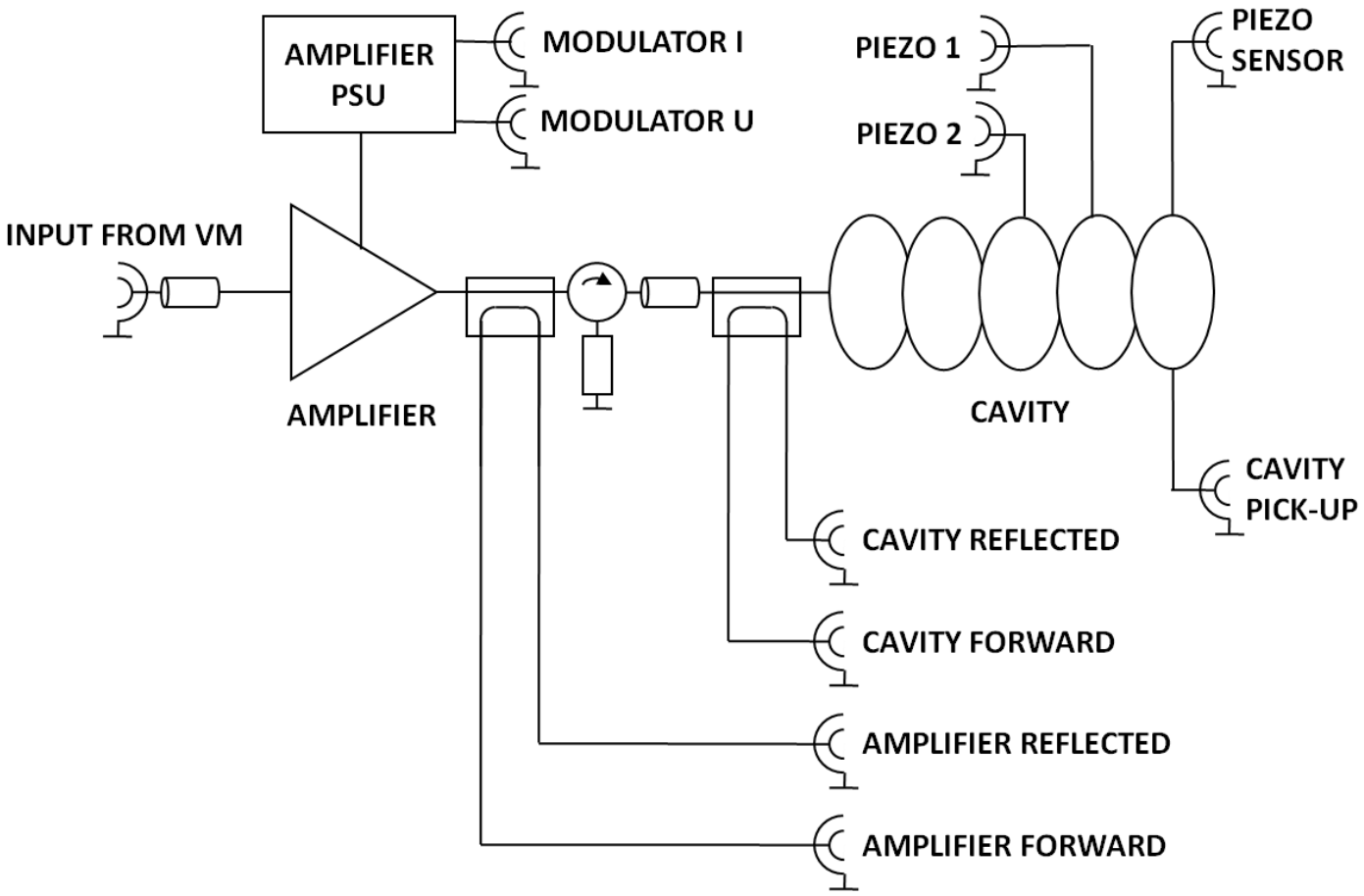
Agenda

- Introduction
- Hardware
- Firmware and Software
- Design Status

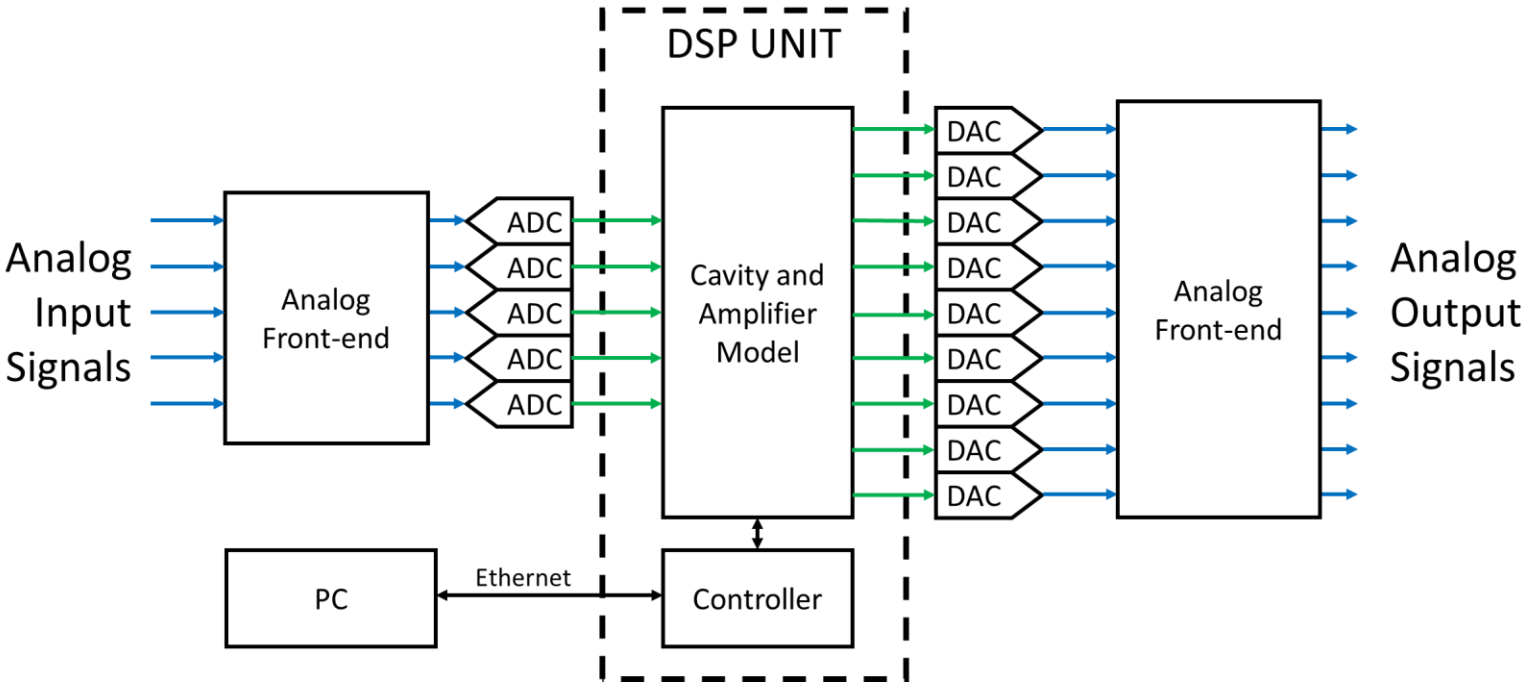
Intoduction

- PEG will assemble and install 80 LLRF control systems.
- Each system will be tested after the assembly and then after the installation.
- To simulate the closed loop operation the Cavity Simulator is needed.

Introduction – Simulated System



Introduction – Block Diagram



Introduction – Requirments

- RF outputs:
  - Number of outputs: 6 (main) + 6 (monitoring)
  - Maximum output power: 15 dBm (main), 5 dBm (monitoring)
  - Center frequency: 704 MHz
  - Bandwidth: 10 MHz
- RF inputs: 2
  - Number of inputs: 2
  - Center frequency: 704 MHz
  - Bandwidth: 10 MHz
- High Voltage analog inputs
  - Number of inputs: 2
  - Voltage range: ±100 V
  - Bandwidth: 100 kHz

Introduction – Requirments

- Fast analog outputs:
  - Number: 2
  - Bandwidth: 1 MHz
- Analog outputs:
  - Number: 1
  - Bandwidth: 100 kHz
- Communication interfaces:
  - Ethernet
  - USB (JTAG)
- Power supply: 230 V
- Power consumption: <250 W

System Latency

- The latency of the real system is around 0,35 µs*.
- It is equal to around 41 clock cycles at 117.4 MHz
- Latency of typical ADC: 10 clock cycles
- Latency of typical DAC: 7 clock cycles
- Latency of the DSP: < 24 clock cycles

* Friedrik Kistensen, "LLRF performance evaluation"

RF Signal Generation Schemes

	Advantages	Disadvantages
Direct Digital Synthesis	• Very simple analog circuit	• High sampling rate DAC required • High data rates • Poor noise performance
Up-conversion	• Very good noise performance	• Complex analog circuit • Additional LO signal required.
Vector Modulator	• Simple analog circuit • Good noise performance	• Two DACs required • Reference signal required

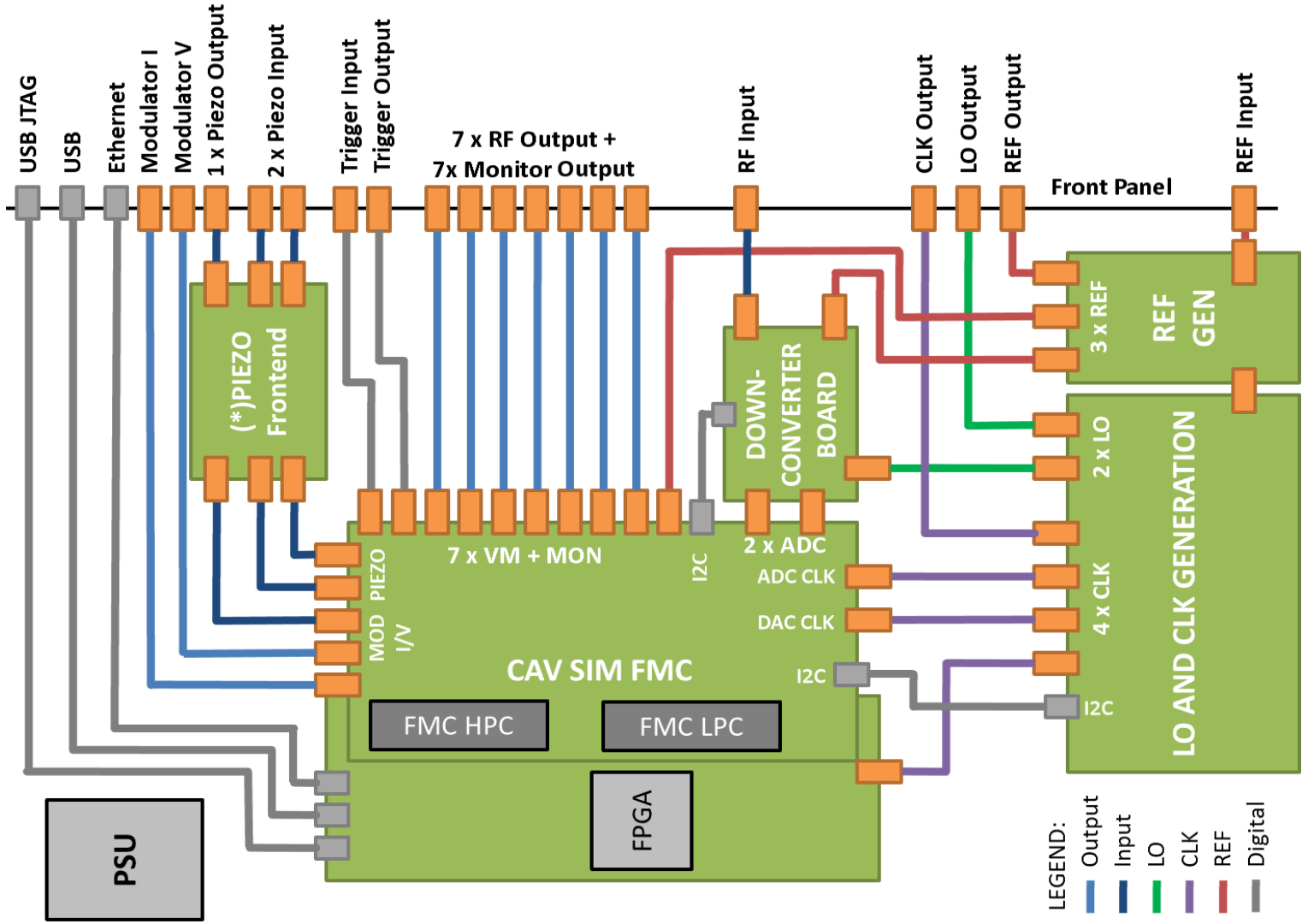
The Vector Modulator scheme was selected

RF Signal Digitizing Schemes

	Adventages	Disadvanteges
Direct Sampling	• Very simple analog circuit	• Require high speed ADC
Down Conversion	• Very good noise performance	• Complex analog circuit • Requires additional LO signal generator
IQ Demodulation	• Simple analog circuit • Good noise performance	• Require two ADCs • Require Reference Signal • Poor intermodulation perfromance

The down conversion scheme was selected.

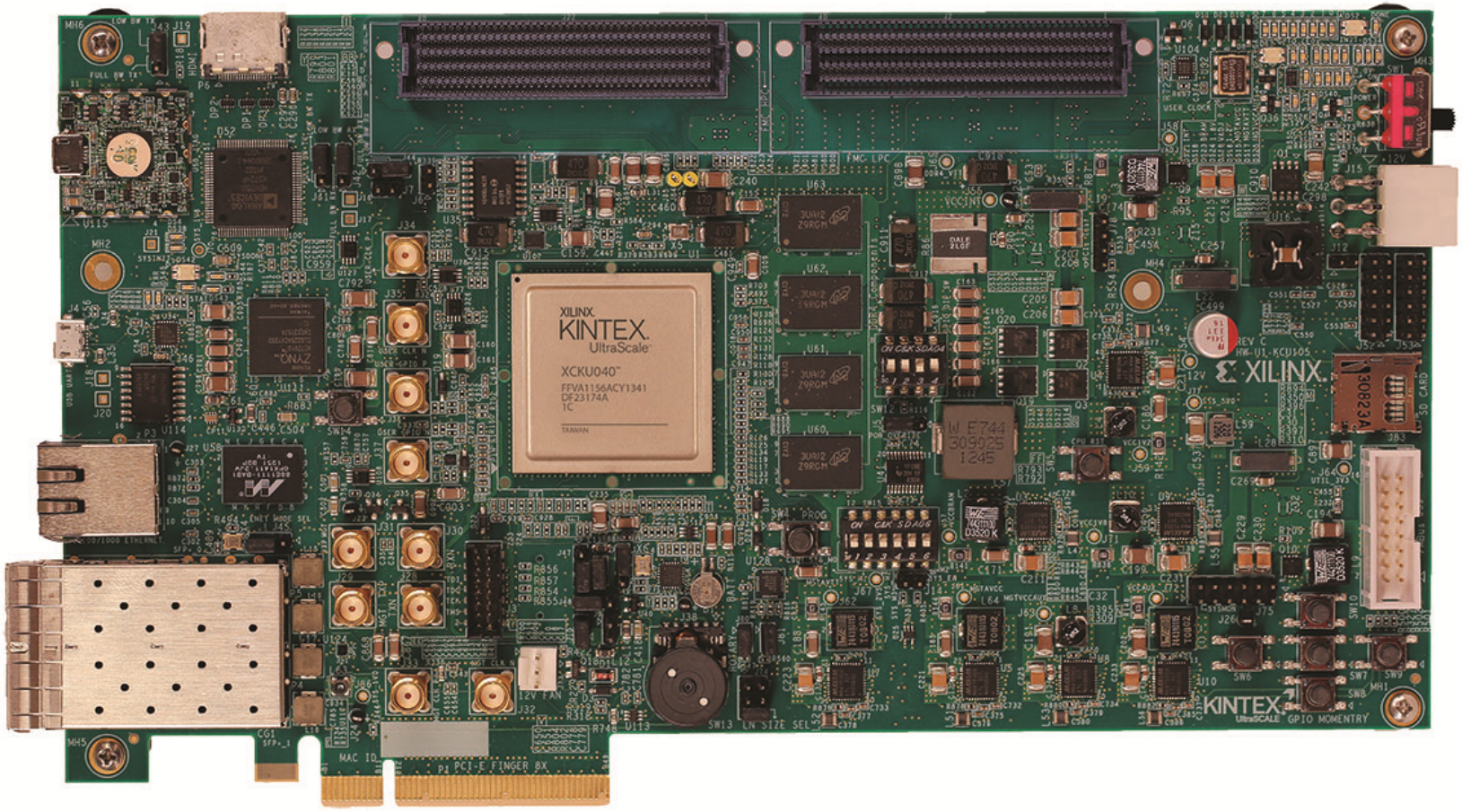
Hardware – Block Diagram



Hardware – FPGA Processing Module

	KC705	**ZC706**	**ZCU102**	**KCU105**
FPGA	Kintex 7 XC7K325T	Zynq 7000 XC7Z045	Zynq Ultrascale XCZU9EG	Kintex Ultrascale XCKU040
CPU	-	Dual-core ARM Cortex-A9 MPCore	Quad-core ARM Cortex-A53	-
Logic Cells (K)	356	350	600	530
Block Ram (Mb)	25.74	19.1	32.1	21.1
DSP Slices	1440	900	2520	1920
RAM Type	DDR3	DDR3	DDR4	DDR4
RAM Capacity	1 GB	2 x 1 GB	4 GB+512 MB	2 GB
FMC Connectors	**HPC:** 58 x LVDS, 4 x GT **LPC:** 34 x LVDS. 1 x GT	**HPC:** 34 x LVDS, 8 x GT **LPC:** 34 x LVDS. 1 x GT	**HPC:** 34 x LVDS, 8 x GT **HPC:** 34 x LVDS. 8 x GT	**HPC:** 57 x LVDS, 8 x GT **LPC:** 34 x LVDS. 1 x GT

Hardware – FPGA Processing Module

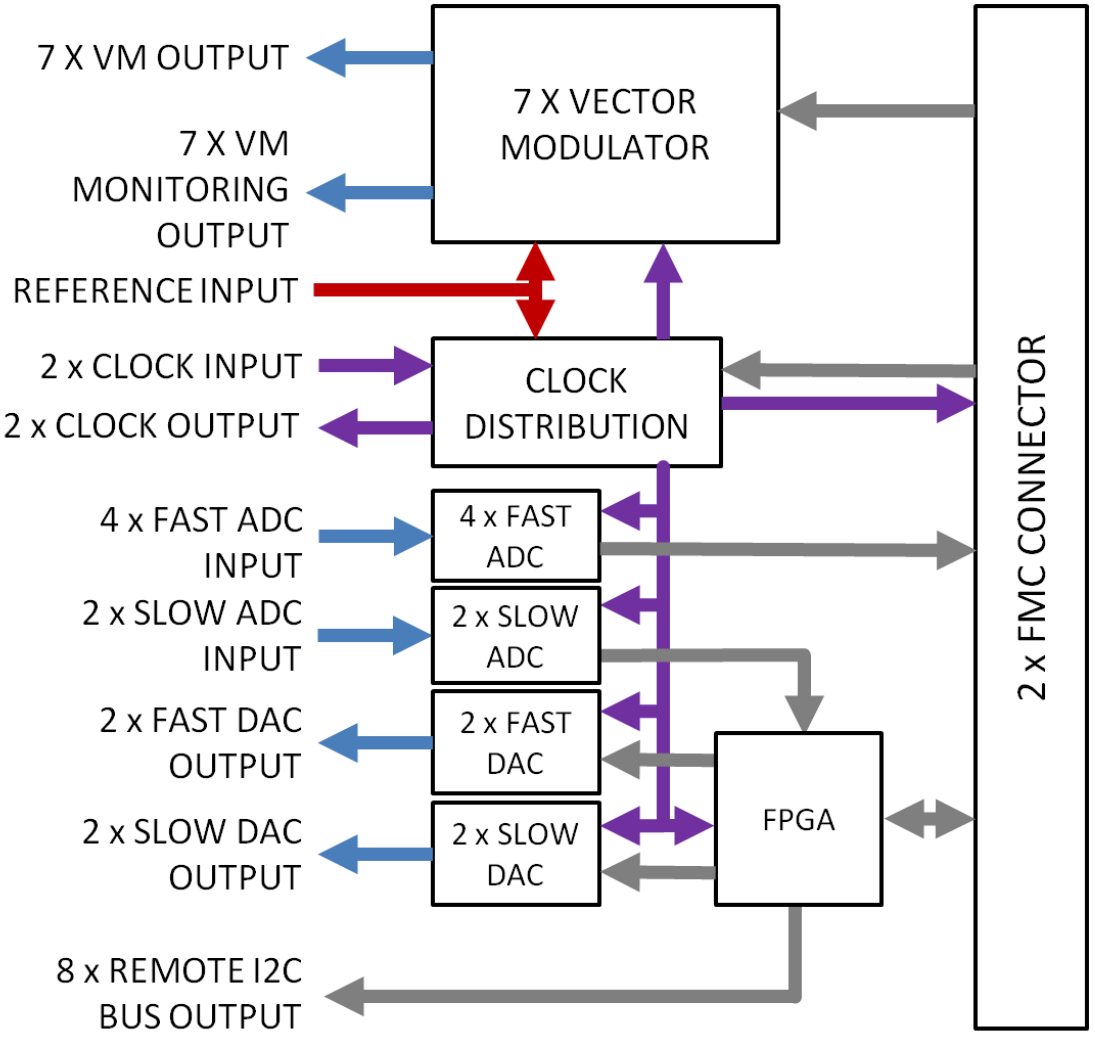


Source: https://wwws.samtec.com/standards/xilinx.aspx

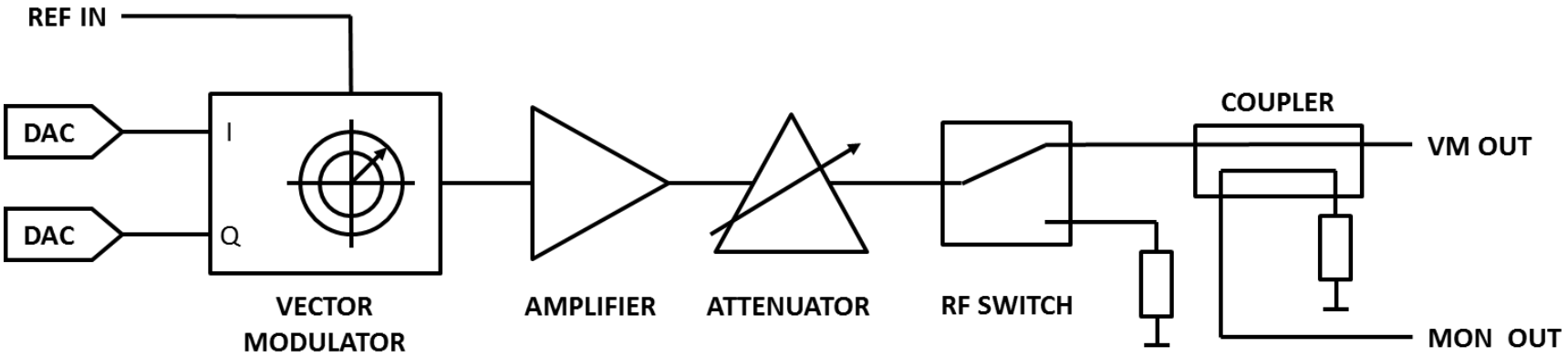
Hardware – Data Converters Module

- 7 vector modulator channels,
- 4 fast ADCs,
- 2 fast DACs,
- 2 slow ADCs,
- 2 slow DACs,
- clock generation circuit,
- reference signal distribution circuit.

Hardware – Data Converters Module



Data Converters Module – Vector Modulator



Data Converters Module – Vector Modulator DAC

Part Number	Sampling Rate [MSPS]	NSD [dBc/Hz]	SFDR [dBc]	IMD	Latency [clock cycles]
DAC3282	625 (x2 Interpolation)	-150	-64	-69	38
DAC3283	800 (x4 Interpolation)	-160	-72	-86	59
DAC5682Z	1000 (x2 Interpolation)	---	-77	-67	78
DAC3482	1250 (x2 Interpolation)	-155	-72	-77.5	140
AD9146	1200 (x4 Interpolation)	-164	-67	-81	64
AD9783	**500**	**-165**	**-80**	**-86**	**7**
AD9747	250	-165	-82	-86	7

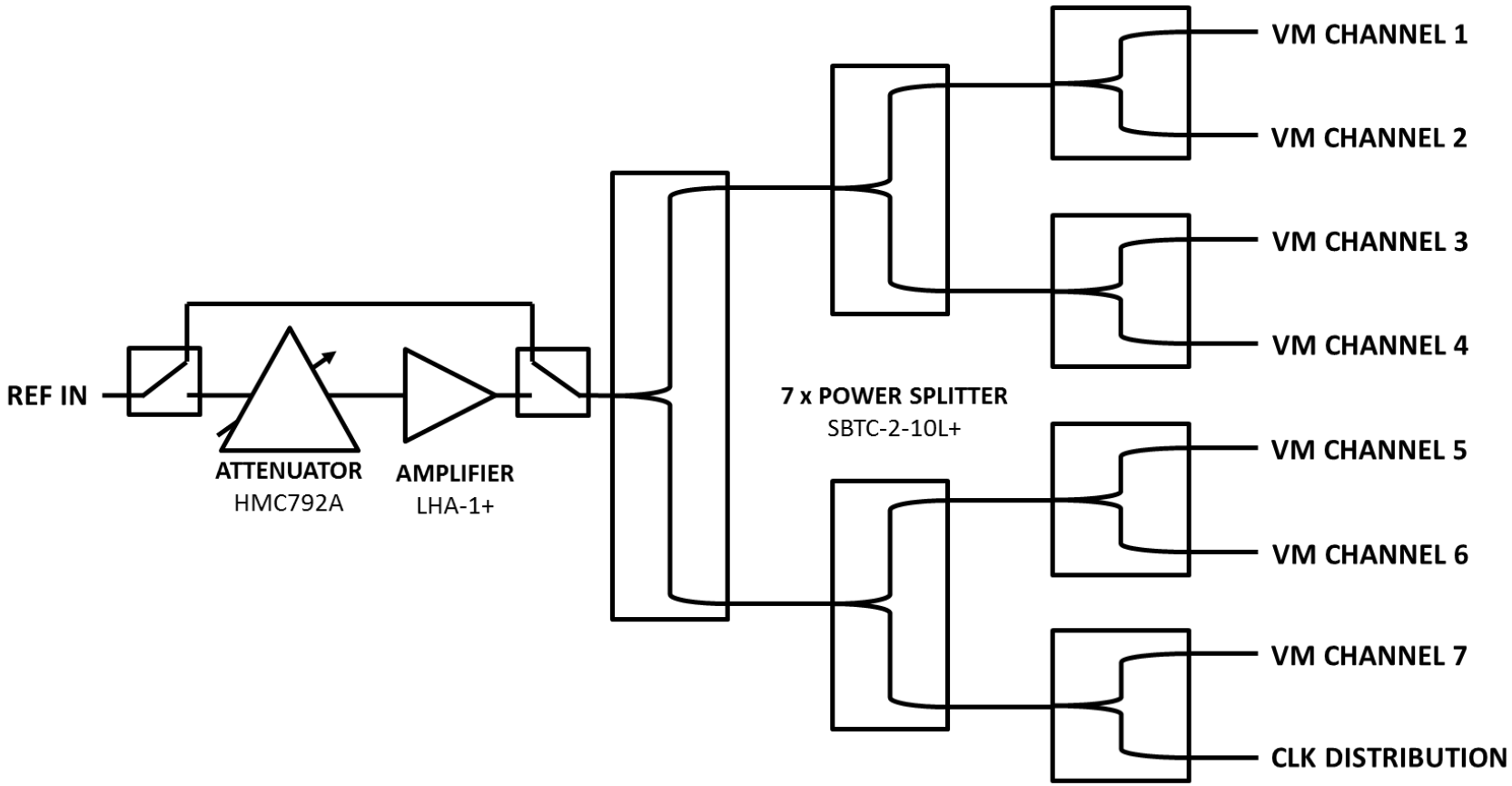
Data Converters Module – Vector Modulator Chip

Part Number	Bandwidth [MHz]	Noise Floor [dBm/Hz]	Uncalibrated Carrier Suppresion [dBc]	Uncalibrated Sideband Suppresion [dBc]	P1dB [dBm]
TRF370317	400 – 4000	-163	40	45	12
TRF370417	**50 – 6000**	**-162**	**38**	**50**	**12**
TRF370315	350 – 4000	-163	40	40	9
TRF370333	350 – 4000	-163	40	40	9
HMC1097	100 – 6000	-160	40	40	11
LTC5598	5 – 1600	-165	55	50	8.5
LTC5588-1	200 – 6000	-160	45	53	8.6

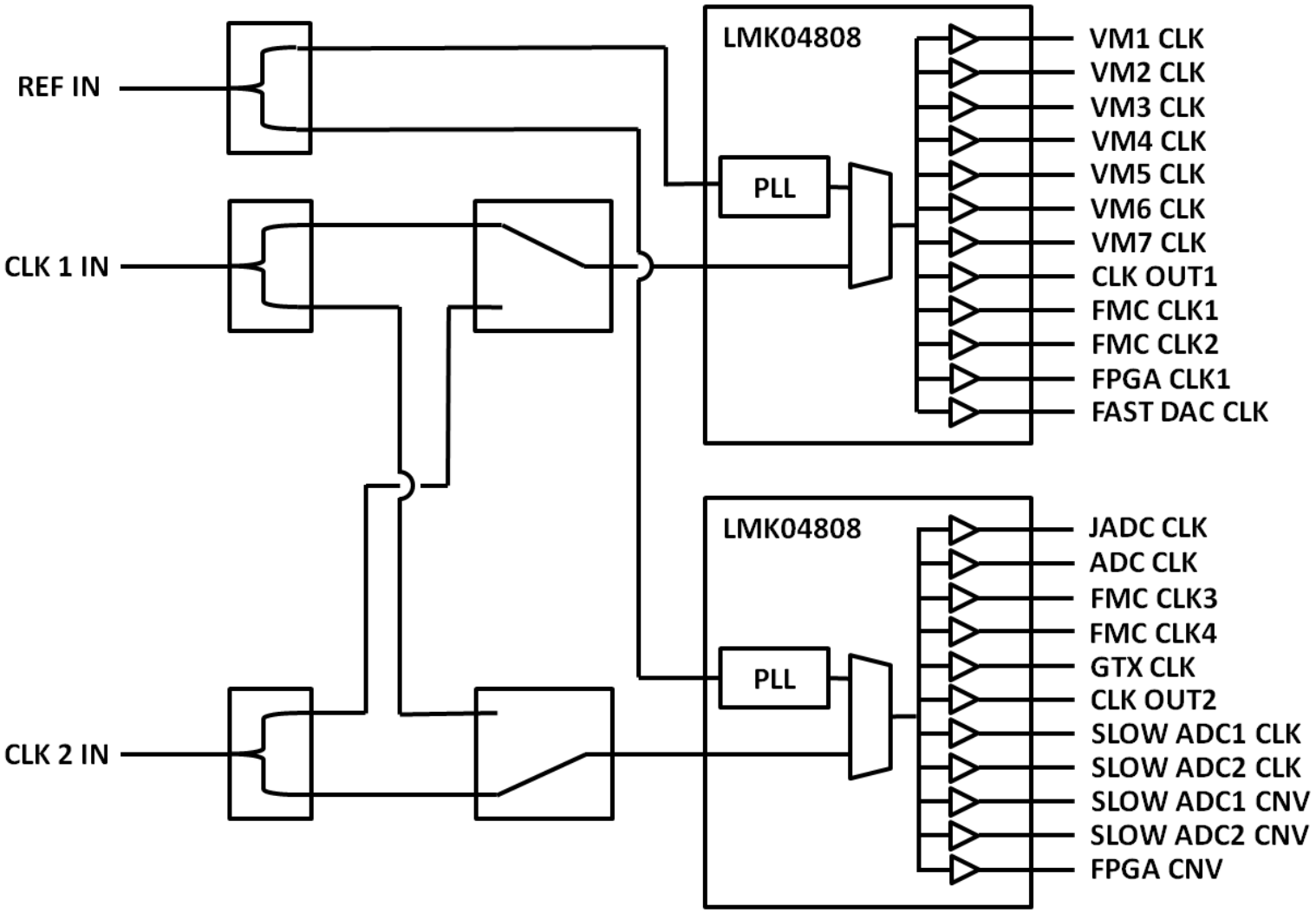
Data Converters Module – ADC

Part Number	Sampling Rate [MSPS]	SNR @ 70 MHz [dBFS]	SINAD @ 70 MHz [dBFS]	ENOB @ 70 MHz	SFDR @ 70 MHz [dBFS]	Apperture jitter [fs]
AD9652	310	75	74.6	12.1	87	100
ADS42LB69	**250**	**75.5**	**74.2**	**12 (170 MHz)**	**90**	**85**
ADC16DV160	160	76	75	-----	95	80
ADS42JB69	**250**	**75.6**	**75.3**	**12 (170 MHz)**	**88**	**85**

Data Converters Module – Reference Signal Distribution

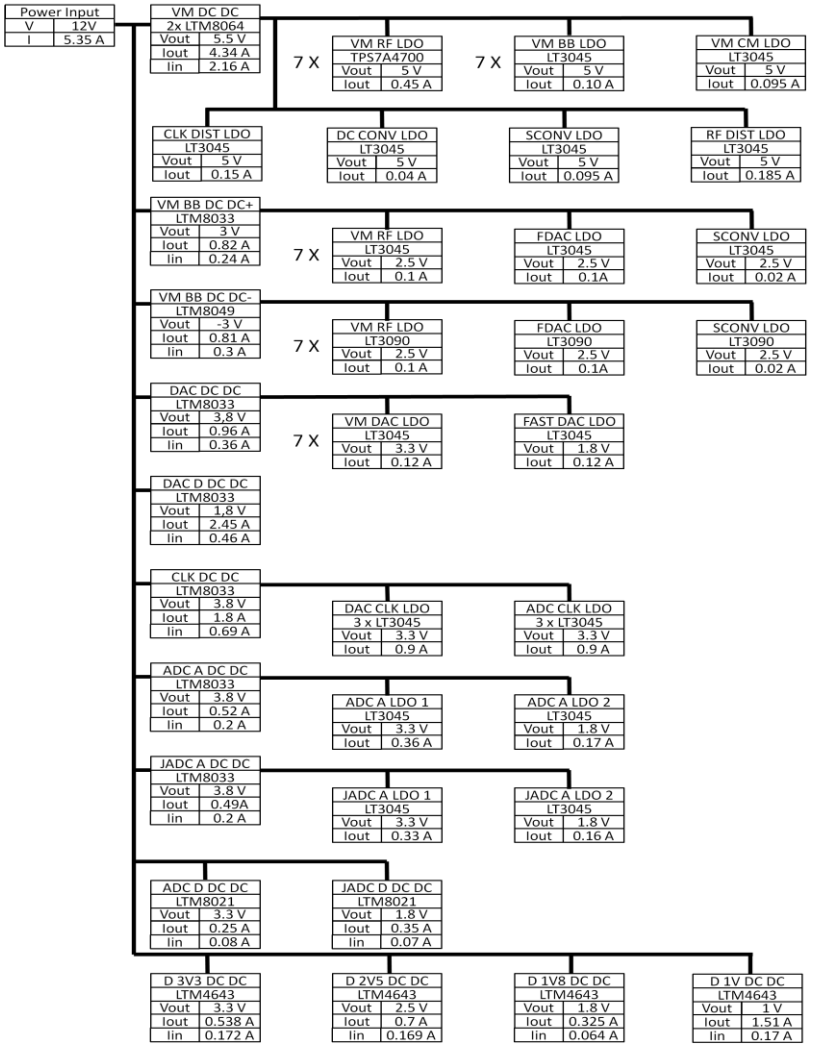


Data Converters Module – Clock Distribution



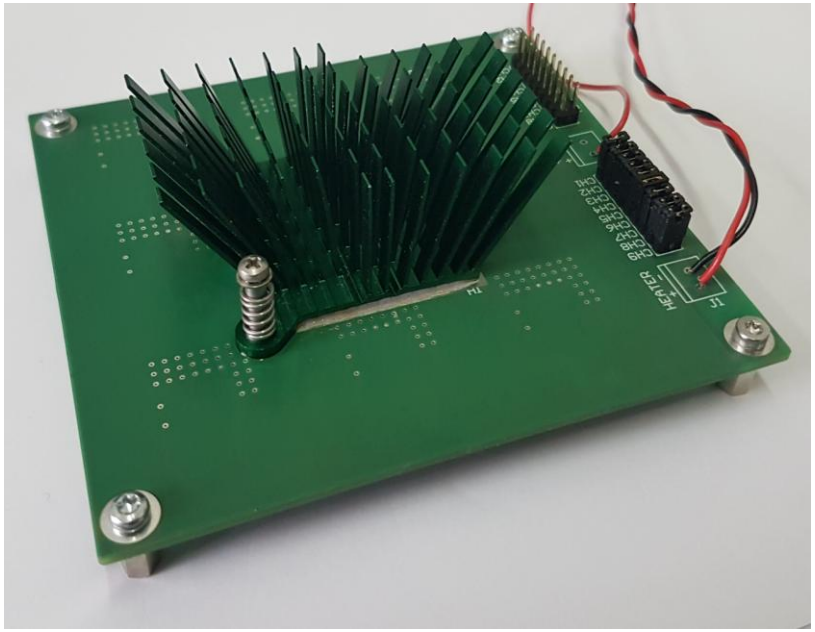
Data Converters Module – Power Supply

- Voltage: 12 V
- Input current: 5,35 A
- Power dissipation: 64,2 W



Data Converters Module – Cooling

- The power dissipation of the module is around 64 W.
- A cooling solution, utiziling BGA heatsink connected directly to GND plane was proposed.
- The board to test the cooling solution has been designed and manufactured.

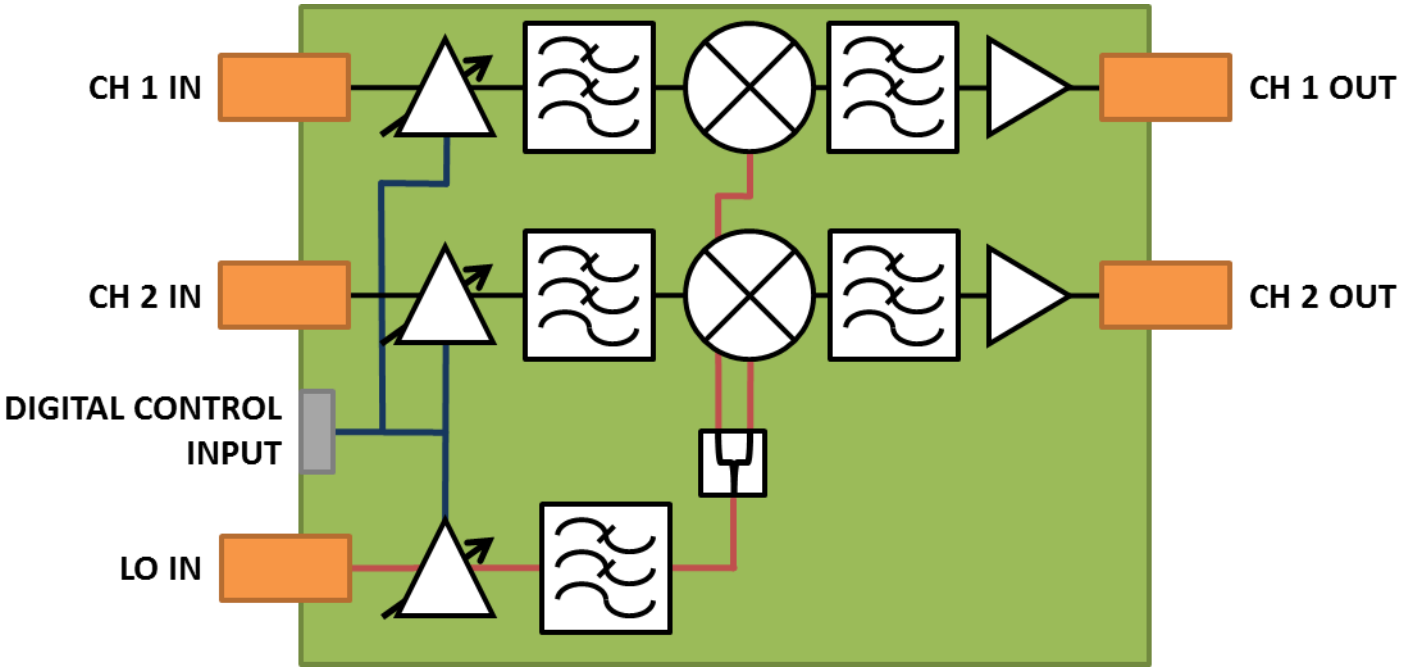


Data Converters Module – Cooling

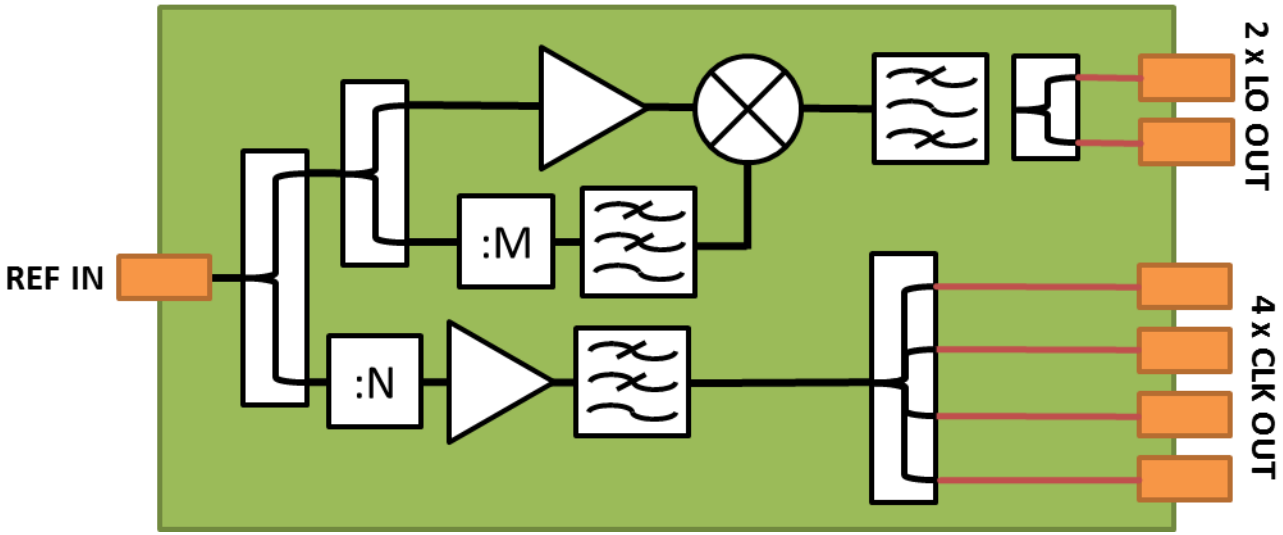
Power dissipated	No heatsink, no forced airflow	No heatsink, forced airflow	Heatsink, no forced airflow	Heatsink, forced airflow
0W	23,9 °C	23,9 °C	23,8 °C	23,8 °C
10W	85,2 °C	-	60,6 °C	-
25W	-	74,6 °C	-	50,8 °C
Thermal resistance	6,13 °C/W	2,03 °C/W	3,68 °C/W	1,08 °C/W

- The expected temperature rise for final board is:
  - Heat sink, no forced airflow: **40 °C**
  - Heat sink, forced airflow: **11.7 °C**
- For additional protection several temperature sensors are placed on board.

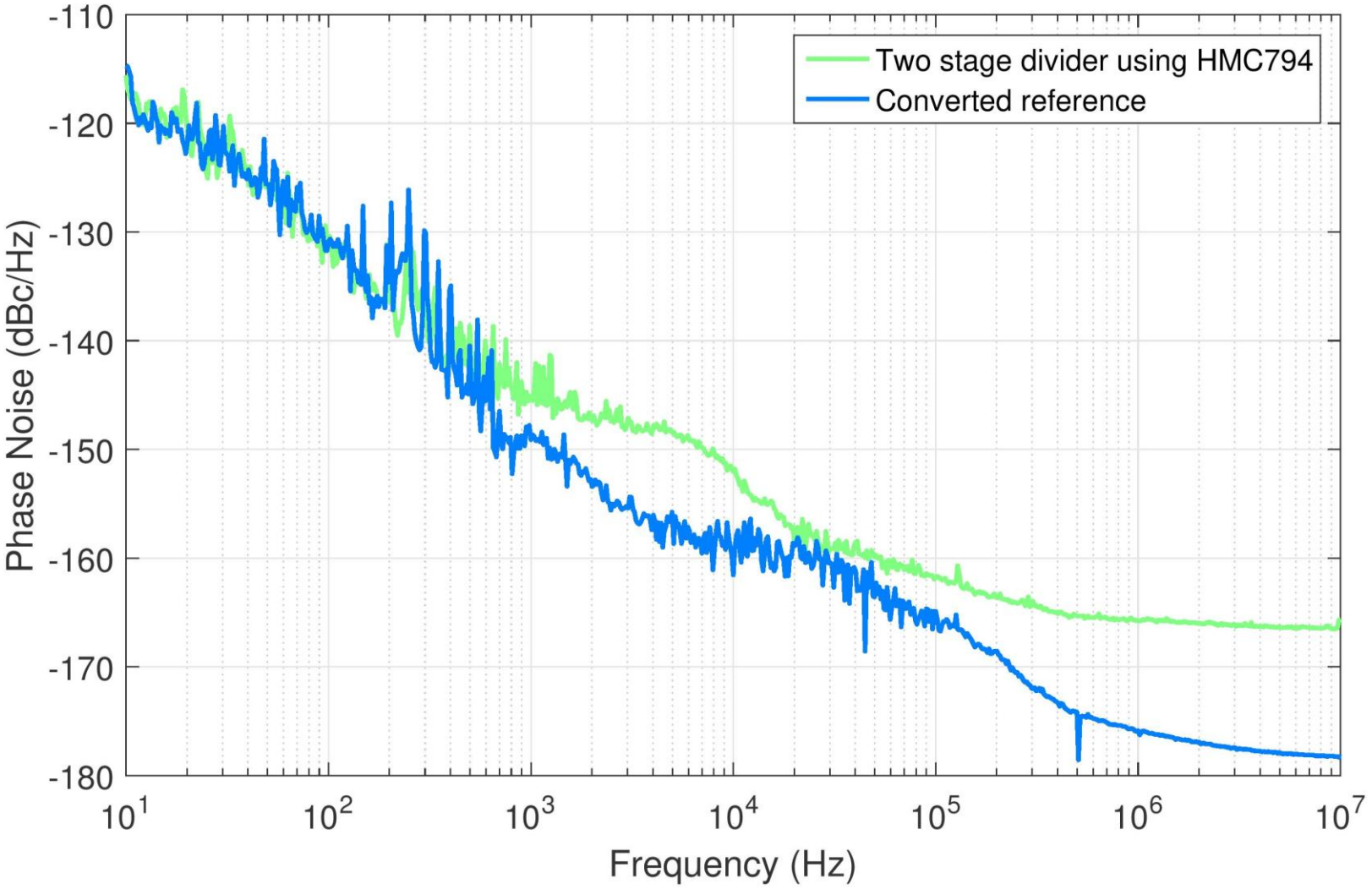
Hardware – Down Converter Module



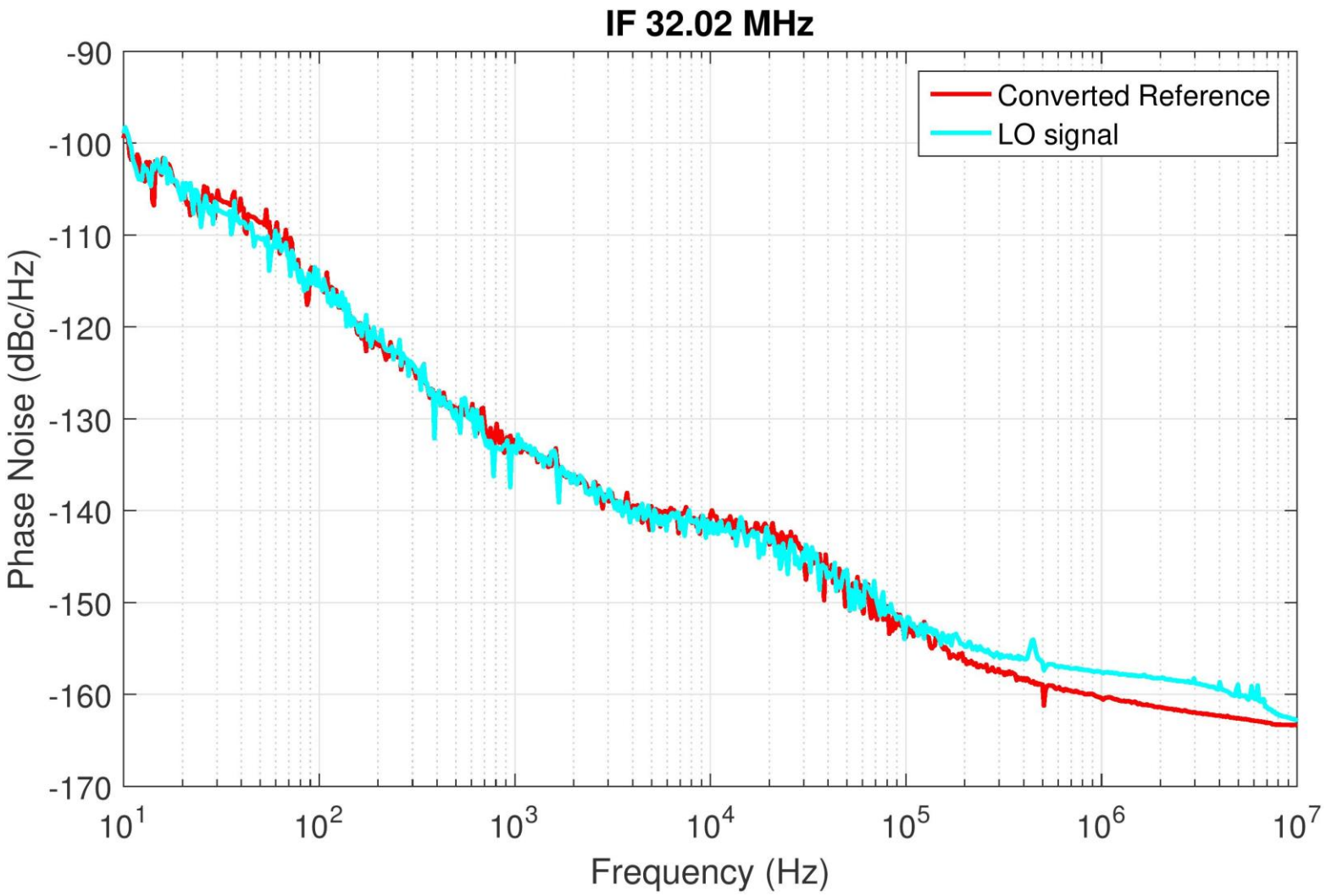
Hardware – LO Genertation Module



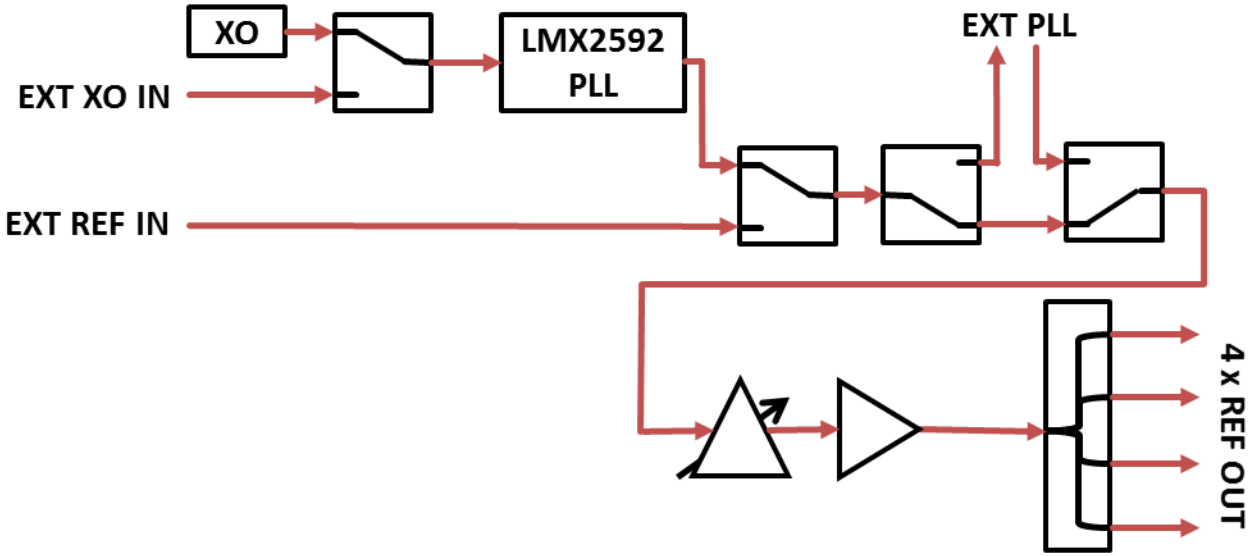
LO Generation Module - Clock Signal Phase Noise



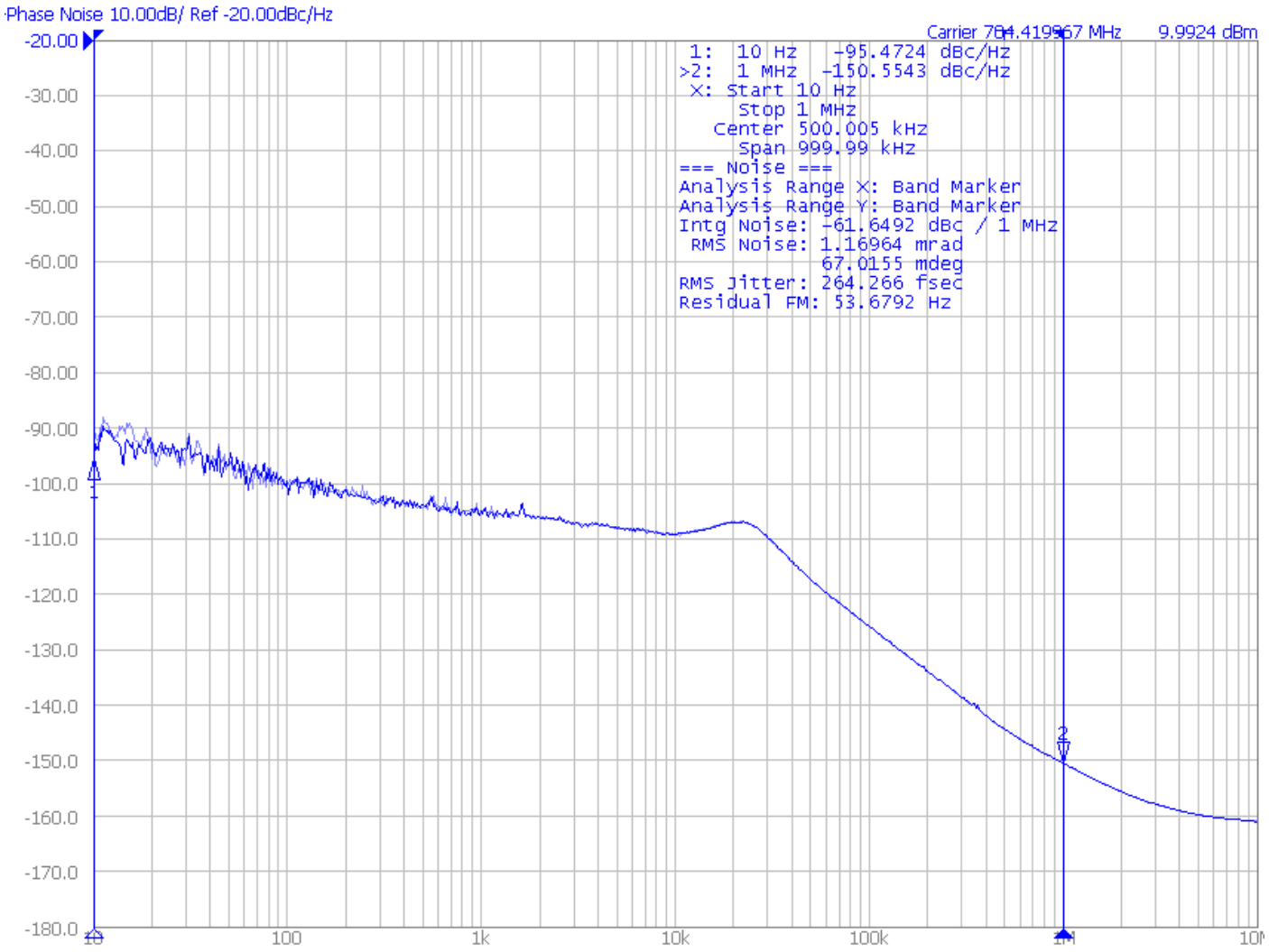
LO Generation Module - LO Signal Phase Noise



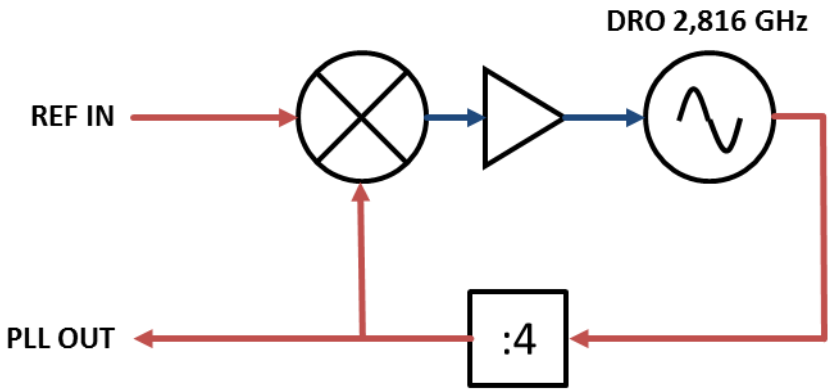
Hardware – Reference Generation Module

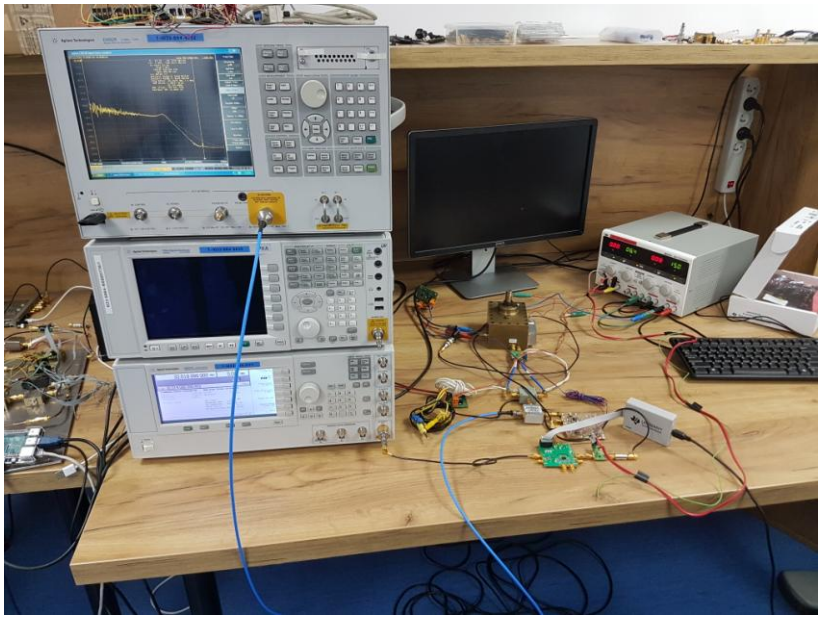


Reference Generation Module – Reference Signal Phase Noise

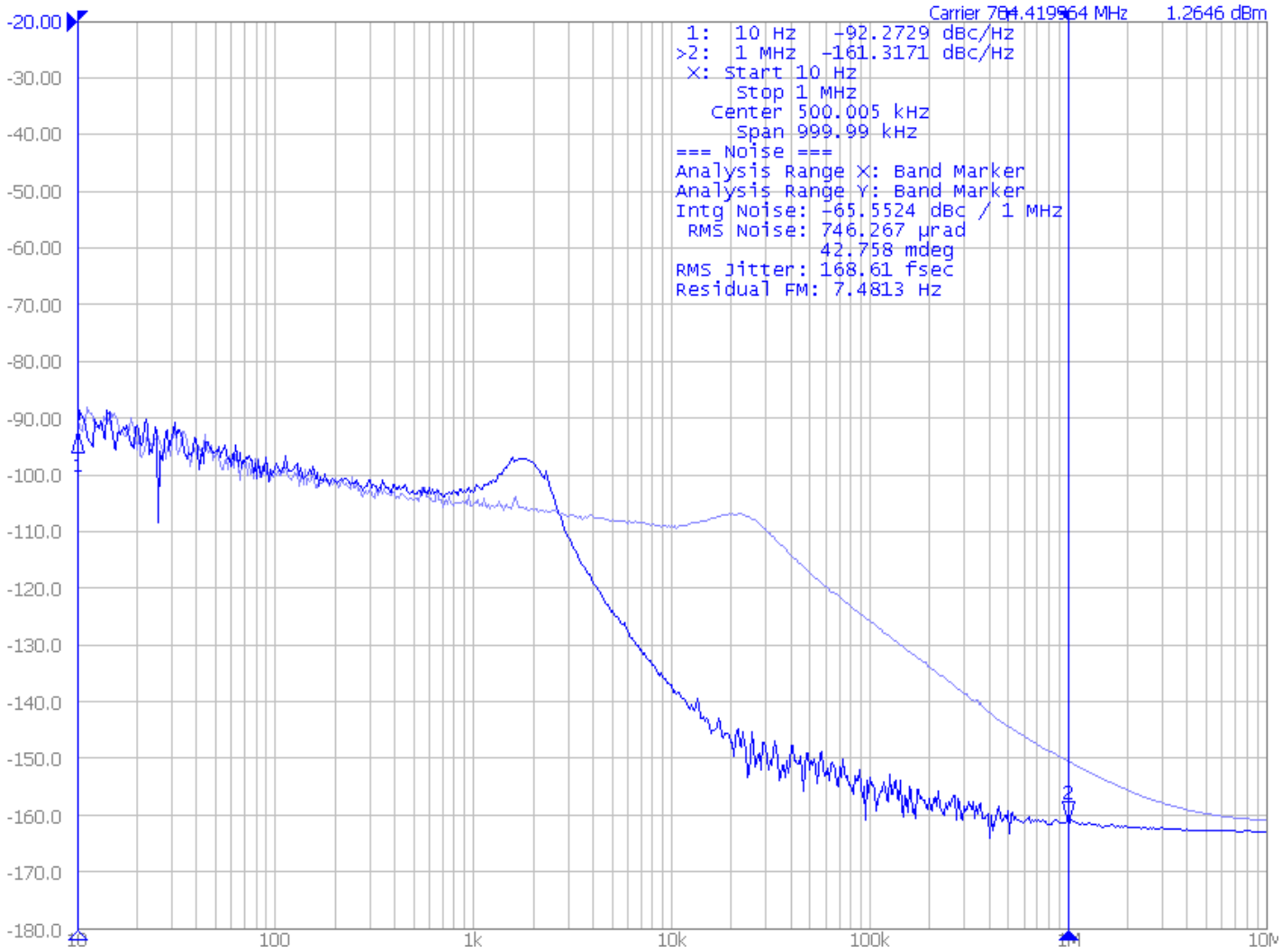


Hardware – External PLL

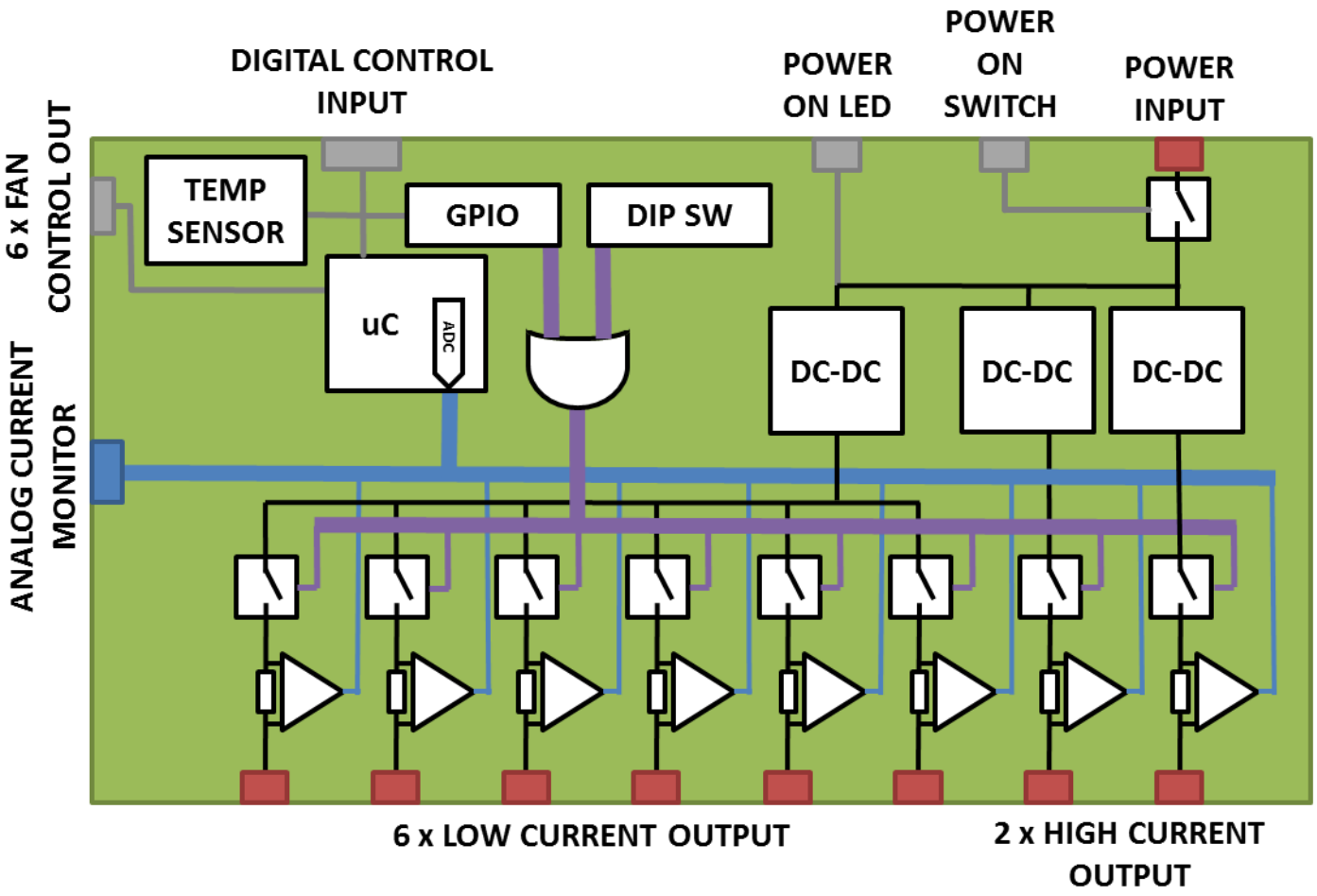




External PLL – Phase Noise Measurements



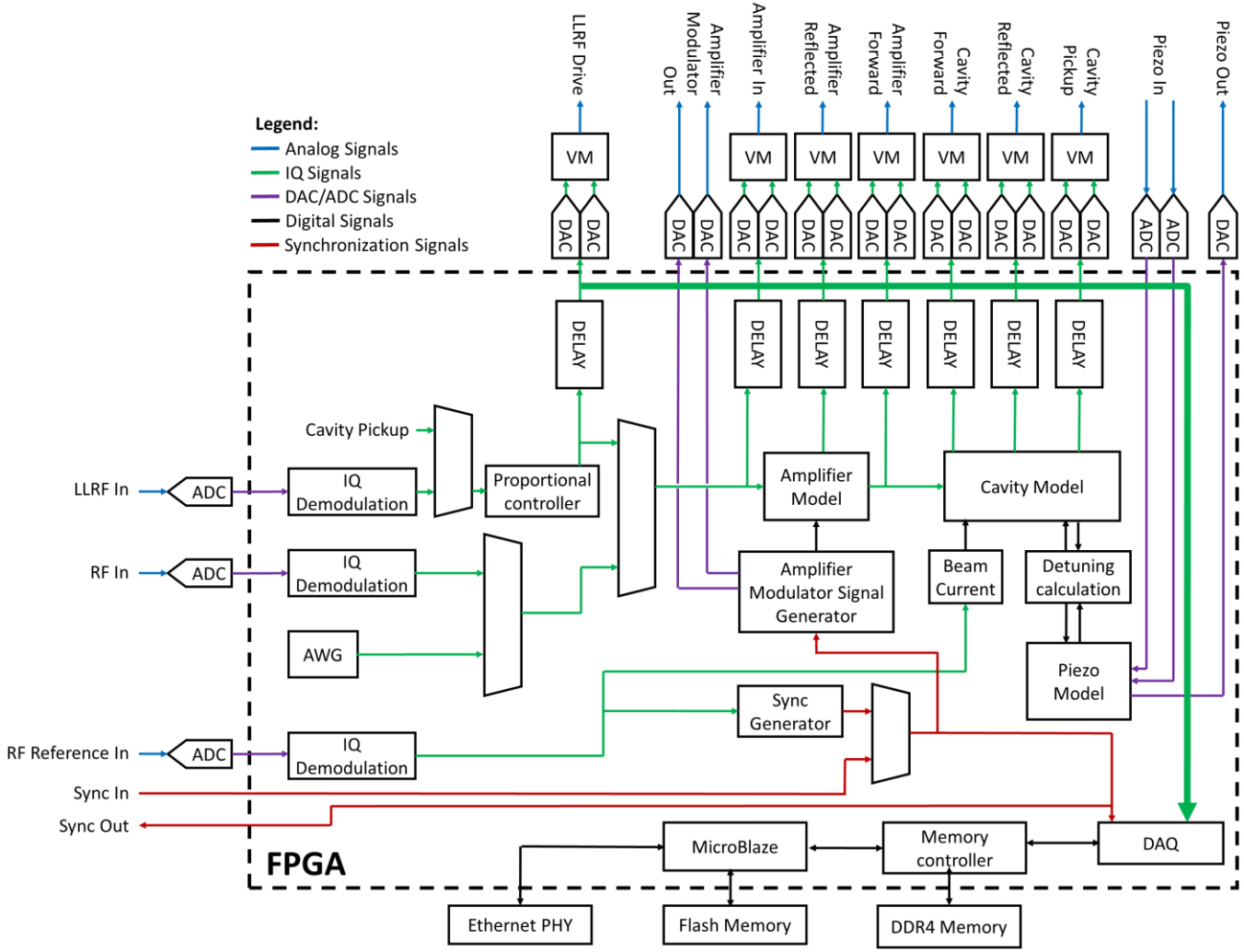
Hardware – Power Supply Module



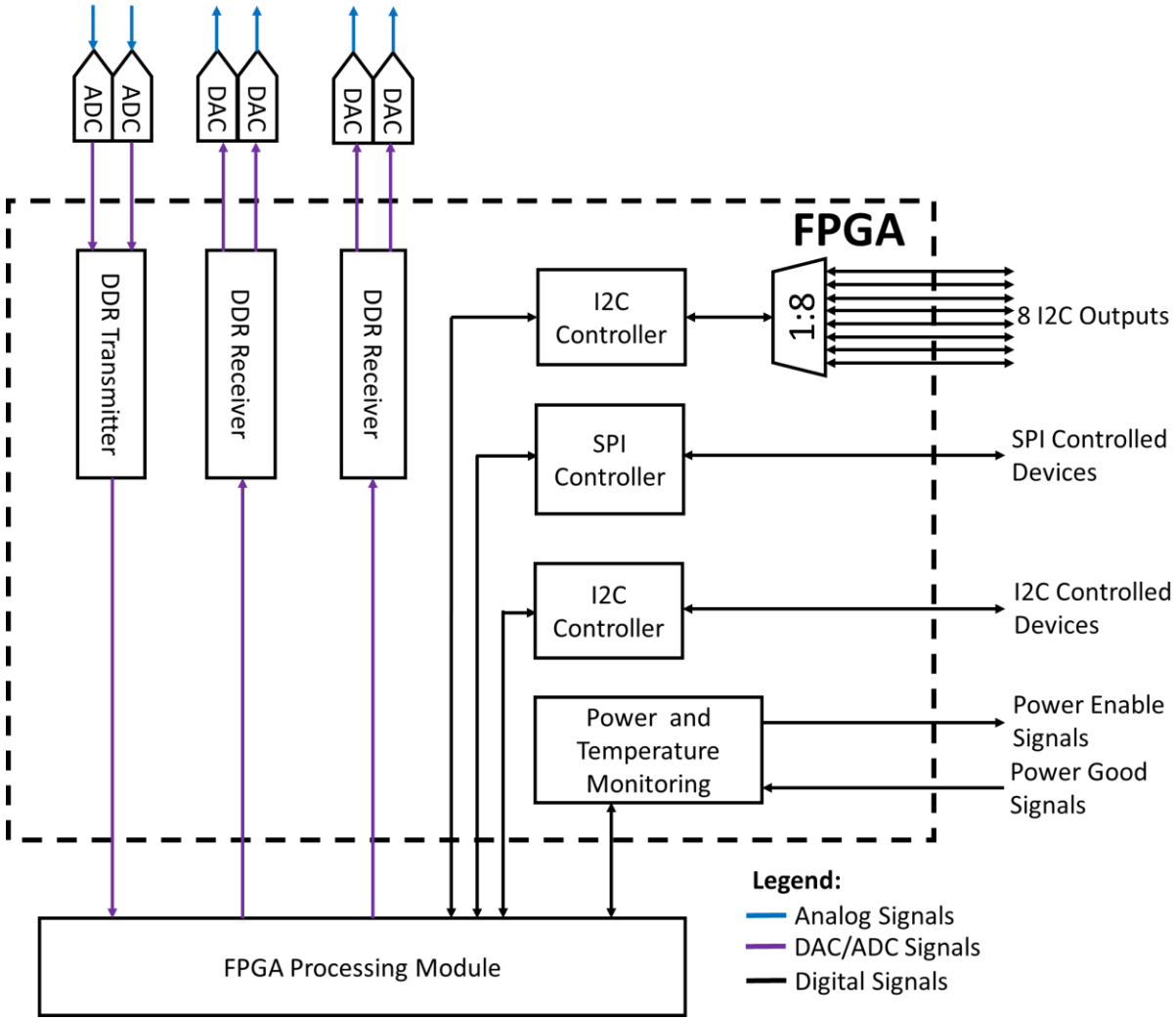
Firmware

- Two FPGAs are used in the Cavity Simulator:
  - Xilinx Kintex Ultrascale in the FPGA Processing Module,
  - Xilinx Artix 7 in the Data Converters Module.
- The FPGA Processing Module is responsible for:
  - communication with a PC,
  - gathering data from ADCs,
  - sending data to vector modulators,
  - data acquisition,
  - digital signal processing for cavity simulation.
- the Data Converters Module is responsible for:
  - communication with other modules,
  - forwarding data from slow ADCs,
  - forwarding data to DACs,
  - configuration of all modules.

Firmware – FPGA Processing Module



Firmware – Data Converters Module



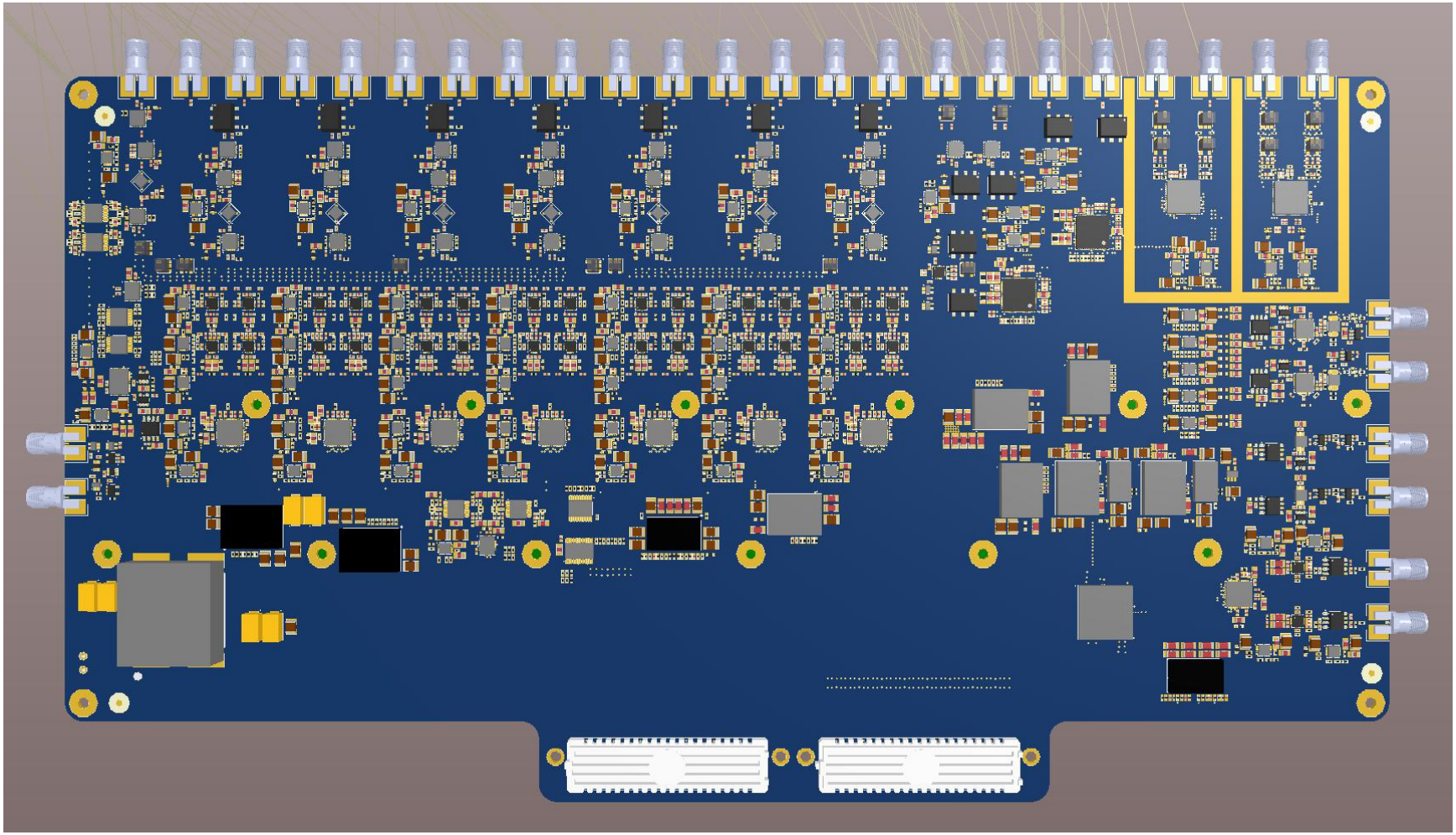
Control Software

- Two software tools are provided to control the cavity simulator:
  - Standalone application
    - Easy control over the device using graphical user interface.
  - API for integration with other systems
    - Dedicated tool for integration with complex systems, for example the LLRF systems test stand.
    - The detailed description of this tool will be ready when the final scope of test is agreed.

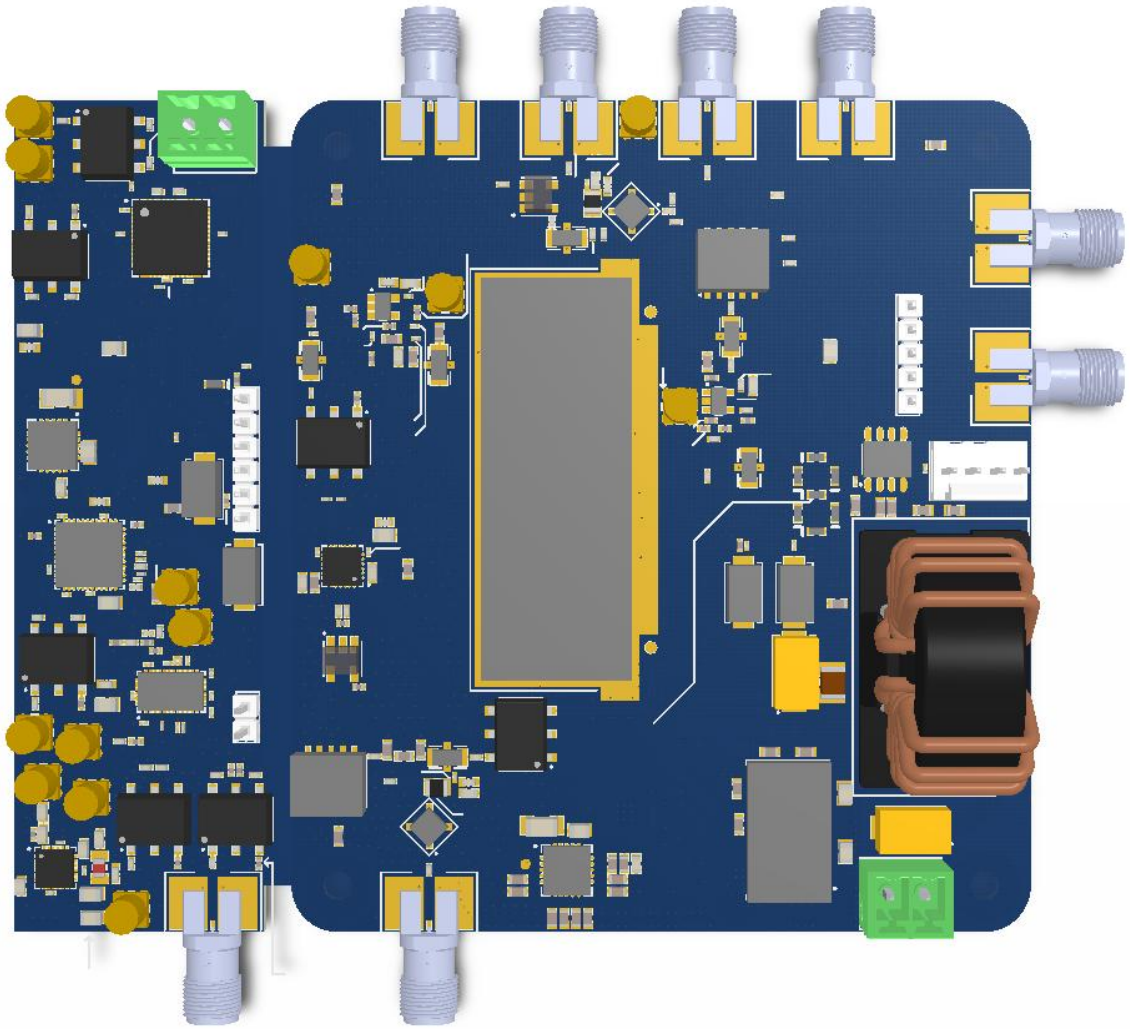
Design Status

- 4 modules are being currently under development:
  - Data Converters Module:
    - Schematics: ready
    - PCB: design in progress
  - LO Generation Module:
    - Schematics: ready
    - PCB: ready for manufacturing.
  - Reference Generation Module.
    - Schematics: ready
    - PCB: design in progress
  - Power Supply Module.
    - Main components selected
    - Performance verification in progress

Design Status – Data Converters Module



Design Status – LO Generation Module



Conclusions

- Concept of the Cavity Simulator was presented
- Measurement results of the expected phase noise of the reference, LO and clock signals were shown.
- The hardware modules design is in progress.
- The firmware development will start after the Data Converters Module design is ready.

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Thank You