EUROPEAN
SPALLATION
SOURCE

Control/Timing Demonstrator

IKON13
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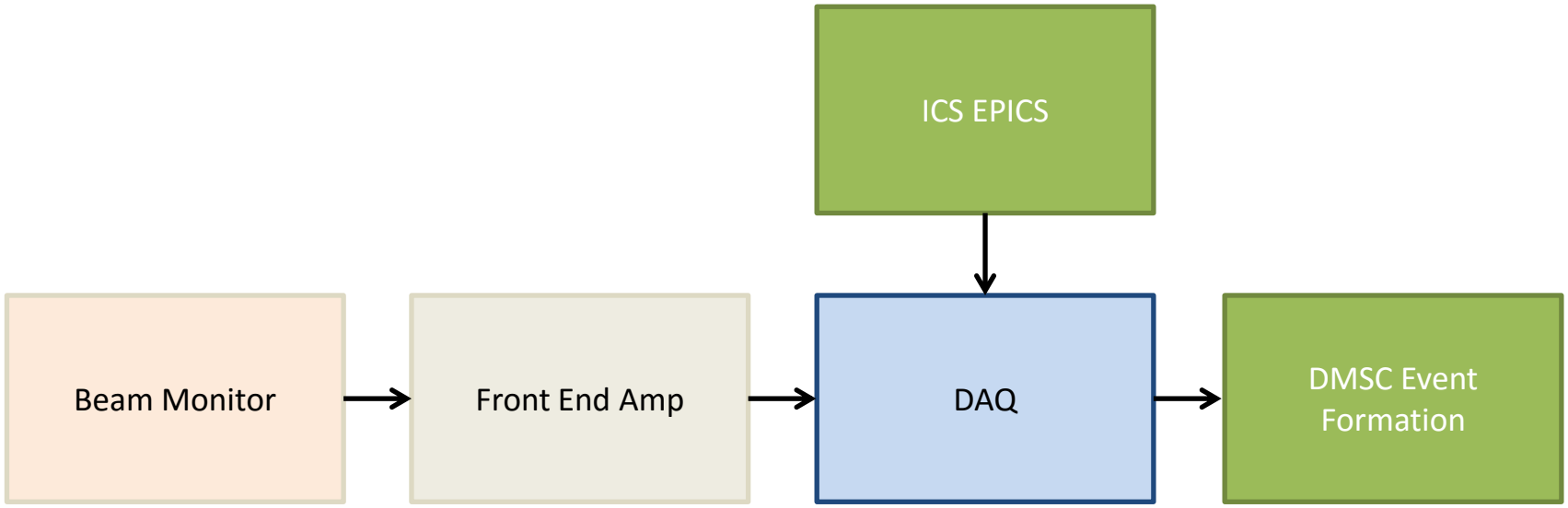
Steven Alcock (DG)

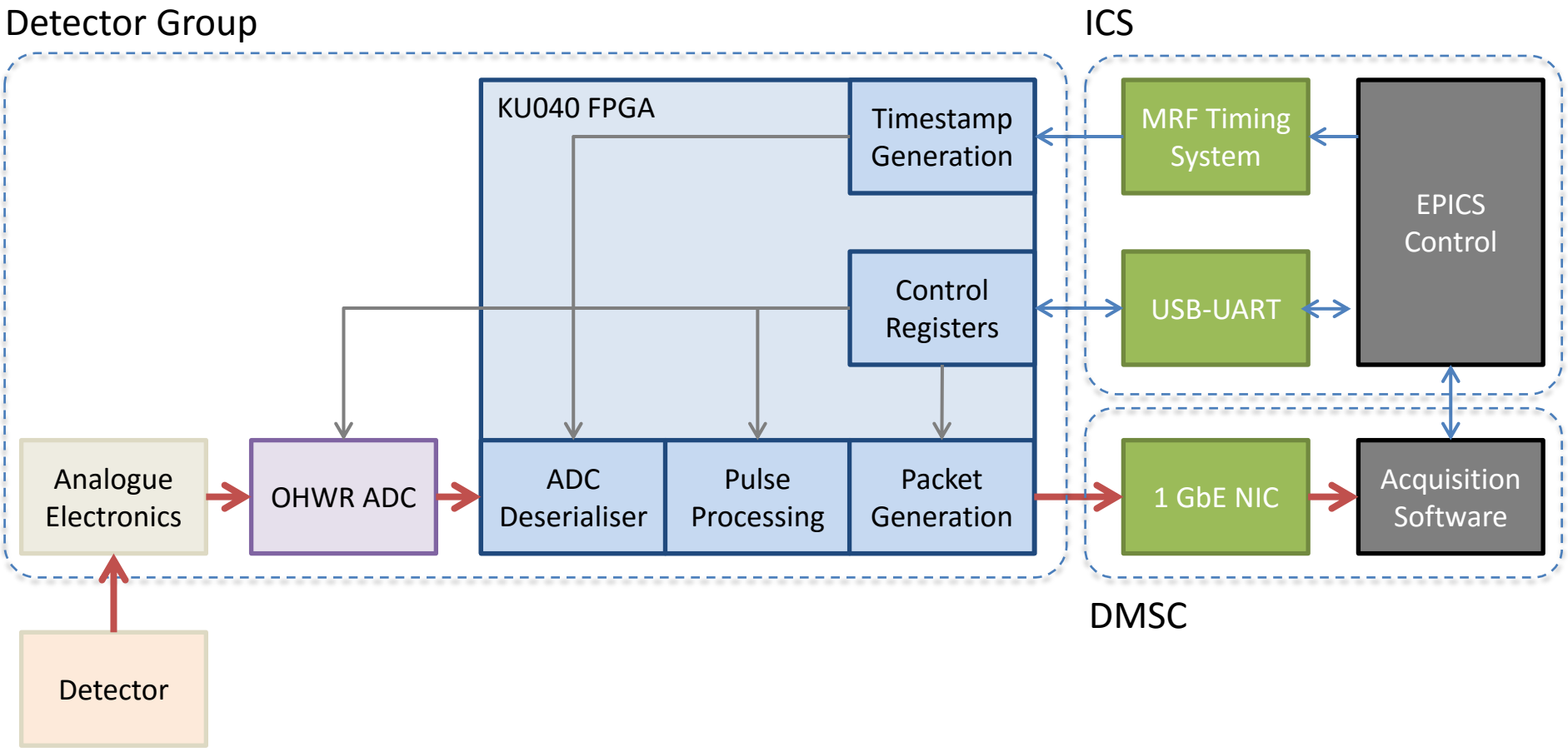
Motivation

- ESSIIP is an ICS project for developing and evaluating integration for relevant stakeholders (Detector Group, Choppers, Motion Control, Sample Environment, and the DMSC) – David Brodrick is coordinating this.
- Detector Group Readout produced a system to prove ICS interfaces (synchronous time distribution and control).
- The resulting system provides ADC readout for a small number of channels and hence could be used for evaluating beam monitors or other detectors.

ESSIIP ADC Readout Demonstrator Architecture



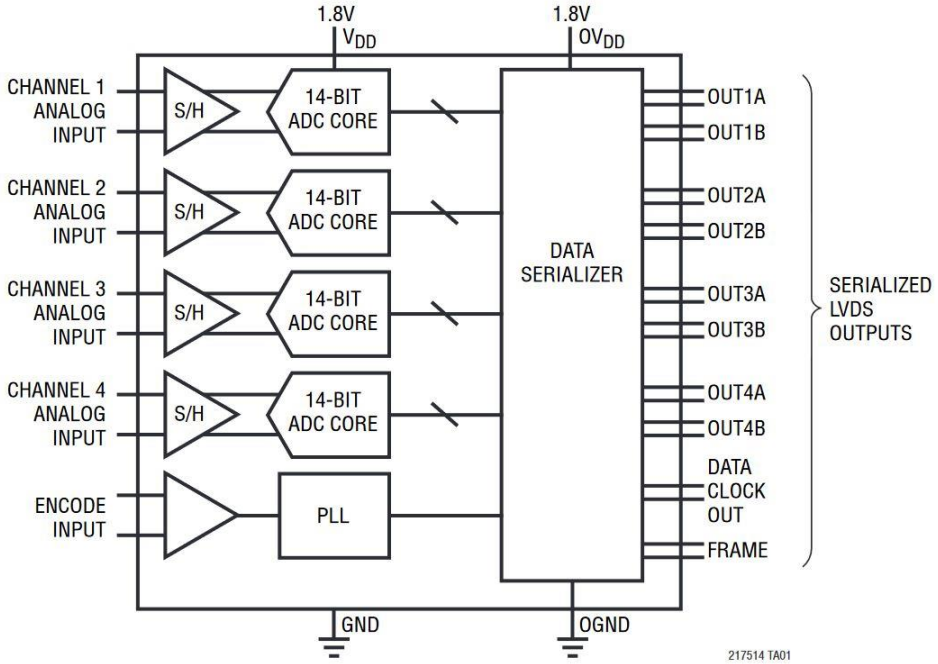
ESSIIP ADC Readout Demonstrator Architecture

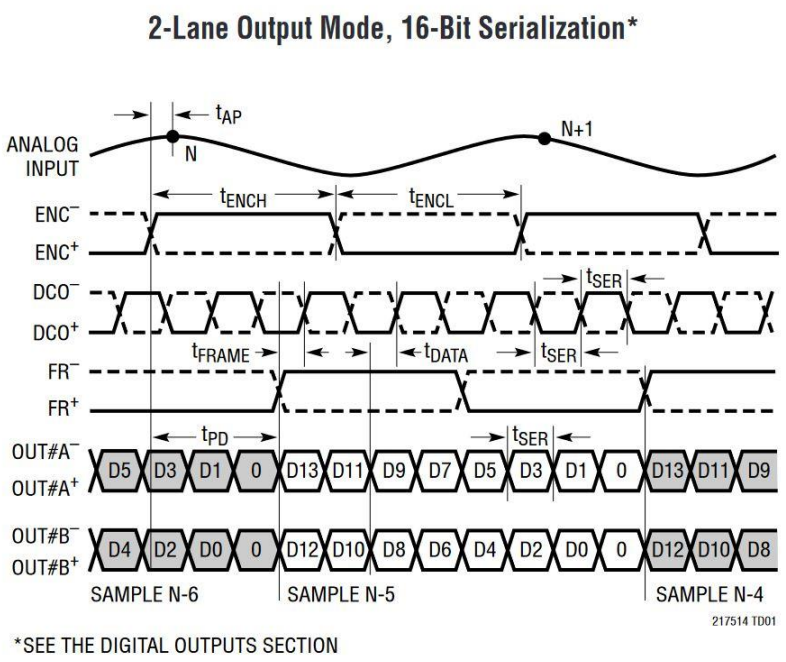


Key Features

- ADC
  - Open Hardware (CERN) design
  - Four channels, 30 MHz analog bandwidth
  - 14-bit resolution
  - 105 MHz sample rate – we use 44 MHz from ICS timing system
  - Programmable gain and offset
  - FMC connector to FPGA.
- FPGA
  - Avnet KU040 development board
  - Configurable pulse detection/zero suppression to reduce data rate
  - Maximum pulse length of 65,536 samples (1.49 ms)
  - Channels read out pairwise depending on pulse activity
  - Synchronous clocking and timestamping from ICS reference signals
  - Custom readout protocol sent via standard Ethernet/IP/UDP.

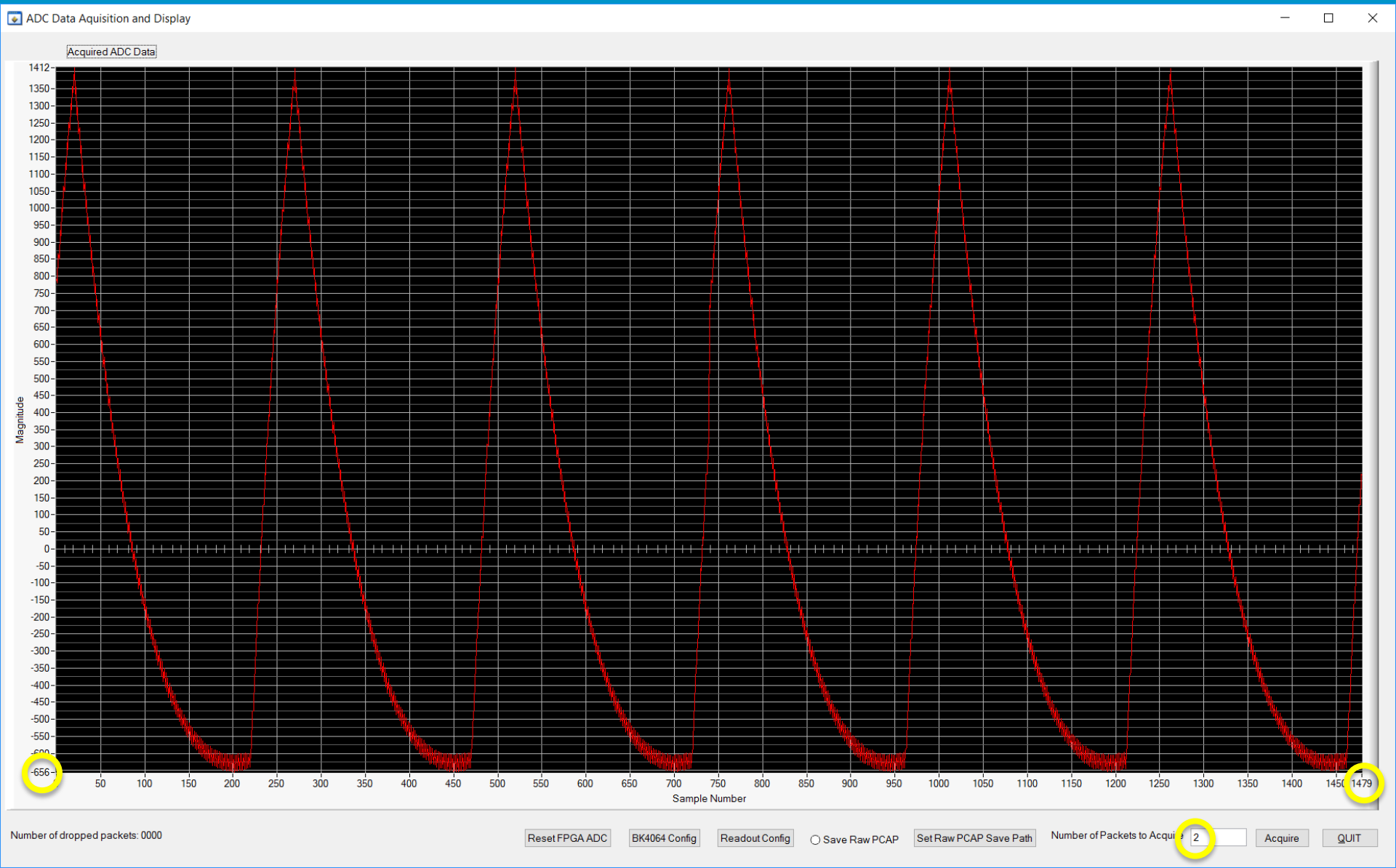
Linear Technology LTC217X-14 ADC



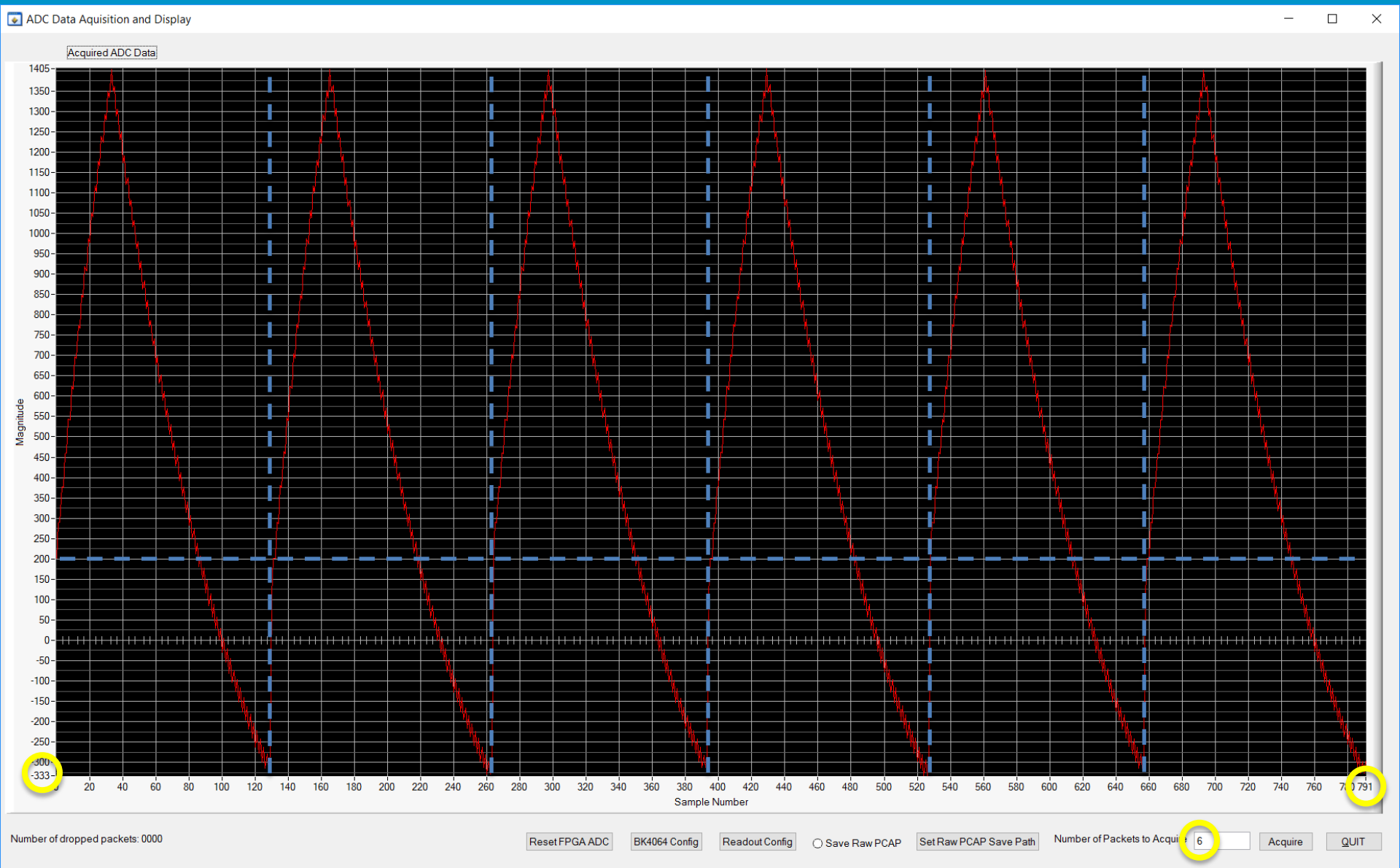


*SEE THE DIGITAL OUTPUTS SECTION

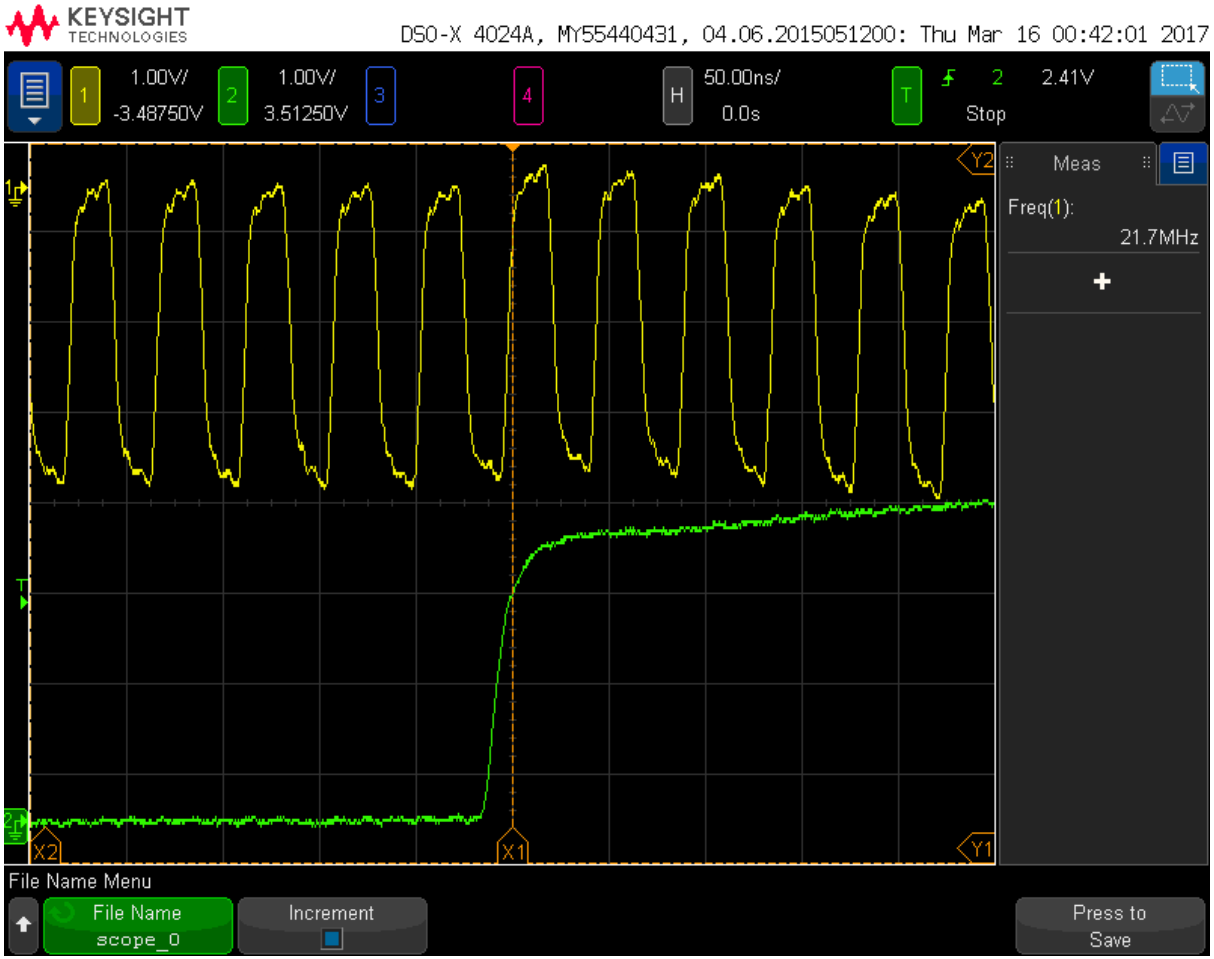
Zero Suppression (1/2)



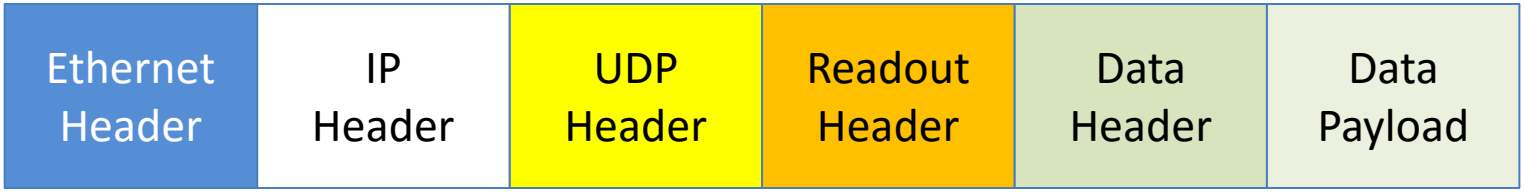
Zero Suppression (2/2)



Timestamp Signalling



Data Packing



- Same as 100 G Demonstrator, but with meaningful data headers and payloads.

Type	Word Count
Sequence	Index
Header Magic Word (0xABCD)	Pulse Width (in samples)
Channel Number (0, 1, 2, 3)	Fragment Count
Fractional Timestamp High	Fractional Timestamp Low
Sample 0	Sample 1
…	Sample n-1
Trailer High (0xBEEF)	Trailer Low (0xCAFE)

To Do List

- Automatic ADC calibration
- Timestamp accuracy verification
- ADC resolution verification
- Software processing and data visualisation
- Readout of all four channels (implemented but not tested)
- Integration and test with a real detector.

Conclusion

- The system can provide synchronous readout for a small number of ADC channels.
- The control and timing interfaces from the ICS EPICS environment have been proven.