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FC Front-End Design Document

Carlos de la Cruz

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Project: MEBT FARADAY CUP

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Change History

Rev.	Date	Author(s)	Description
0.1	May 4, 2017	C. de la Cruz	First version.
0.2	May 4, 2017	C. de la Cruz	References compilation and minor changes.

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1 Introduction

The Faraday Cup purpose is to stop the pulsed beam as well as to measure the total beam current. The current generated by the beam in the cup should be converted into a voltage signal capable to be read tens of meters away (in the gallery) by the digitizer. That signal conditioning is made by the Front-End Electronics, which is required to accomplish the specifications agreed in [1]. A summary of these specifications can be observed in Table 1.

Table 1: FC Front-End Specifications.

Parameter	Value
Beam peak current	62.5 mA
Dynamic range	10
Slow Tuning Mode [2]	50 µs & 1 Hz
Fast Tuning Mode	5 µs & 14 Hz
Sample frequency	>= 2 MHz
Total measurement error	< 0.1 mA
Measurement precision	σ < 0.01 mA
Output voltage	Differential $\pm$10 V
ADC Resolution	16 bits
Repeller power supply	0 to -1000V

Designing high-resolution detection circuits for low currents supply presents considerable challenges because bandwidth, gain, and noise are strongly coupled.

2 Cabling and connections

The cabling and connection layout of Figure 1 has been proposed for the FC System. The scope of this section is to describe just the components that comprise the path of the signal (1A, 1B, 1C 1D).

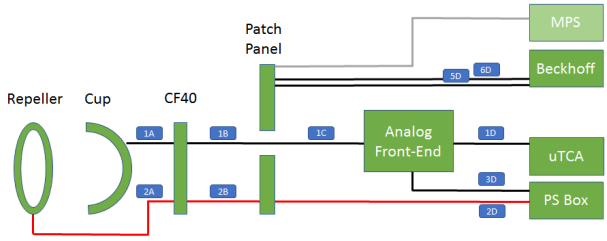

Figure 1: Cabling scheme of FC System.

At first, a screwed connection is going to be attached in order to the cup to collect the current.

For the vacuum area (1A), radiation resistant kapton coaxial cable has been selected (Allectra 311-KAP50-RAD or similar). The stray or parasitic capacitance depends on the length by 65 pF/m and is an important parameter because it may limit the total bandwidth of the system. The length of this cable will be the distance from the flange to the grid plus the actuator stroke, that is around 0.5 m. A CF40 flange including a SMA feedthrough is proposed.

The signal cable in air (1B) is coaxial halogen-free (Flamex RG174 or similar). The same cable pass through the Patch Panel (1C) in order to avoid an intermediate connection, but it is attached to the panel by a cable gland. The Patch Panel is located at the base of the Faraday Cup Actuator and the Analog Front-End box is attached to the structure of the Linac no more than 3 m away from the FC. Stray capacitance of this cable is 106 pF/m.

Coaxial connectors like BNC or SMA are expected to have at input and

output of the Front-End. The output voltage signal is driven to the digitizer, around 30 m away in the Gallery, by a coaxial low losses cable (1D) Huber+Suhner S 12272-04 or similar halogen-free cable .

3 Circuit Design

As the cup is isolated and floating, the collected current can be treated as a high-resistance current source.

The current to voltage conversion circuit might be a simple resistor. In a steady state, the voltage drop divided by the resistor value stands for the current collected by the cup. However, this circuit has some drawbacks that can be solved with a transimpedance conversion made by an amplifier [3]:

- The resistor creates a positive voltage in the cup in every pulse. If the voltage level is not controlled, the power to dissipate might be higher than the withstanding of the materials.
- According to the literature, a parasitic capacitance might appear in the cup. Values might vary between 10 pF [4] and 3.5 nF [5]. That capacitance is added to the cables and connections contribution to limit of the bandwidth.
- Less accuracy of the measurement due to the tolerance and thermal noise of the resistor.

The schematic of the Front-End circuit proposed, designed in Altium Designer, is shown in Appendix A. In following sections, each functional part of the schematic is described.

3.1 Input protections

Usual ways of damaging amplifiers with input voltage are ESD (electrostatic discharge), common mode overvoltage (voltages outside supply

range even if the power supplies are turned off) and differential input overvoltage [6].

Studying the case of the FC Front-End, a TVS (transient voltage suppressor) made of back to back diodes is needed to protect the first op amp against quick voltage swings across its input pins. BAV199 limits the voltage to around ± 1 V at the input, protecting the amplifier, but also not allowing a large amount of collected charge to remain at the cup in case of failure or temporal disconnection of the Front-End.

Before that, a common mode line filter WE-SL1 has been placed to reject noise comming from the input.

3.2 Amplifiers selection

Although there are no special requirements for radiation environment, the amplifiers selected are Analog Devices proprietary XFCB process, specially developed for radiation withstand [7].

AD8397 [8] is a fast operational amplifier capable of driving heavy loads with excellent linearity. It's selected as preamplifier for the current to voltage conversion stage. Most of fast amplifiers can not handle the high output current needed for the FC application.

AD8066 [9] is a dual voltage amplifier with JFET inputs, high performance and low noise operation. One of the amplifiers is used as voltage buffer with no amplification. The other is arranged to work as low pass filter and ADC driver as well.

3.3 Transimpedance and amplification

Considering the nominal current (62.5 mA) plus a significant margin, and matching the result with the full scale value (10 V), the total gain (G), defined by the ratio V_{OUT}/I_{IN} is 100. That means a sensitivity of 10 mA/V.

In the first stage, there is a current-to-voltage gain of 50, given by the first feedback resistor. Its value is a balance between a high gain limiting total bandwidth and low gain degrading signal to noise ratio. The related capacitor feedback should give stability to compensate the input capacitance created by cables and connectors. According to [10], this value is obtained from the relation:

$$C_F = \sqrt{\frac{C_{IN}}{2\pi(GBWP)R_F}} \tag{1}$$

,where:
C_{IN} is the total input capacitance, calculated with the data of Section 2
$GBWP$ is the operational amplifier gain bandwidth product
R_F is the feedback resistor

The second stage is just a buffer with a voltage gain of 2. This amplifier presents also an inverted configuration so at the end of these stages the signal has the same polarity than the input.

3.4 Low pass filter

At the end of the line, there is an active low-pass filter. It is second-order butterworth type and it is designed to attenuate -20 dB/dec after the theoretical cut-off frequency of 2.5 MHz. This target frequency has been selected to be higher than the final required one, but lower than the noise gain's zero [11]. The objective is to attenuate non-desired frequencies of the signal as well as to cancel high frequency noises.

3.5 Grounding

There are two different grounds in the circuit, as it can be observed in the drawing of Figure 2.

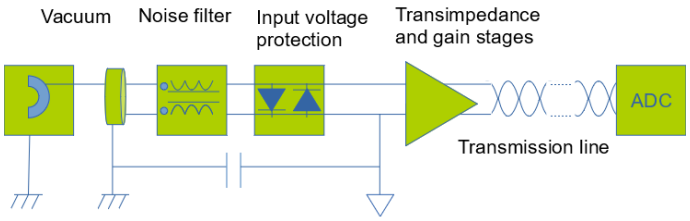

Figure 2: Drawing of FC System grounding.

The Beam Ground corresponds to the accelerator machine. It comes into the circuit through the shield of the input cable, which is connected to the vacuum flange. It is considered an *unclean* ground. Because of that, it is decoupled from the *clean* ground, called the Circuit Ground, by a 33µF capacitor.

The Circuit Ground is taken from the central point of the supply rails, and is generated inside de circuit by the OP07 amplifier, not coming from the Back-End (where power supplies are located).

4 Simulations

The simulation software used to support the design calculations is LT-Spice, provided by Linear Technologies. The basic schematic used for the simulations in shown in Figure 3 and the complete code is in Appendix B.

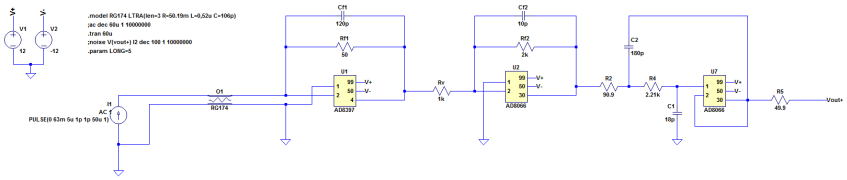

Figure 3: LTSpice schematic for the Front-End simulations.

The incoming signal that emulates the charge collected by the cup is represented by a pulsed current source. The input cable is modeled as a lossy transmission line, where cable characteristics are parametrized. The model of each amplifier has been downloaded from the manufacturer's website. Positive and negative DC voltage power sources are selected as the amplifiers bipolar power supply.

4.1 Step response

The pulsed current source is configured as the maximum, minimum and nominal beam pulse, with with the corresponding amplitude and 50 µs of duration. Rise and fall time of this pulse is 1 ps and cable length is set to 3 m. The output profiles of the signal can be observed in Figure 4 and the main measurements are in Table 2.

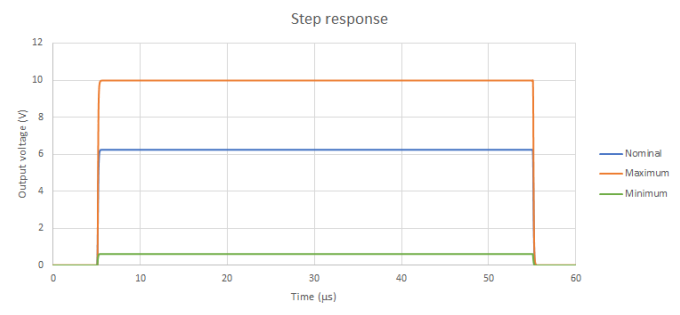

Figure 4: Simulated step responses.

Table 2: Measurements in step response simulation.

Parameter	Max. input	Nominal Input	Min. input
Input current	100 mA	62.5 mA	6.25 mA
Output voltage	9.98 V	6.245 V	0.624 V
Rise time	146 ns	136 ns	134 ns
Fall time	146 ns	136 ns	134 ns
Overshoot	None	None	None
Offset	4.12 mVpp	4.12 mVpp	4.12 mVpp

4.2 AC Analysis

In this test, the simulation command is set to small signal *AC Analysis*, where the input current source is swept from 1Hz to 10 MHz. The obtained Bode plots after and before the filter are represented in Figure 5. The AC characteristics of the output signals are summarized in Table 3.

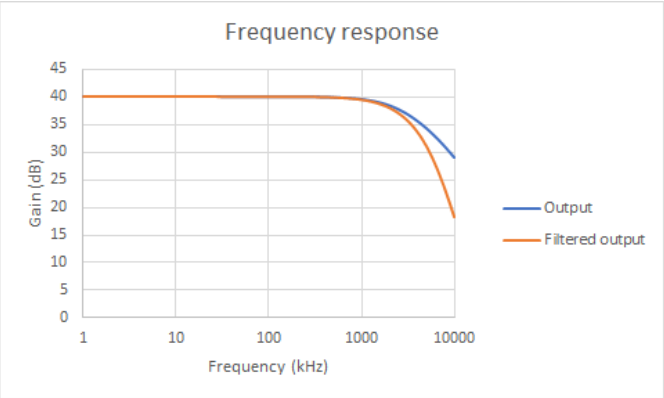

Figure 5: Simulated frequency response.

Table 3: Measurements in frequency response simulation.

Parameter	Result
Cut-off frequency (-3 dB)	2.51 MHz
Flatness (-0.1 dB)	417 kHz
Resonance	None
Filter action	-20 dB/dec

The test is repeated with different cable lengths, but the performance is almost equal in every case, so cable length is not a sensitive variable in this application.

4.3 Noise Analysis

The following noise sources are considered for the calculation. They are drawn in Figure 6 and explained with deeper details in [12]:

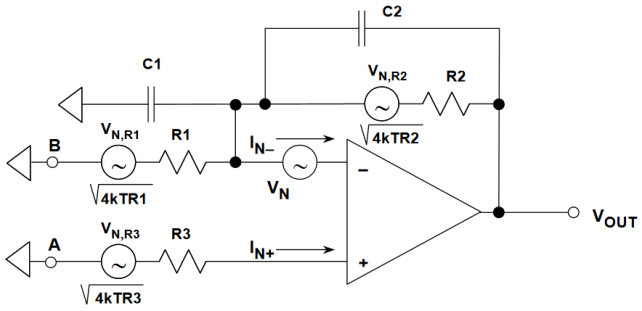

Figure 6: Noise sources. Figure from [12]

- Amplifier Input Voltage Noise $I_N R_2$

- Amplifier Input Current V_N

- Resistor Thermal Johnson noise $\sqrt{4KTR_i}$

where
I_N and V_N can be obtained from the amplifiers datasheets.
T is the Ambient Temperature
K is the Boltzmann constant

The results of Table 4 represent the noise sources of the first 2 amplifiers (U_1 and U_2), and the noise referenced to the output of the amplifier U_2, just before the filter stage.

Table 4: Noise results.

Noise source	Noise result (nV)	Output ref. noise (nV)
Johnson noise of R_{F1}	0.91	1.82
Voltage noise of U_1	4.50	9.00
Current noise of U_1	0.08	0.15
Johnson noise of R_V	4.06	8.12
Johnson noise of R_{F2}	5.74	5.74
Voltage noise of U_2	7.00	7.00
Current noise of U_2	12.00	12.00

The root-sum-square of all the output contributions represents the total RMS output density noise:

$$Noise_{RMS} = \sqrt{\sum N_i} = 19.40 nV/\sqrt{Hz} \tag{2}$$

To doublecheck results with LTSpice, the simulation command is set to *Noise* mode, swapping from 1 Hz to 10 MHz. The result in Figure 7 is a constant value in the frequency range of interest and matches with the previous numerical calculations.

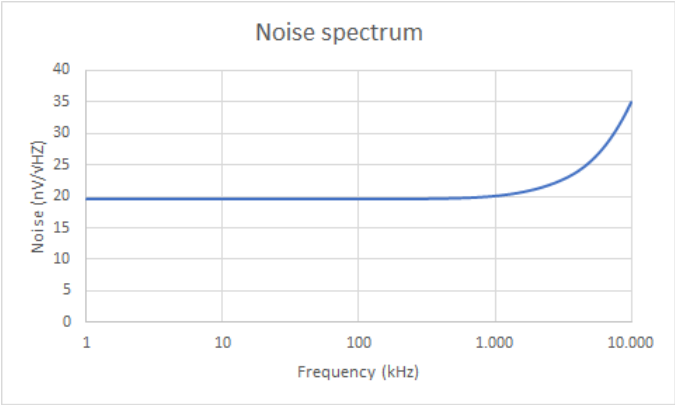

Figure 7: Noise simulation result.

The noise floor represents the average level of noise and is obtained by integrating the obtained density noise over the bandwidth of interest, in this case the bandwidth not attenuated by the downstream low pass filter (2.51 MHz). The noise floor can be referenced to the input current by dividing this value by the cascade gain. Any input current under this result cannot be measured.

Table 5 shows the result of noise floor and other interesting parameters related to noise, like the signal to noise ratio (SNR) and the effective number of bits (ENOB).

Table 5: Noise results.

Parameter	Result
Noise floor	27.43 μV RMS
Min. input current	274 nA RMS
SNR	104.14
ENOB	17.01

It is verified that the minimum readable current due to the expected noise, 274 nA, is better than the required precision, 10 μA, and the less significant bit (LSB), 1.52 μA.

5 Error estimation and calibration

After a previous evaluation, following systematic-type error sources have been identified in each amplifier stage of the FC Front-End: unbalanced voltage (offset), resistor tolerances and error gain [13].

Offset voltage figures can be found in the datasheets of the amplifiers. They are typically 0.4 mV in AD8066 and 1 mV in AD8397.

Resistor tolerance error is expected to be low due to the selection of surface mounted (SMT) resistors with tolerance of 0.1%. The relative error introduced in stages 1 and 2 is:

$$\epsilon_R = \frac{-2\alpha}{1-\alpha}\frac{G-1}{G} \tag{3}$$

$$\epsilon_{R1} = 0.22\% \tag{4}$$

$$\epsilon_{R2} = 0.44\% \tag{5}$$

,where:
G is the gain of the stage
α is the resistor tolerance

Error gain of the amplifiers depends on their finite open-loop gain, but the result is negligible:

$$\epsilon_G = \frac{G}{G+A} \tag{6}$$

$$\epsilon_{G1} = 0.079\% \tag{7}$$

$$\epsilon_{G2} = 0.011\% \tag{8}$$

,where:
G is the gain of the stage
A is the open-loop gain of the amplifier

All of these systematic expected errors can be fixed with an appropriate calibration method. By introducing a well-known set of input currents to the Front-End (x_i), a linear fitting should be done in order to find the calibration factors p' and q' and obtain y'_i instead of y_i. The process is

sketched in Figure 8, and it is automatically carried out by the Control System, where the calibration factors are Process Variables which can be modified when a new calibration is done.

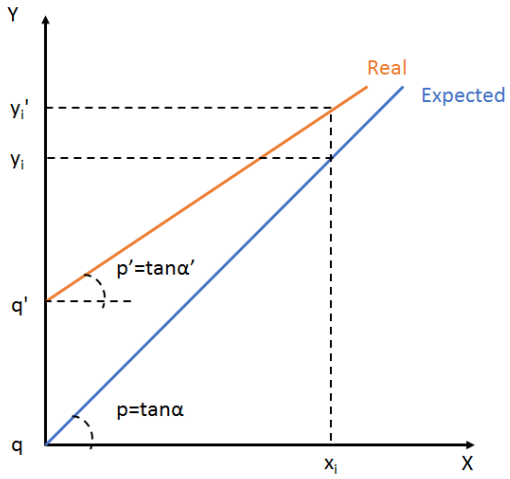

Figure 8: Linear calibration method.

6 Conclusions and future works

- All the stages of the design process of the FC Front-End electronics has been described in detail, demonstrating the accomplishment of all the requirements.
- The use of every key component like cables, input protections and amplifiers has been justified, as well as the values selected for components like resistors and capacitors.
- The performance of the electronic circuit in DC and AC modes has been simulated for all ranges of input signals, verifying that the results match with the expected values in every case.
- An appropriate grounding scheme has been provided in order to minimize external noises.
- Possible internal noise effects have been evaluated numerically and doublechecked with simulations.
- Uncertainty has been estimated and a calibration method has been proposed to fix possible systematic errors.
- Once the detailed design is finished, the next step is to lay out and manufacture the final PCB and the Back-End (Power Supplies System).

References

[1] Agreed Requirements Document *L4_Requirements_MEBT_PBI_2016-11-09.*

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[3] Electrical model and dynamic behavior of a FC depending on the acquisition circuit. *Carlos de la Cruz, (ESS-Bilbao) 2015.*

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[5] Diagnostics for High Intensity Hadron Beams. *Patrick Ausset (Spiral 2), 2013.*

[6] Op Amp Output Phase-Reversal and Input Over-Voltage Protection *Analog Devices Tutorial MT-036, 2008.*

[7] BI review on Radiation development and testing. *Gerrit J. Focker (CERN), 2013.*

[8] AD8397 Datasheet. `http://www.analog.com/media/en/technical-documentation/data-sheets/AD8397.pdf`

[9] AD8066 Datasheet. `http://www.analog.com/media/en/technical-documentation/data-sheets/AD8065_8066.pdf`

[10] Transimpedance Amplifiers (TIA): Choosing the Best Amplifier for the Job. *Texas Instruments Application Report SNOA942, 2015*

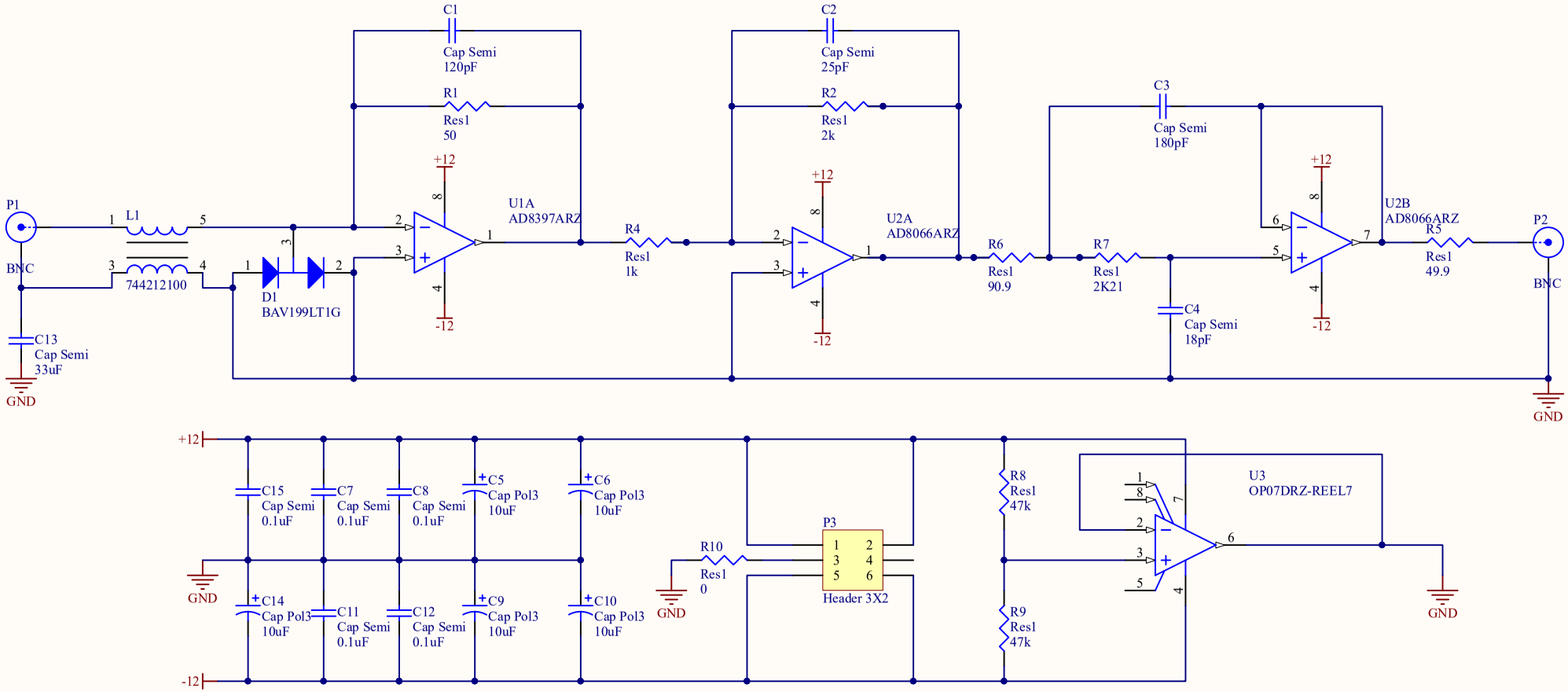
[11] Amplifier High Impedance Sensors - Photodiode Example *Microchip Application Note AN951, 2004*

[12] Op Amp Total Output Noise Calculations for Second-Order System *Analog Devices Tutorial MT-050, 2008.*

[13] Adquisición y distribución de señales. *Ramón Pallàs, Editorial Marcombo, 1993*

Appendices

A Front-End Circuit Schematic



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B Simulation netlist

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5 15 4 0
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