MEBT-BI-FC08-02

FC Front-End Prototype Tests

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Project: MEBT FARADAY CUP

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Change History

Rev.	Date	Author(s)	Description
0.1	April 14, 2017	C. de la Cruz	First results.
0.2	April 26, 2017	C. de la Cruz	Minor changes.

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1 Introduction

The objective of the Faraday Cup (FC) Front-End is to convert the collected current at the cup into a voltage signal, as well as to amplify and condition this signal to drive it tens of meters away to the digitizer. At this stage of the design procces, a first protoype of the FC Front-End has been fabricated and tested, and the performance is described in this document.

2 Description of device and equipment

The schematic of the circuit designed is shown in Figure 1. A comprehensive description of the design proccess can be consulted in the Design Document MEBT-BI-FC09.

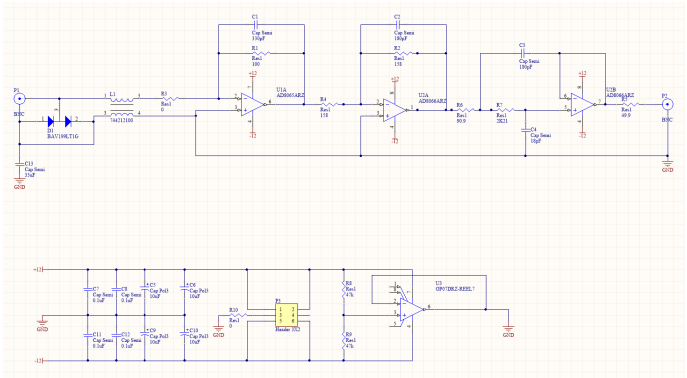

Figure 1: Schematic of FC Front-End Prototype.

The layout has been implemented in a double side board of FR-4 material. The size is 73 x 36 mm, with BNC connectos at the input and output. To minimize noise sources, components selected are SMT and tracks are 0,254 mm thickness. An image of the final Front-End prototype can be observed in Figure 2.

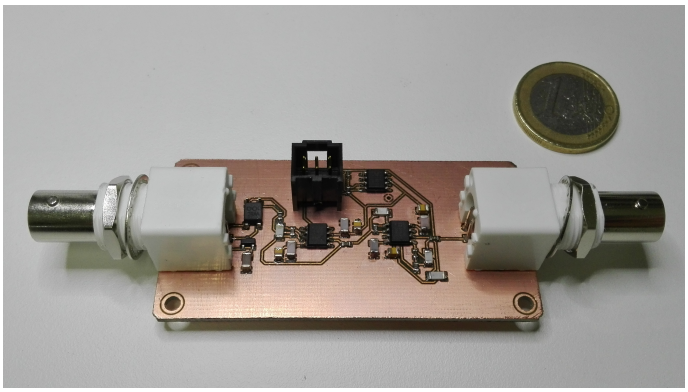

Figure 2: Image of FC Front-End Prototype.

A detailed list of all the equipment used for the tests is shown in Table 1.

Table 1: Used equipments.

Device	Model and Manufacturer
Oscilloscope	Tektronix DPO 7354
Pulse generator	Hameg HMF2525
Bipolar source	TTI CPX400DP
A/D Converter	D-tAcq ACQ420FMC
VME Board	IOxOS IFC1210
Multimeter	Amprobe 35XP-A

3 Tests

3.1 Step Response

The incoming signal that emulates the charge collected by the cup is a 100 Ω resistor placed in series after a voltage pulse generator, to obtain an input current from the point of view of the Front-End. In this test, the objective is to characterize the output of the Front-End with a step input signal. This signal replicates the nominal beam current, and its characteristics are detailed in Table 2.

Table 2: Input parameters in step response test.

Parameter	Value
Input current	62.5 mA
Rise time	1 ps
Fall time	1 ps
Width	50 µs

The output measured at the oscilloscope is compared with the simulation values. The method and code used to obtain the simulations are detailed in the Design Document MEBT-BI-FC09. The result is shown in Table 3 and represented in Figure 3.

Table 3: Measurements in step response test.

Parameter	Test	Simulation
Output voltage	6.25 V	6.25 V
Rise time	150.3 ns	97 ns
Fall time	148.4 ns	97 ns
Overshoot	None	None
Offset	1 mVpp	4.12 mVpp

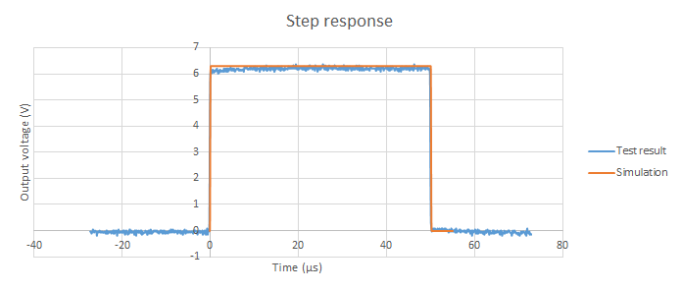

Figure 3: Step response.

3.2 Linear Response

A sine waveform with 100 Hz and different amplitudes has been applied to the input of the Front-End. The output has been measured in each case and represented in Figure 4. The result is properly fitted to a straight line, with an offset of 1.1 mV. This linearity means a good current estimation from any voltage value readout with a calibration gain close to 1. The offset value matches with the obtained in the step response test and with the figures of the amplifier manufacturer's datasheet.

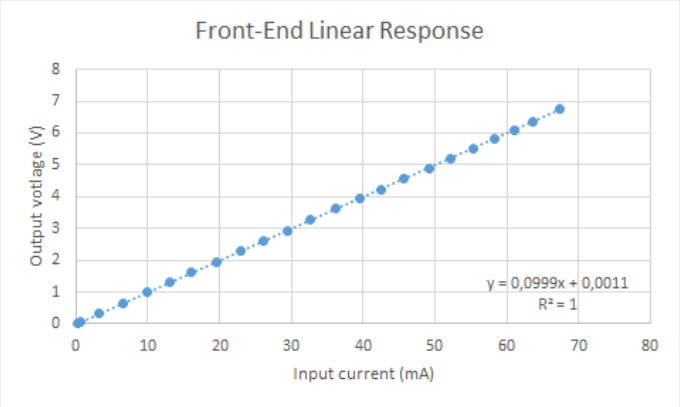

Figure 4: Linear response.

3.3 Frequency Response

A square waveform of 3 V amplitude has been used as input for this test. The frequency has been swept from DC to 10 MHz to observe the amplitude attenuation with the increase of frequency. The results of the test and the simulation values are in the bode diagram of the Figure 5. It turns out that the cut-off frequency (-3 dB) obtained is 2.35 MHz with no resonances.

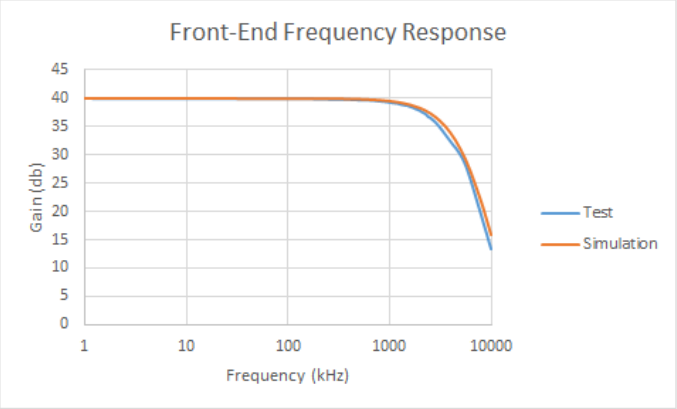

Figure 5: Frequency response.

3.4 Frequency Response with input cable

The coaxial cable selected for the final installation, TE Connectivity CLFH-178CK0135, is a RG178 type with 3 m length. It has been connected to the input of the Front-End and the frequency response test is repeated. The results are shown in Figure 6. The cable introduces a pole to the system that makes the frequency performance a bit better than without cable in the conditions tested.

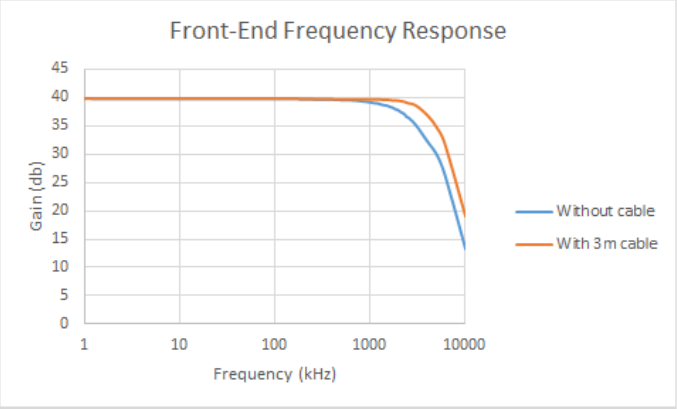

Figure 6: Frequency response with cable.

3.5 Integration to the VME Control System

The step response test is repeated in the same conditions, but in this case the data acquisition is done by the D-tAcq converter instead of the oscilloscope. The acquisition is commanded by the IOC *fc_mebt*, that is running in the IOxOS board placed at the VME crate. This scenario is almost the same than the final layout of the application (see Figure 7). The results are displayed in the OPI program made in CS-Studio, as it can be seen in Figure 8.

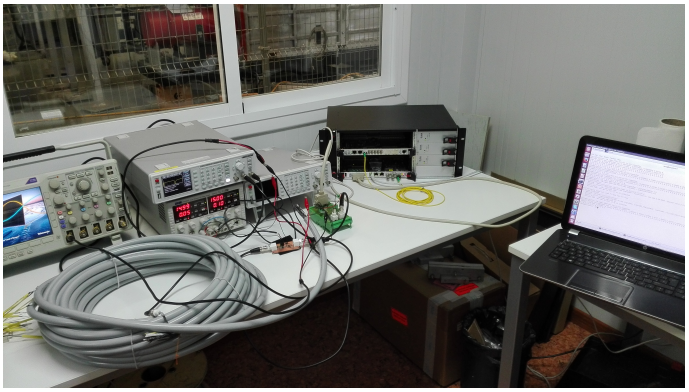

Figure 7: VME Integration test.

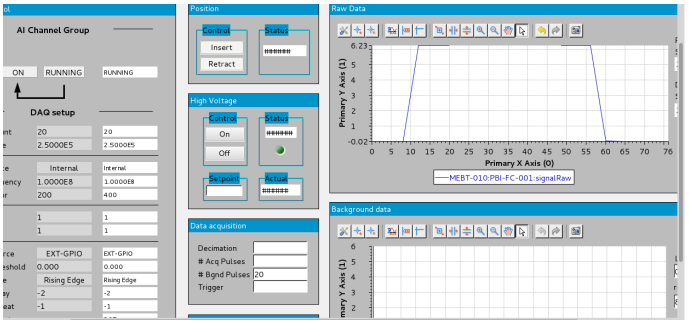

Figure 8: CS-Studio OPI Screenshot.

The sampling is configured at 250 kHz with the external trigger connected to the output trigger of the signal generator. The output measurement, recorded in the array PV *MEBT-010:PBI-FC-001:signalRaw*, is compared with the osciloscope profile in the Figure 9. The amplitude is exactly the same (6.25 V) with neglectable offset.

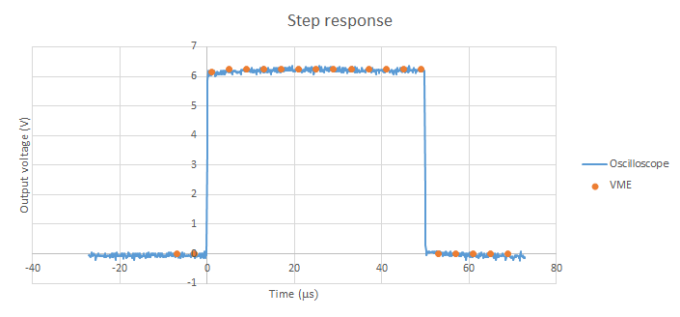

Figure 9: VME acquisition test results.

3.6 Integration to the VME Control System with output cable

In the final layout of the application, the electronic circuit of the Front-End wil be placed inside the LINAC Tunnel, close to the vessel where the Faraday Cup is installed. However, the Control System will be located in the Racks Gallery, around 25 meters away. In order to make a complete integrated test, a cable with similar characteristics of the planned one (screened, 0.5 mm^2 section and 25 m length) has been plugged in. In the same conditions than the previous test, the step response is compared with and without cable and displayed in Figure 10. It can be observed than the voltage drop due to the cable is close to zero, therefore there is no loss of accuracy expected in the final system.

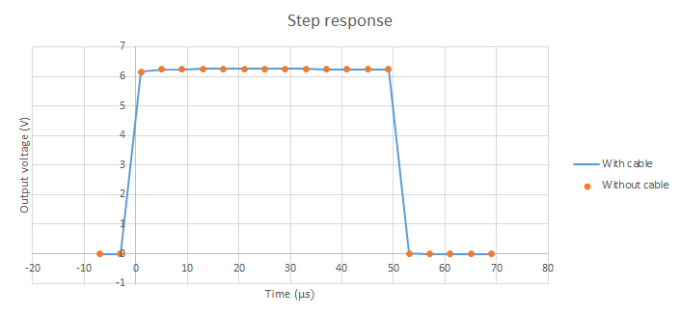

Figure 10: Step response with output cable.

4 Conclusions and future works

- A first prototype of the FC Front-End has been tested at different conditions: step, linear and frequency response. In each case, the obtained results turn out that the performance is very similar than the design values and simulation results.
- Some vertical tests have been succesfully carried out. Input and output cables don't add losses or bandwith alterations. It has been verified that the data acquisition made by the Control System is the same than the recorded by the oscilloscope.
- The next stage of the design process is the fabrication of the final PCB, including some minor improvements detected and final components and connectors.