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MEBT Faraday Cup Software Development Document

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Project: MEBT

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Approved by: I. Bustinduy

Change History

Rev.	Date	Author(s)	Description
1	18-11-2016	A. Milla	First version.
2	01-12-2016	A. Milla	Statistics in IOC, proposals added and other minor changes.

MEBT Faraday Cup Software Development Document

A. Milla

1 Introduction

The Faraday Cup (FC) will be used to measure the beam current and as beam stopper for accelerator start up. The FC is designed in order to withstand the commissioning beam modes.

1.1 Purpose

The purpose of this document is to describe the development of the software for the MEBT Faraday Cup. The object is to present the ideas behind the software final design. In this way the future maintainers will have a better understanding of the product making easier the possible future updates.

This document is a continuation of the Faraday Cup's Preliminary Design Review (PDR) [1] based design document, MEBT Faraday Cup Software Design Document[2].

The intended audience is the Beam Diagnostics group and the ICS division at the European Spallation Source, ERIC (ESS) and the Control & Diagnostics group at ESS Bilbao (ESSB).

2 Hardware

2.1 General interface layout

In this section we explain the control interface layout for the Faraday Cup, starting from the the top level, the network, to the device itself.

The FC will use the optics and beam instrumentation subnet. It will also need an indirect connection (not through the control box) with the cooling and interlock PLCs.

In the figure 1 we show the main components involved in the control system of the Faraday

Cup:

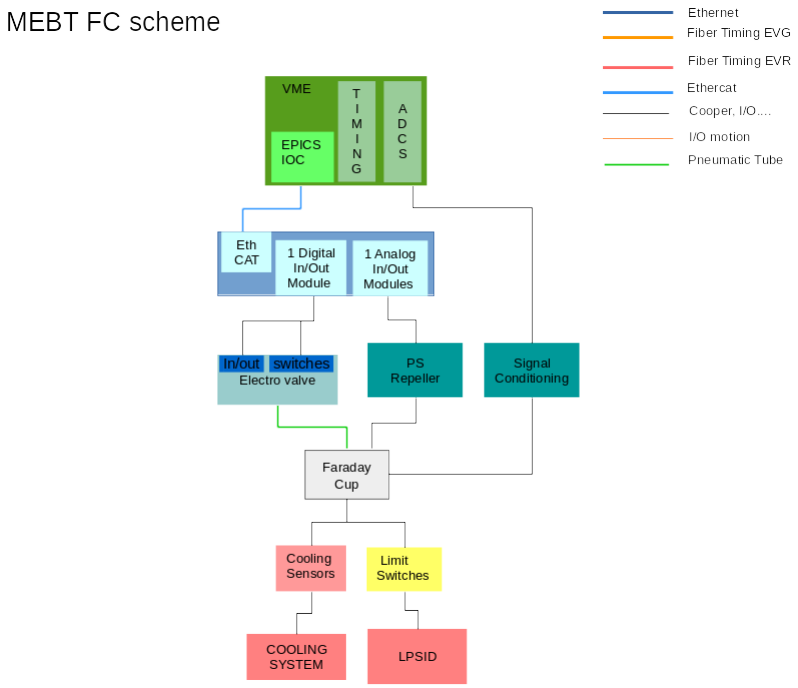

Figure 1: MEBT FC scheme

2.2 Hardware description

ESS Bilbao has done the development of the Faraday Cup using the next hardware:

- VME Crate: ELMA type 39 horizontal, 4U, 84HP.
  - CPU: IOxOS IFC 1210
  - Digitizer board: D-Tacq ACQ420FMC-4-2000-16:
    * 4 analog channels
    * 2 MSPS
    * 16 bits
  - Event Receiver Board PMC-EVR-230
  - Event Generator Board VME-EVG-230
- Beckhoff I/O
  - Bus ethercat: EK1100
  - Input/Output modules
    * Digital: EL1018 and EL2808

    * Analog: EL3002 and EL4032

The final hardware design will have a μTCA platform. The migration from VME to μTCA will be done under the responsibility of ESS. ESS Bilbao will do the software testing using a VME hardware testbench. Then ESS Bilbao can not guarantee the delivered software's performance in a μTCA platform.

3 Software

3.1 IOC overview

The IOC will have at least the next basic functionalities:

- Send insert/retract instruction to the Beckhoff I/O.
- Control the repeller PS.
- Get the data from the FC.

In the figure 2 we see a flow diagram. In the flow diagram we observe that if the operator decides to insert the FC from the idle position, how the IOC will check the Beam Mode status. And depending on this status will continue to block the operator in the idle position or will allow the setting of the repeller. The use of the repeller will be optional. Once the FC is inserted the IOC will start reading until the operation is finished and the FC is retracted.

3.2 IOC development

3.2.1 FC Insert/Retraction

The implementation of this functionality will be based in the etherCAT module for the Beckhoff I/O provided by ESS.

3.2.2 Repeller

The implementation of this functionality will be based in the etherCAT module for the Beckhoff I/O provided by ESS.

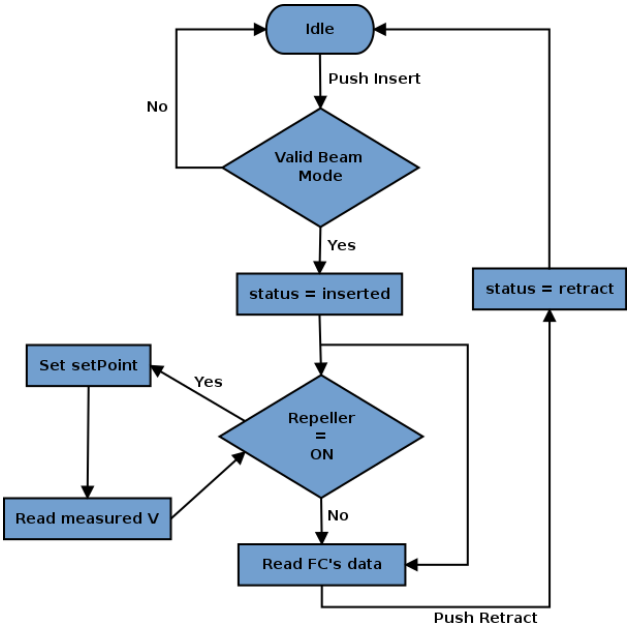

Figure 2: IOC Basic flow diagram.

3.2.3 Signal acquisition

The Faraday Cup has to receive the raw signal from the digitizer and show it in the GUI, For this purpose we use the ifcdaq module. Once we have received the signal we stored it in a buffer with the size specified as the signals needed for the background subtraction (fig. 3).

3.2.4 Background subtraction

We have implemented and additional function in the Faraday Cup Control in order to perform a background subtraction of the raw signal. For this purpose samples are acquired before and after the signal chosen for the analysis.

The implementation is done with 2 subroutines. One for the signal buffering and the other one for the application of the background subtraction.

Signal Buffering In order to save the different pulses needed for the background subtraction. We have developed a function that reads as arguments the raw signal and the number of pulses needed for the background subtraction. Knowing the number of pulses for the background subtraction we allocate the needed memory, and we save the raw signal. For the posterior signals we just save the signal in the allocated memory. Once this is full the

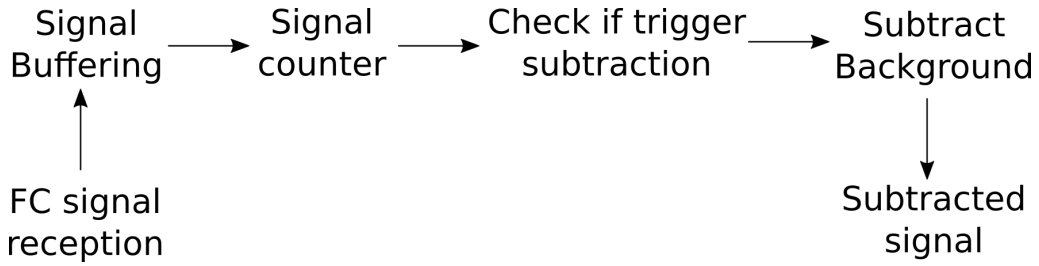

Figure 3: IOC Workflow.

middle position will be the signal that we will use for the background subtraction (see fig. 4).

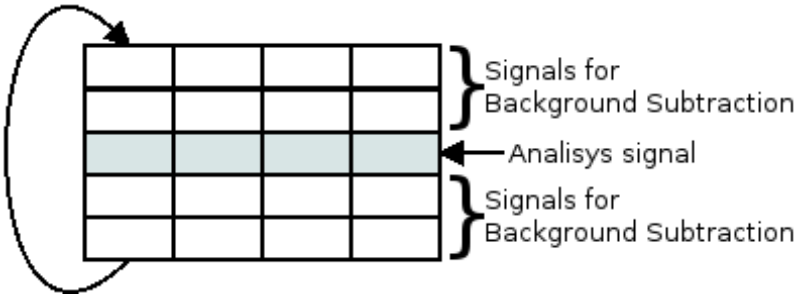

Figure 4: Background subtraction buffer.

Background subtraction We perform a basic background subtraction in this case we take the previous and posterior signals to signal for the analysis and we calculate the average. We subtract the average to the analysis signal. And if this is above the threshold we choose the average value for that position. If the value is below the threshold we use the analysis signal value.

Statistics Over the the obtained subtracted data we perform some basic statistics. The implemented statistics are:

- Peak current value.
- Minimum current value.
- Standard deviation.
- Average current value.

These statistics are implemented in an EPICS subroutine.

3.3 GUI development

In order to manage the software, we have designed the a GUI (see fig. 5) using CS Studio.

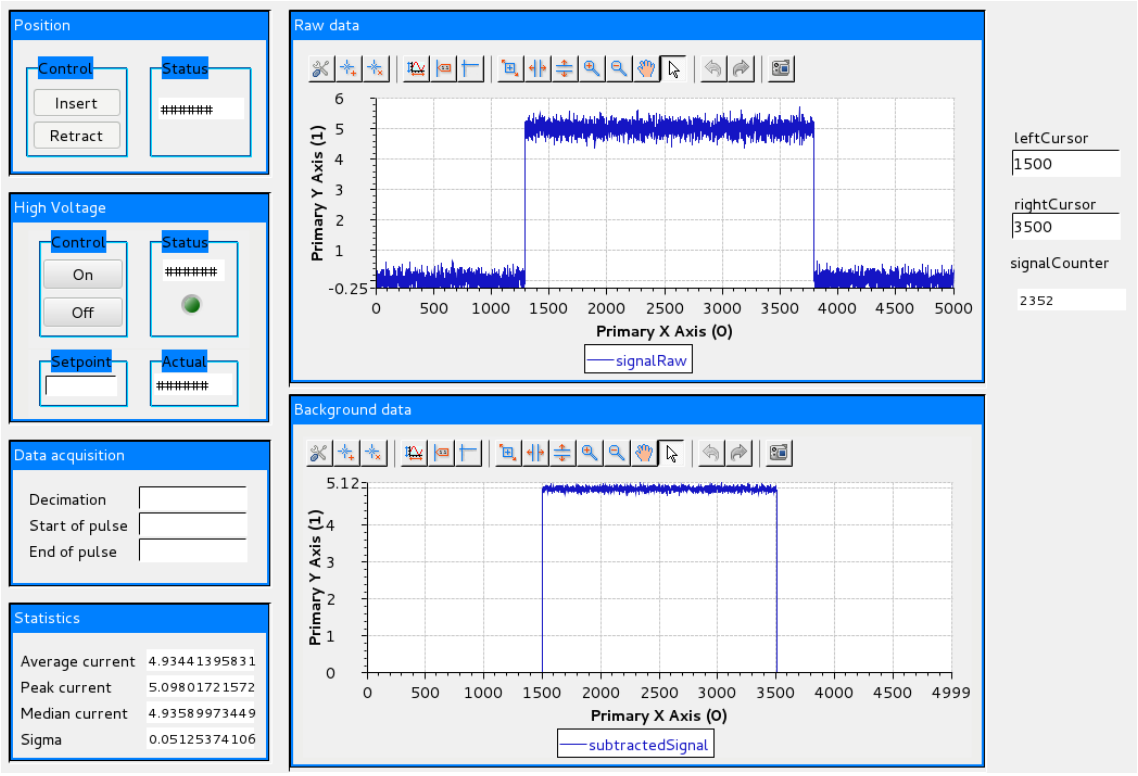

Figure 5: FC proposed GUI based on ESS guidelines.

In figure 5, we obseve how the different functionalities of the Faraday Cup control are implemented in the GUI: position control, repeller voltage, data plotting, show statistics, etc. These modules can be blocked depending on the the beam mode status.

3.4 List of PVs

The list of PVs for the control of the different IOC funcionalities is described. It is important to point out that the nomenclature of the PVs is provisional, and it will be changed according to ESS guideliness for IOC integration.

Name	I/O	Type	Comment
nPulsesAnalysis	Input	Scalar	Pulses interval for the analysis signal
prevTrigger	Output	Scalar	The last pulse number of the analysis signal.
backgroundSubtract	Output	Waveform	Returns the subtracted signal result.
signalBuffer	Input	Waveform	Buffers all the raw signals.
signalCounter	Output	Scalar	Counts the raw signals.
triggerSubtraction	Output	Scalar	Triggers the signal subtraction.
newSignalEvent	Output	Event	Notifies a new raw signal.
ifSubtraction	Output	Scalar	It's an internal fanout.
splitter	Output	Scalar	It's an internal fanout.
cursorLeft	Input	Scalar	The left cursor for the analysed signal.
cursorRight	Input	Scalar	The right cursor for the analysed signal.
nPulsesForSubtraction	Input	Scalar	Number of pulses stored for the background subtraction.
signalRaw	Input	Waveform	The received raw signal from the FC.
subtractedSignal	Output	Waveform	The resulted subtracted signal.

3.5 Requirements

Based in the Faraday Cup functionalities document [3] and in the MEBT Faraday Cup Software Design Document[2], the next requirements have to be taken in account:

Req #	Description	Done
Req 1	The operator shall be able to control remotely the insertion/retraction of the FC.	
Req 2	The operator shall be able to set the value of the bias voltage provided by the power supply.	
Req 3	The status of the beam permit (Beam mode) shall be flagged on the engineering screen.	
Req 4	The engineering screen shall be locked if the beam permit is not in the right status.	
Req 5	The operator shall define the time of acquisition by choosing the number of samples.	
Req 6	The operator shall be able to choose the interval needed for the background subtraction, before and after the beam pulse.	
Req 7	The operator shall be able to decimate the number of samples in order to simulate a lower sampling rate.	
Req 8	The operator shall be also able to delay or advance the trigger of the acquisition with respect to the timing system trigger.	
Req 9	All the acquired signal raw data has to be converted to mA.	
Req 10	A time interval will be implemented in order to estimate the beam intensity on the flat top after the transient..	
Req 11	From the user selected flat top basic data statistic might be implemented, like: • Peak current value. • Minimum current value. • Standard deviation of the beam current fluctuation over the pulse. • Average current value.	
Req 12	Raw data from FC shall be displayed at a refresh rate of 14Hz.	
Req 13	A second plot panel shall display the analysed data at a lower refresh rate that will be defined by the operator (1 second at least).	
Req 14	The basic statistic shall be refreshed at the same rate than the analysed data.	

3.5.1 Proposals for improvements

These are proposals that ESSB have collected from ESS stakeholders:

Prop. #	Description	Done
Prop. 1	A gain factor has to be implemented for the calibration.	
Prop. 2	Add continuous mode based set point to trigger the acquisition.	
Prop. 3	The operator should can specify the length of pulse in the GUI.	

4 References

[1] D. de Cos, A. Milla, C. de la Cruz, J. Ortega, I. Rueda, R. Miracoli, and I. Bustinduy, "Preliminary design of the ESS MEBT Faraday Cup," *PDR BILBAO MEBT DIAGNOSTICS*, 2016-07. [Online]. Available: `https://indico.esss.lu.se/event/592/contribution/3/material/slides/`.

[2] A. Milla, "MEBT Faraday Cup Software Design Document," ESS Bilbao, Design Document, 2016. [Online]. Available: `https://chess.esss.lu.se/enovia/common/emxNavigator.jsp?objectId=21308.51166.26624.20665`.

[3] B. Cheymol and H. Kocevar, *Faraday cup functionalities*, version 1, European Spallation Source, ERIC, 2016.