ZHAW – Institute of Applied Mathematics and Physics (IAMP)

Fast Beam Interlock System (FBIS)

Architectural Proposal

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Martin Rejzek	21.07.2017	Extended chapter about Mezzanine Cards, Latency and Functional behavior.
Martin Rejzek	01.08.2017	Re-structured document. Extended chapter about fundamental architecture concept.
Martin Rejzek	04.08.2017	Walk-through (krav, rehm, rejz)

Table Of Contents

1 Introduction

1.1 Scope

This document contains a proposal for architectural building blocks and their interfaces. To some extend also realization ideas are included. The proposal is based on the evaluation of /Design Options/. The document does not contain the final, concrete FBIS architecture.

The concrete FBIS architecture depends on the Protection Functions the FBIS is part of and the respective requirements of these functions. The Protection Functions have not evolved far enough to specify finalized architectural requirements on the FBIS.

The document is intended for readers familiar with the FBIS concept of operations /FBIS ConOps/.

1.2 Purpose

This document presents and discusses a set of architectural building blocks foreseen for the FBIS and:

- presents the concept behind these building blocks
- presents the interfaces of the building blocks
- presents the functional behavior of the building blocks

Furthermore this document illustrates how the building blocks can be put together to form a concrete architecture. This illustration aims at representing the final FBIS architecture as close as possible given today's knowledge and taking into account the currently expected requirements from Protection Functions. Where appropriate this document also explores architecture alternatives.

Partially this document also contains realization ideas for the architectural building blocks and their interfaces. Strictly seen these realization ideas pre-empt the design. However, we believe they help to get a better understanding of the architectural building blocks and interfaces and hence included them in this document.

For reasons of documentation concepts and realization ideas are phrased in the simple present tense. E.g. "The mechanical dimension is 19" compatible" instead of "the proposal foresees to realize the mechanical dimension is 19" compatible".

1.3 Acronyms and Definitions

Table 1 lists all special acronyms and definitions used in this document.

Table 1: Acronyms and Definitions.

Acronym	Definition
BIF	Beam Interlock Function
COTS	Commercially off the shelf
DLN	Decision Logic Node
EBIF	Emergency Beam Interlock Function
FBIS	Fast Beam Interlock System
GBP	Global Beam Permit
LBP	Local Beam Permit
LPS	Local Protection System
MC	Mezzanine Card
MCH	MTCA shelf Crate Handler
MP	Machine Protection
OPL	Optical Protection Line
OPLR	OPL Mezzanine Card in the “OPL repeater configuration”
OPLT	OPL Mezzanine Card in the “OPL termination configuration”
RBIF	Regular Beam Interlock Function
SCU	Signal Conversion Unit
SLink	High-Speed serial Link. The “S” stands for “serial”

2 References

Table 2 lists all documents referenced.

Table 2: Referenced Documents

Ref.	Document-No.	Version	Title
/FBIS ConOps/	CB:280675	3	FBIS Concept of Operations
/Design Options/	CB:283431	1A	FBIS Architectural Design Options
/FBIS SRS/	CB:280773	1B	FBIS System Requirements Specification

3 FBIS Architectural Design Proposal

3.1 Introduction

This chapter describes the FBIS architecture proposal which is derived from the design options given in /Design Options/. The proposal takes into account the current state of the Protection Function requirements, FBIS Concept of Operations (/FBIS ConOps/), and FBIS System Requirements Specification (/FBIS SRS/).

The following sub-chapters describe:

- The basic structure of the architecture from a physical viewpoint (chapter 3.2)
- The concepts, interfaces and functional behaviour of the individual architectural building blocks (chapters 3.3 and 3.4)
- Special considerations for the control of Actuation Systems (chapter 3.5)
- Special considerations for MP-related Systems directly interfacing with the Actuation Systems (chapter 3.6)

3.2 The Basic Structure

The FBIS architecture is based on two main architectural building blocks:

- The “Decision Logic Node” (DLN) and the
- “Signal Conversion Unit” (SCU)

Put very brief, their functions can be described as following:

- The DLNs perform the protection logic implemented by the FBIS. They also realize the interfaces to the Higher-Level Safety, Control System and the ESS Timing System.
- The SCUs handle the interfaces of Sensor and Actuation Systems and read, respectively drive their signals.
- and to the Actuation Systems. The main function of the SCUs is aggregation and serialization of input signals respectively control of the Actuation Systems.

DLN and SCU interface with each other via a so called SLink. Each SLink is a point-to-point connection, however both, the DLNs and SCUs feature multiple SLink interfaces, hence a n-to-m structure can be achieved as illustrated in Figure 1.

A network called “FBIS Network” is used for communication among the DLNs. Finally an Optical Protection Line (OPL) allows the DLNs and to directly request a beam switch-off.

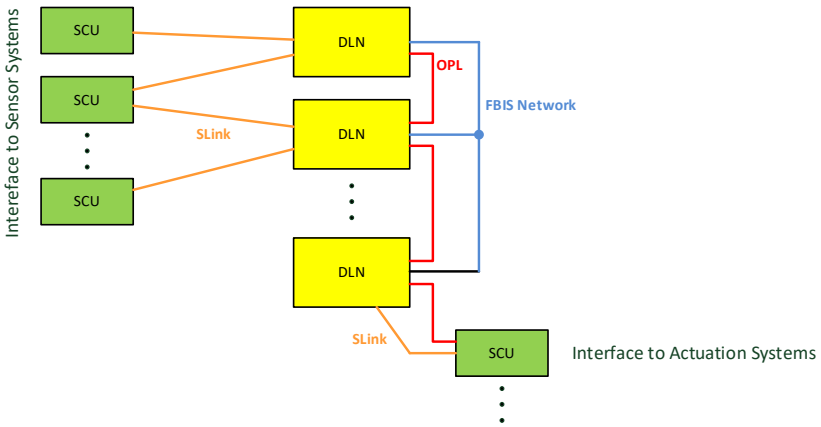


Figure 1: The FBIS consists of Signal Conversion Units (SCUs) and Decision Logic Nodes (DLNs). Communication between SCUs and DLNs is realized by Slink’s, communication among DLNs by an Optical Protection Line (OPL) and the FBIS Network. The SCUs shown on the right side interface with the Sensor Systems, the one on the left side with the Actuation Systems. Not explicitly shown is the DLNs interface to Higher-Level Safety and Control Safety and the ESS Timing System.

3.3 Signal Conversion Unit (used to Interface with Sensor Systems)

3.3.1 Concept

SCUs are used to interface with Sensor Systems. Since one single SCU can interface with multiple Sensor Systems the SCU serves as a kind of “local concentrator”. The SCUs and their connection to Sensor Systems is based on the physical layout of the facility and not by the “type” of Sensor System. Hence a single SCU may for example interface with RF-Sensor-Systems and Beam-Instrumentation-Sensor-Systems.[1]

An SCU is equipped with Mezzanine Cards which realize the actual interface to the Sensor System. Different types of Mezzanine Cards can be used on the same SCU allowing to satisfy the requirements of the different types of Sensor Systems. If the interface of a Sensor System changes only the respective Mezzanine Card has to be replaced. This design provides flexibility and allows to add interfaces not considered today.

3.3.2 Interfaces

As already mentioned the physical interfaces to Sensor Systems is realized with the help of Mezzanine Cards. The interface to DLNs is realized by a serial high-speed interface called SLink. Figure 2 shows a sketch of a SCU and its interfaces.

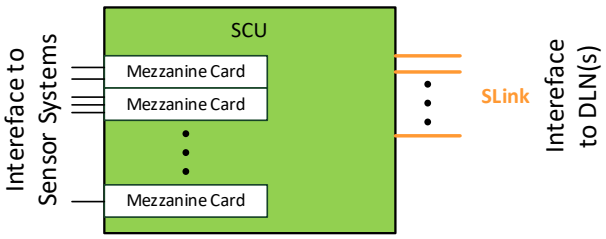


Figure 2: The physical interface of the SCU to Sensor Systems is realized on Mezzanine Cards. A single SCU provides multiple slots for Mezzanine Cards. The SCU also provides multiple SLink interfaces to DLN(s).

3.3.3 Functional Behaviour

The SCU realizes the following functionalities:

- Sample discrete input signals: The SCU continuously samples the discrete input signals such as Beam Permit or Ready signals and determines the state of the inputs (OK, NOK, Error, …).
- Sample data link inputs and decode the data: The SCU continuously reads the data link inputs and decodes the data.
- Detect failures with respect to the discrete and data link inputs: The SCU detects erroneous discrete input signals (e.g. short circuits) and makes this information available for further processing. The SCU evaluates the incoming data streams and detects communication failures.
- Serialize the input data and send it via the SLink(s): The SCU serializes the discrete and data link inputs and together with additional information send this information via the SLink interfaces to the connected DLN(s).

Additionally:

- Perform self-diagnostic tests: The SCU performs self-diagnostic tests as appropriate. For example to detect power failures or over temperature.
- Verify the SCU hardware configuration: The SCU detects its own hardware configuration. For example what type of Mezzanine Cards are installed. The SCU verifies whether the detected hardware configuration meets the expectation.

[1] In contrast to having one SCU interfacing with all Beam-Instrumentation-Sensor-Systems and a next SCU interfacing only with RF-Sensor-Systems.

- Provide read/write access to status and control registers: The SCU provides read/write access to status and control registers via the SLink interface, for example to read the identification number and firmware version of the SCU carrier or the SCU hardware configuration.

The SCU does not:

- Perform any FBIS decision logic calculations
- Provide features like masking
- Depend on the Proton Beam Destination and Proton Beam Mode
- Provide direct interfaces to Higher-Level Safety and Control Systems (EPICS) and the ESS Timing System

These functions are provided by the DLNs.

3.3.4 Architectural Application Options

As shown in Figure 1 SCUs are used to locally concentrate signals from Sensor Systems and make them available to the DLNs. Additionally SCUs are used to interface with Actuation Systems. This aspect is covered later in chapter 3.5.

Although not favourable because of increased latency, a tree structure of SCUs could be realized as shown in Figure 3 and Figure 4. While the signals read by SCU 1 in Figure 3 are communicated to SCU 2 by means of the SLink the tree structure in Figure 4 makes use of dedicated hard-wired signals.

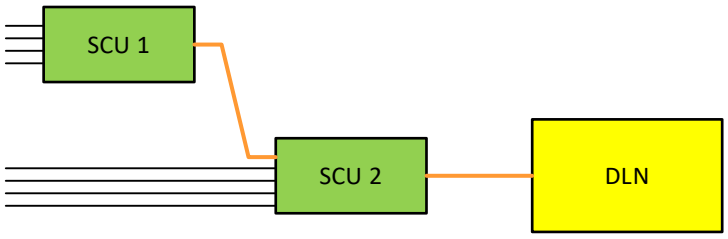


Figure 3: SCUs can be used to realize a tree structure. The SLink is used to communicate the state of the sensor signals read by SCU 1 to SCU 2.

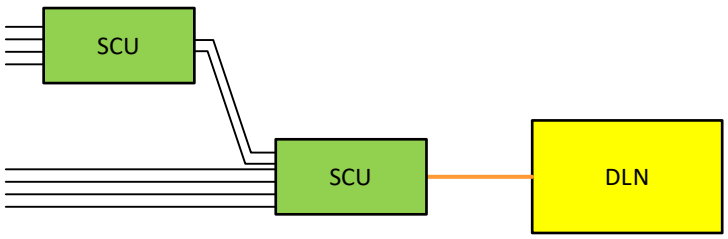


Figure 4: Alternative the structure shown in Figure 3. The states read by SCU 1 are communicated to SCU 2 by means of discrete, hard-wired signals.

3.4 Decision Logic Node

3.4.1 Concept

The sum of all Decision Logic Nodes process the FBIS decision logic. Each node processes that part of the logic which is related to the Sensor System signals locally connected. Every DLN computes a Local Beam Permit (LBP). If a DLN requests a beam switch-off it sets the LBP to state “NOK”.

All DLNs as well as the SCUs interfacing with the Actuation Systems are connected to the Optical Protection Line (OPL) which represents the Global Beam Permit (GBP). Any of the systems connected to the OPL may interrupt the line and through this force the Global Beam Permit to state “NOK”.

An example is given in Figure 5. It is assumed that a beam switch-off is required if any of the BEAM-PERMIT signals switches to NOK:

- The signals BEAM-PERMIT-A and BEAM-PERMIT-B read by SCU 1 are communicated via SLink 1 to DLN 1;
- Likewise the signals BEAM-PERMIT-C and BEAM-PERMIT-D read by SCU 2 are communicated via SLink 2 to DLN 2;
- DLN 1 computes the part of the FBIS decision logic that is relevant to BEAM-PERMIT-A and BEAM-PERMIT-B: DLN 1 sets its Local Beam Permit to state “NOK” when BEAM-PERMIT-A is “NOK” or BEAM-PERMIT-B is “NOK”;
- Likewise DLN 2 computes the part of the FBIS decision logic that is relevant to BEAM-PERMIT-C and BEAM-PERMIT-D: DLN 2 sets its Local Beam Permit to state “NOK” when BEAM-PERMIT-C is “NOK” or BEAM-PERMIT-D is “NOK”;
- If any Local Beam Permit is set to state “NOK” the respective DLN forces the Global Beam Permit to “NOK” by interrupting the Optical Protection Line.

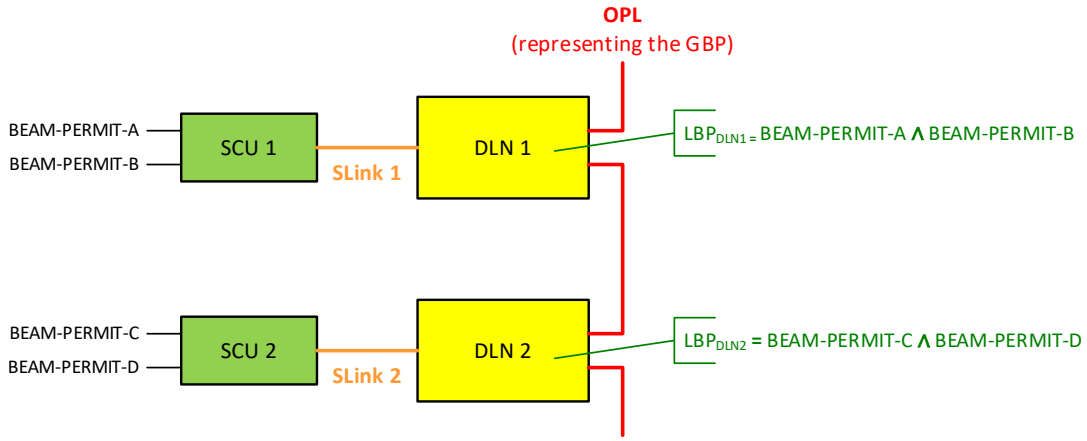


Figure 5: Example architecture with two SCUs connected to a DLN each.

3.4.2 Interfaces

The DLNs provide SLink interfaces and an optical protection line interface.

Additionally the DLNs are connected to:

- The FBIS Network
- Higher-Level Safety and Control Systems (via EPICS)
- The ESS Timing System

Figure 6 illustrates the interfaces of a single DLN.

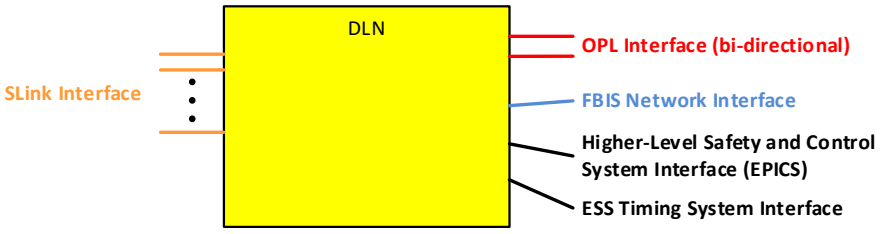


Figure 6: A DLN features multiple SLink interfaces, a bi-direction OPL interface, a FBIS Network interface as well as a Higher-Level Safety and Control System interface (EPICS) and a ESS Timing System interface.

3.4.3 Functional Behaviour

The DLN realizes the following basic functionalities:

- Deserialize the SCU data stream: The DLN deserializes the data stream(s) from one or multiple SCUs (or other DLNs)
- Provide latching and masking features: The DLN provides latching and masking features for discrete inputs and values received via data links.
- Interface with Higher-Level Safety and Control Systems: The DLN interfaces with Higher-Level Safety and Control Systems (aka EPICS) for configuration and diagnostic purposes.
- Interface with the ESS Timing System: The DLN interfaces with the ESS Timing System to retrieve triggers signals and timestamps and to receive information about the requested modes (e.g. Requested Proton Beam Mode).
- Logging: The DLN provides a logging feature.

The DLNs also compute the FBIS decision logic according to the current configuration and modes (e.g. according to the current Proton Beam Destination):

- State Evaluation: The DLN evaluates the state of all BEAM-PERMIT signals, READY signals and operational status and health information from Sensor Systems (and Actuation Systems if applicable).
- Compute Local Beam Permit: According to the FBIS Decision Logic and current configuration (e.g. latching, masking) the DLN computes a Local Beam Permit.
- Broadcast Local Beam Permit: The DLN broadcasts the Local Beam Permit via FBIS Network.
- Control the Global Beam Permit: The DLN controls the Global Beam Permit by means of the Optical Protection Line.
- Compute Local Enforced Proton Beam Destination: The DLN evaluates all Proton Beam Destination configuration information received from Sensor Systems (and Actuation Systems if applicable) and computes together with the requested Proton Beam Destination received via the Higher-Level Safety and Control System interface (EPICS) and the ESS Timing System a locally enforced Proton Beam Destination.
- Compute Local Enforced Proton Beam Mode: The DLN evaluates all Proton Beam Mode configuration information received from Sensor Systems (and Actuation Systems if applicable) and computes together with the requested Proton Beam Mode received via the Higher-Level Safety and Control System interface (EPICS) and the ESS Timing System a locally enforced Proton Beam Mode.
- Verify mode consistency among all DLNs: The DLN receives via the FBIS Network the locally enforced Proton Beam Destinations and locally enforced Proton Beam Modes of all other DLNs and verifies their consistency. If an inconsistency is detected the DLN enters the safe state.

Additionally:

- Perform self-diagnostic tests: The DLN performs self-diagnostic tests as appropriate, for example to detect power failures or over temperature. In case of a problem the DLN enters the safe state.
- Verify the SCUs are operational and functioning correctly: The DLN verifies that all SCUs are operational and correctly perform their functions. In case a SCU is not operational or does not perform its function and when this SCU handles signals relevant for the currently enforced Proton Beam Destination, the DLN enters the safe state.
- Perform SCU diagnostic checks: The DLN performs diagnostic checks all SCUs connected via SLink to the DLN. If a problem is detected the DLN enters the safe state.
- OPL Integrity Check: The DLN checks the integrity of the OPL by comparing the status read at the OPL inputs with information received via the FBIS Network Interface. If inconsistencies are detected, the DLN enters the safe state.
- Software Beam Permit: The DLN provides a Software Beam Permit which can be set via the Higher-Level Safety and Control System interface or the FBIS Network interface.
- Information about Latched Local Beam Permits: The DLN informs the ESS Timing System whether it latches a Local Beam Permit or not.

3.4.4 Architectural Application Options

The decision logic calculated in a DLN may also base on signals received from multiple SCUs and cover for example a 2oo3 evaluation[2]. If the signals for the 2oo3 evaluation is comming from different SCUs, these either need to be directly connected to the DLN as shown in Figure 7 on the left side or another DLN may "relay" (forward) the signal as shown on the right.

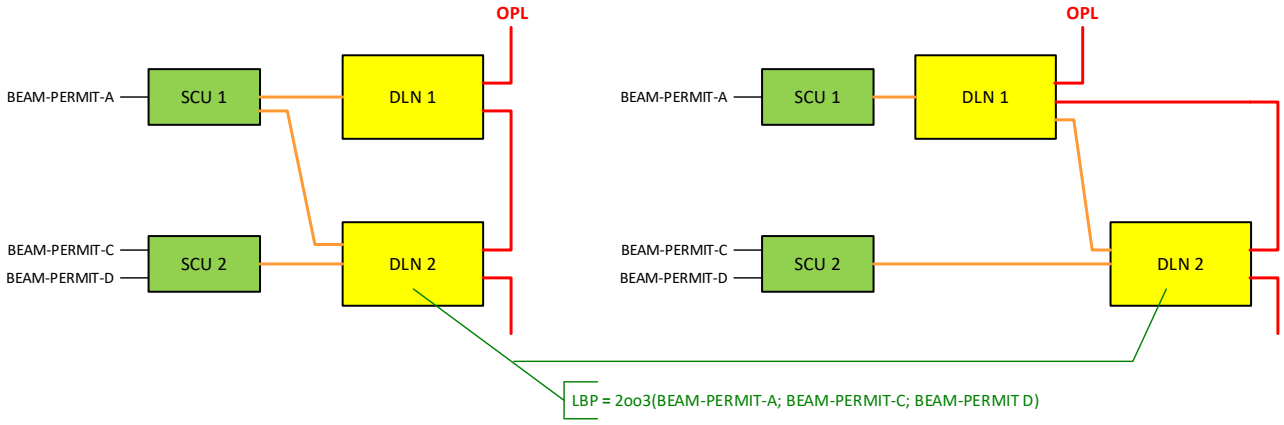


Figure 7: A DLN may also evaluate a 2oo3 function. If the signals is coming from different SCUs they either need to be directly connected to the DLN (left) or they may be "relayed" by another DLN (right).

3.5 Special Considerations for DLNs and SCUs Interfacing with Actuation Systems

Special considerations apply SCUs which interface with Actuation Systems and for the DLNs communicating with these SCUs. An example of such a SCU and DLN is given in Figure 1 at the very bottom or in Figure 8.

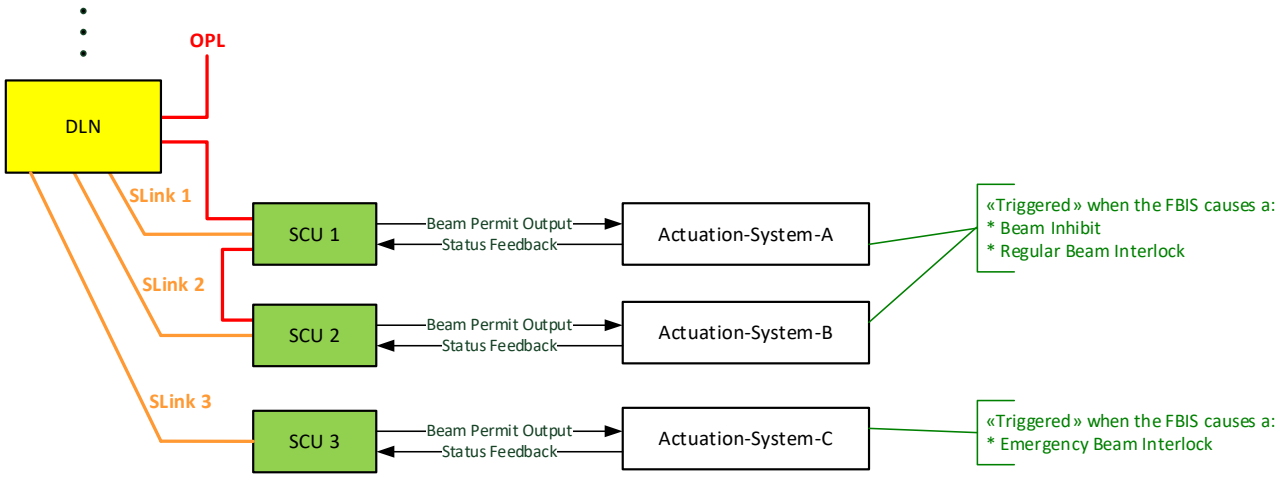


Figure 8: Example of SCUs interfacing with Actuation Systems. All SCUs communicate via SLink with a DLN. The SCUs "triggered" when the FBIS causes a Beam Inhibit or Regular Beam Interlock are directly connected to the OPL

Figure 8 illustrates the following setup:

- A single DLN interfaces with the SCU 1, SCU 2, and SCU 3
- SCU 1 interfaces with Actuation-System-A
- SCU 2 interfaces with Actuation-System-B
- SCU 3 interfaces with Actuation-System-C

[2] 2-out-of-3 means in this context the following: If two or all three signals are in state "NOK" the Local Beam Permit is set to "NOK" as well. If only one signal is in state "NOK" and the other signals are in state "OK" the Local Beam Permit is not set to "NOK".

- Every Actuation System features the following interface:
  - Beam Permit Output (FBIS output, Actuation System input)
  - Status Feedback (FBIS input, Actuation System output)

For the sake of this example we assume:

- Actuation System A shall be activated when the Global Beam Permit is in state “NOK”. In other words: Actuation System A is part of the Beam Inhibit and Regular Beam Interlock functions.
- Actuation System B shall be activated when the Global Beam Permit is in state “NOK” as well. Consequently Actuation System B is also part of the Beam Inhibit and Regular Beam Interlock functions.
- Actuation System C shall only be activated when one or both of the other two Actuation Systems fail to successfully switch-off beam. Actuation System C is hence part of the Emergency Beam Interlock function.

Whenever the Global Beam Permit is in state “NOK”, the signals “Beam Permit Output” to Actuation System A and B are automatically set such that the Actuation System switches-off beam. This functionality is realized directly in SCU 1 and SCU 2 by means of a hard-wired interrupt line. (Further details are described in chapter 4.1.6.2).

The DLN supervises SCU 1 and SCU 2 and checks whether the signals are correctly set. Additionally the DLN receives the “Status Feedback” signals from Actuation System A and B via SLink 1 and SLink 2. If the feedback does not reflect the expected states within a given timeout the Beam Inhibit, respectively Regular Beam Interlock is escalated to an Emergency Beam Interlock. In this case the Actuation System C is triggered by the DLN via SLink 3 and SCU 3.

3.6 Special Considerations for MP-related Systems Directly Interfacing with the Optical Protection Line

One of the architectural design constraints derived in /Design Options/ was to implement the FBIS such, that other parts of the BIS have direct access to MP-related Beam Switch-Off Actuation Systems. This is realized by allowing the MP-related Systems to directly influence the Optical Protection Line by means of a hard-wired interrupt line. (Further details are described in chapter 4.1.6.2).

Note that the FBIS could neither mask nor latch the signal from the MP-related System. However, the signal is read by the FBIS for diagnostic purposes.

Either a DLN or SCU can be used to realize this behaviour as shown in Figure 9.

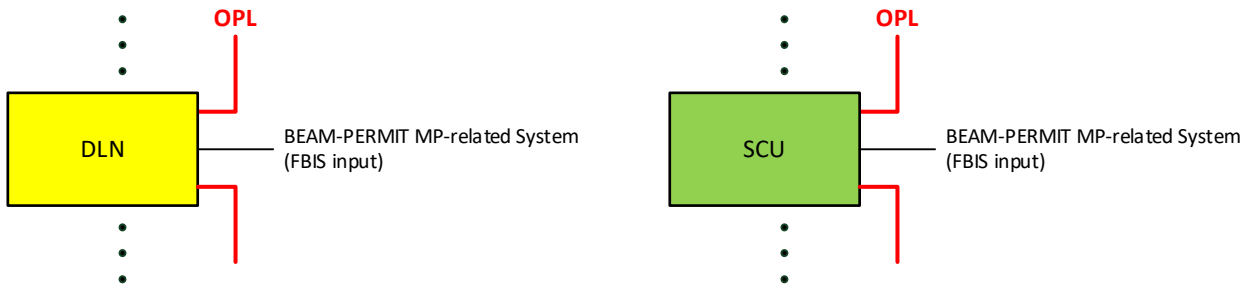


Figure 9:MP-related Systems may directly interface with the Optical Protection Line. Either a DLN or SCU can be used to realize this behaviour.

4 Realization Idea

This chapter contains realization ideas for the architectural entities and their interfaces introduced in chapter 3.

4.1.1 Signal Conversion Unit

Figure 10 shows the breakdown structure of a SCU.

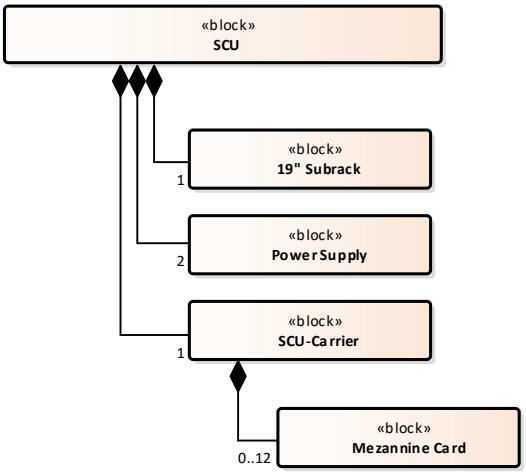


Figure 10: Breakdown structure of a Signal Conversion Unit (SCU). The numbers next to the blocks represent the count.

4.1.1.1 19” Subrack

As form factor for the SCU a 19” subrack is used. An example is shown in Figure 11. This form factor is standardized and widely used in industry. Every mechanical part can be ordered separately and usually different versions exist (such as heavy-weight, or EMC-shielded). The subracks are available in different heights and depths. A wide range of accessories such as front and rear-panels, rails, cover plates, cassettes, etc. are available.

Figure 11: Example of a 19” subrack by the company Pentair/Schroff.

4.1.1.2 Power Supply

Power for the SCU is provided by Euro-Card sized power supplies which are COTS devices. An example is given in Figure 12. In order to allow a hardware fault tolerance of 1 and to satisfy the high availability requirements the proposal foresees two redundant power supplies. If one of them fails the SCU is still fully operational and the operator is informed about the failure. The Power Supply is positioned with the help of guiding rails and fixed via the front panel to the 19” subrack. Replacement is very simple and can even be done while the SCU is in operation.

Figure 12: Example of a Euro-Card Power Supply with 220 V AC Net Power input and DC output voltage(s).

4.1.1.3 SCU-Carrier

The SCU-Carrier is the core part of a SCU. It features two FPGA's and Slots for up to 12 Mezannine Cards (MC). It also provides 2 times 4 SFP cages to realize the SLink interface to DLNs or other SCUs. 4 SLink interfaces are connected to FPGA A, the other four are connected to FPGA B. A schematic sketch of the SCU-Carrier with its interfaces is given in Figure 13.

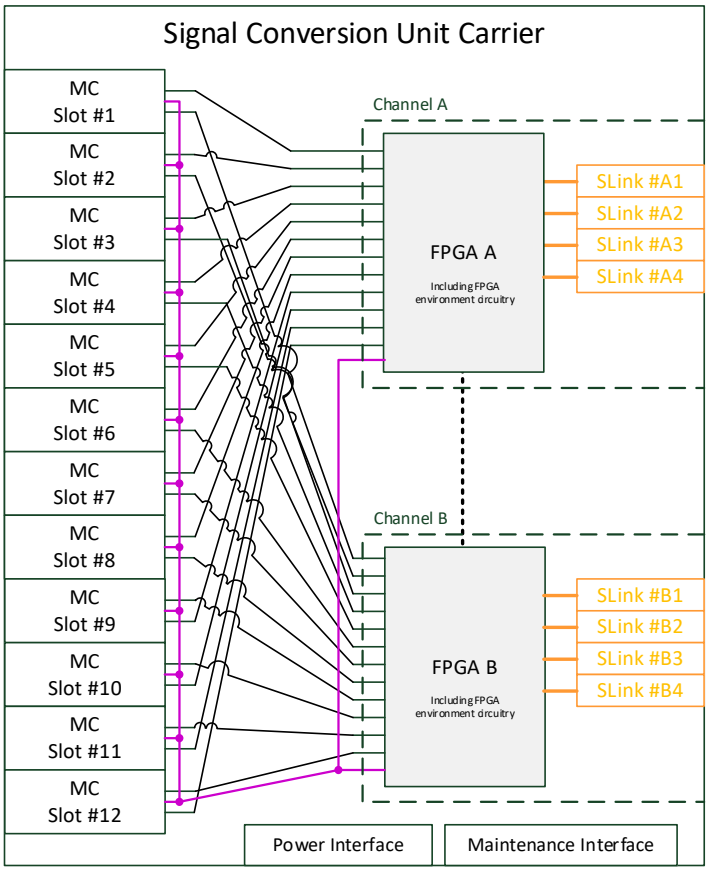


Figure 13: Schematic sketch of a SCU-Carrier.

As shown in the sketch, both FPGA have point-to-point signals routed to the MC Slots. This allows to realize a wide range of signalling patterns as described later in chapter 4.1.3.

The cross-verification functionality between the FPGAs is indicated by the dashed line in Figure 13.

The light violet line running across all MC slots and both FPGAs represent the interrupt functionality which is described later in chapter 4.1.6.2.

The Maintenance Interface allows to flash the Firmware and perform diagnostics during maintenance intervals.

The board is powered via the Power Interface.

A SCU may be equipped with up to 12 Mezzanine Cards. The Mezzanine Cards provide physical interfaces for example to Sensor Systems such as the RF system. Chapter 4.1.3 provides more details about the Mezzanine Cards and their interfaces

The Mezzanine Cards are coded by an ID which can be read-out by the FGPAs on the SCU-Carrier during runtime. This allows the firmware to check the correct MC is present and allows to abstract the SCU-Carrier firmware from the hardware configuration. One and the same base-firmware can be used on all SCU-Carriers.

Typically not all MC Slots of a SCU will be equipped. This has the following advantages:

- Unused signals are already discarded at SCU level (it is not necessary to provide interfaces on the DLN which are not used in the end)
- The number of signals handled by an SCU can be increased easily.
- If all slots of a SCU are occupied a second SCU could be added. If the DLN features a free SLink interface the second SCU can be easily connected to the DLN. If not, the SCU could be connected to another SCU using the reserve SLink interfaces.

The mechanical realization of the SCU and SCU-carrier shall take into account that MCs can be replaced individually. The replacement of one MC shall be possible without removing the SCU from its location and without having to unconnect the cables to the other MCs.

4.1.2 Decision Logic Node

The Decision Logic Nodes (DLNs) are the counter-parts to the SCU. Figure 14 shows the breakdown structure of a DLN equipped with redundant DLN-Carrier and DLN-RTM boards (which is the proposed standard configuration).

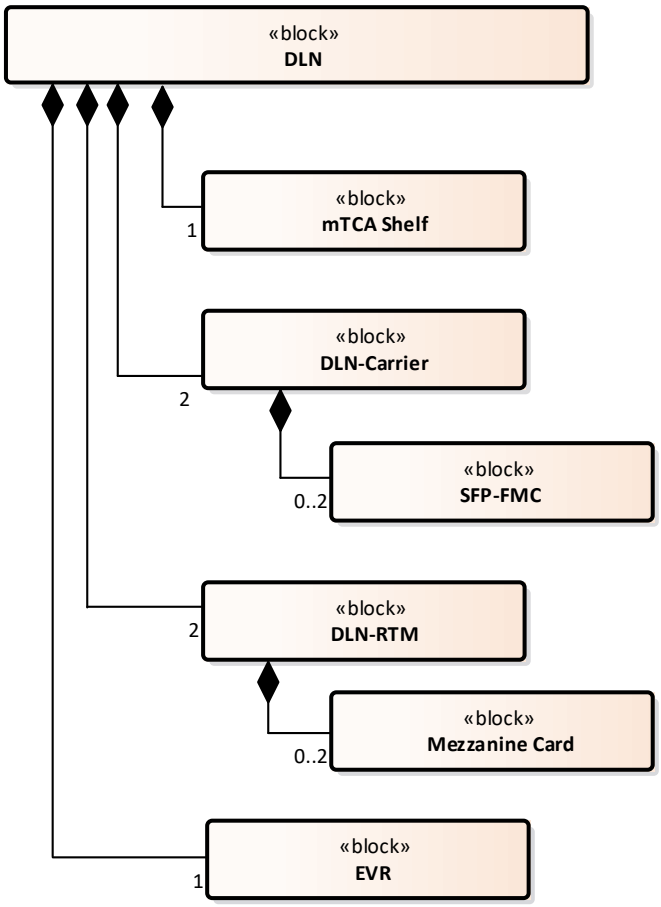


Figure 14: Breakdown structure of a Decision Logic Node (DLN). The standard configuration with two DLN-Carriers and DLN-RTMs is shown.

4.1.2.1 mTCA Shelf

The DLN bases on the mTCA.4 form factor which is a standardized and widely used form factor at ESS. Principally every type of mTCA.4 compatible shelf can be used. The proposal foresees a shelf with redundant power supplies for reasons of availability.

In the standard configuration with 2 DLN carriers s a total of 3 mTCA slots are occupied:

- DLN Carrier – Channel A (with DLN RTM module)
- DLN Carrier – Channel B (with DLN RTM module)
- ESS Timing System EVR (not RTM module)

A sketch of a 6 slot shelf as it will be used at ESS is given in Figure 15.

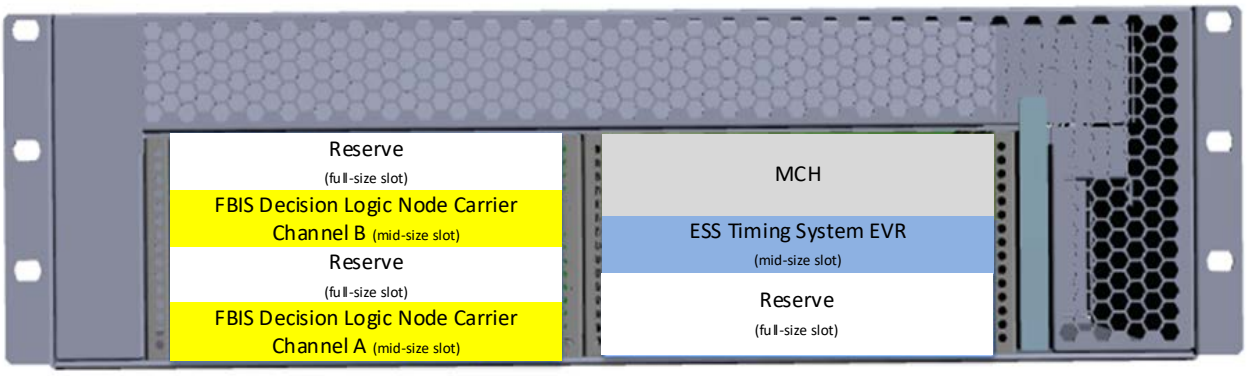


Figure 15: Sketch of a mTCA.4 Shelf equipped with a crate handler (MCH), ESS Timing System Event Receiver and redundant FBIS Decision Logic Node Carrier modules.

4.1.2.2 DLN-Carrier

As DLN-Carrier a IOxOS IFC-1410 card is used. The Carrier can be equipped with up to two FMCs. The DLN-Carrier is used in combination with a custom Rear Transition Module (RTM).

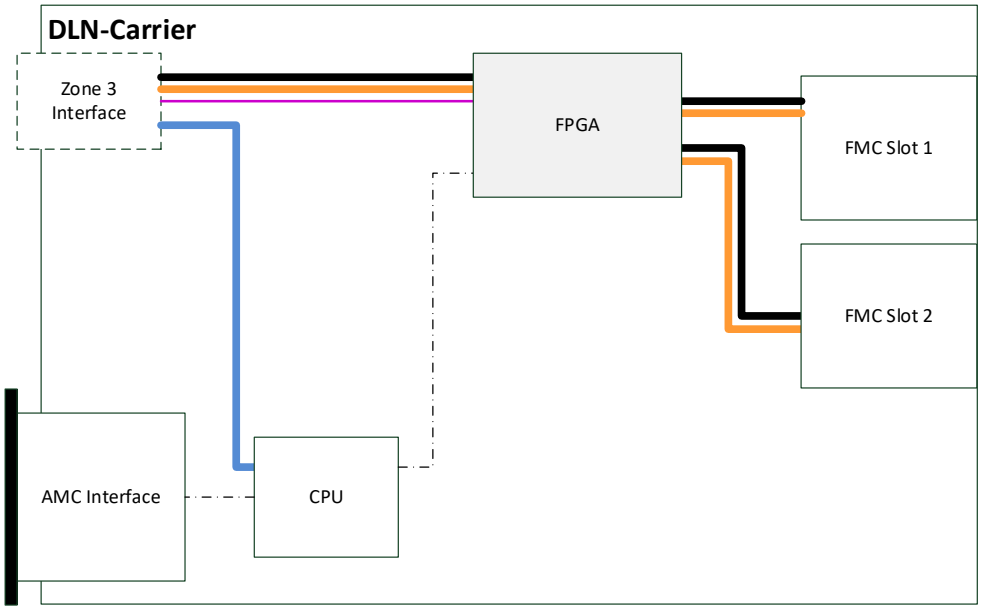


Figure 16: Schematic sketch of a DLN-Carrier.

When both FMCs are equipped with appropriate high-speed serial link modules, a single DLN-Carrier features up to 12 SLink Interfaces:

- 4 SLink interfaces on FMC Slot 1
- 4 SLink interfaces on FMC Slot 2
- 4 SLink interfaces on the DLN-RTM

FMCs with 4 high-speed serial links are commercially available.

Note that no hardware modifications to the IFC-1410 board are required. The board is used as shipped by IOxOS and simply flashed with the correct firmware.

While the FPGA calculates a part of the FBIS decision logic, the CPU provides the interface to the Control System (EPICS).

The FPGA receives information from the ESS Timing System EVR via the AMC Interface. This information includes: timestamp, triggers, and data.

4.1.2.3 DLN-RTM

The DLN-RTM is a custom made rear transition module. Two versions of this module exist featuring the following interfaces:

DLN-RTM Version 1

- 1 FBIS Network Interface
- 1 MC Slot
- 4 SLink Interfaces

DLN-RTM Version 2

- 1 FBIS Network Interface
- 2 MC Slots

Principally the DLN-RTM is based on the IOxOS RSP 1461 RTM which already features all above interface with the exception of the MC Slot(s).

Figure 17 shows a sketch of the DLN-RTM. Version 1 is shown on the left, Version 2 on the right.

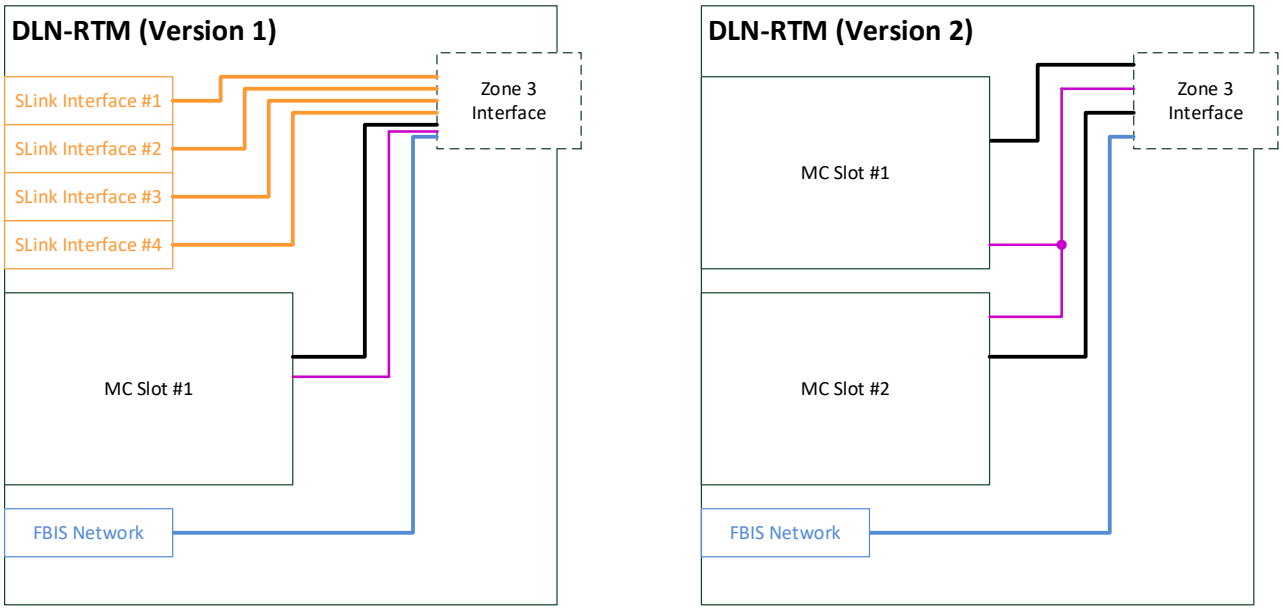


Figure 17: Schematic sketch of a DLN-RTM. Two configurations exist. One with a single MC slot and 4 SLink interfaces (Version 1, shown on the left) and one with two MC slots (Version 2, shown on the right).

4.1.3 SLink Interface

The interface between the SCUs and DLNs is realized by a high-speed serial data link referred to as “SLink”. The physical implementation is realized with optical SFP modules. The SFP form factor is standardized and extremely common in industry (especially in telecommunication). Various SFP modules (aka plug-ins) are commercially available featuring optical and electrical interfaces. Furthermore the SFP modules can be easily replaced on the fly. Figure 18 shows a picture of a SFP cage and module.

Figure 18: Picture of a SFP cage (left) and SFP module (right).

The protocol used by the SLink bases on the Xilinx Aurora lightweight link-layer protocol optimized for high-speed serial communication. This protocol provides full-duplex throughput rates up to Gbps with minimal latencies. Basing on this the FBIS makes use of the following “higher level” telegrams:

- A telegram which allows to communicate the state of a handful of discrete signals very efficiently and with minimal latency. This telegram is automatically broadcasted with highest priority.
- A telegram which allows to communicate the state of a few dozens of discrete signals and data link message fields efficiently and with minimal latency. This telegram is automatically broadcasted with the second highest priority
- A telegram which allows to read/write registers and memory areas. Unlike the above this telegram bases on a handshaking pattern between receiver and sender. In other words: This telegram is not automatically broadcasted.

4.1.4 Optical Protection Line

An Optical fibre with two strands is used to realize the Optical Protection Line. The two strands are necessary to allow bi-directional communication.

The OPL signal is daisy chained from node to node. The following explanations base on an example consisting of five DLNs all connected to the OPL. Figure 20 shows the example in the style typically used to represent the OPL throughout this document (see also Figure 1, Figure 5, etc.

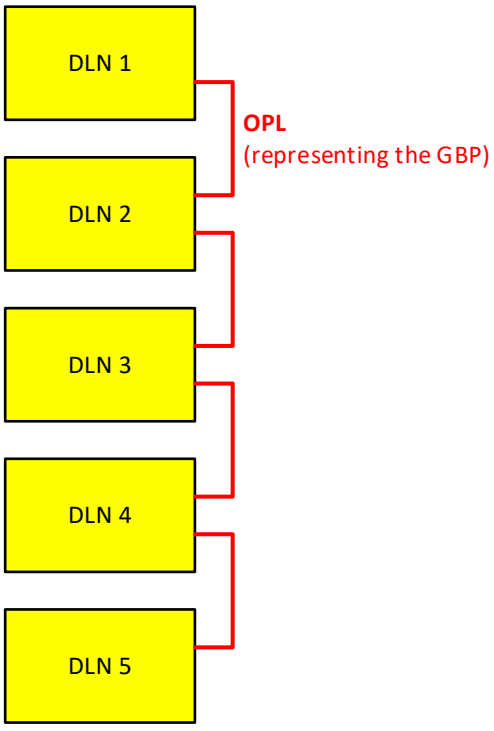


Figure 19: Example setup of five DLNs all connected to the Optical Protection Line.

Figure 20 shows the same example but with more details.

- The connection to the OPL is realized by means of Mezzanine Cards indicated as grey boxes within the DLNs and SCUs.
- DLN 2 through DLN 4 simply repeat the OPL signals (indicated by the abbreviation “OPLR”)
- DLN 1 and DLN 5 act as OPL signal termination. (indicated by the abbreviation “OPLT”)
- The OPL line consists of two fibre optic strands for the bi-directional communication
- Switches indicate the OPL Mezzanine Card feature to interrupt the OPL signal (the OPL Mezzanine card features a more elaborate circuit than one single simple switch per direction, see chapter 4.1.6.2)
- Red is used to indicate the OPL currently communicates Global Beam Permit = OK

Details about the OPL Mezzanine Card are given in chapter 4.1.6.2.

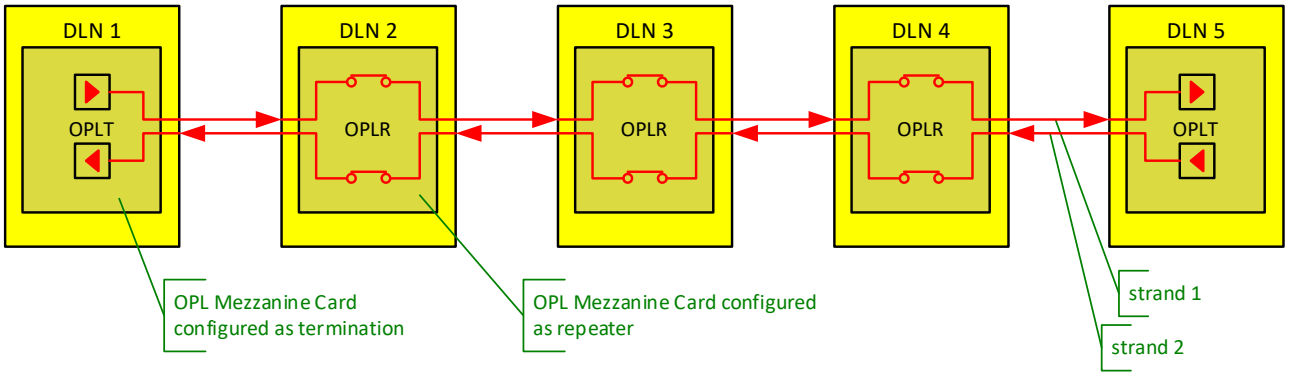


Figure 20: Same example structure as in Figure 28 but with more details.

The Global Beam Permit states OK and NOK are coded as follows:

- NOK = no light
- OK = square waveform with a frequency in the range of MHz

Figure 21 shows the situation when DLN2 interrupts the OPL signal.

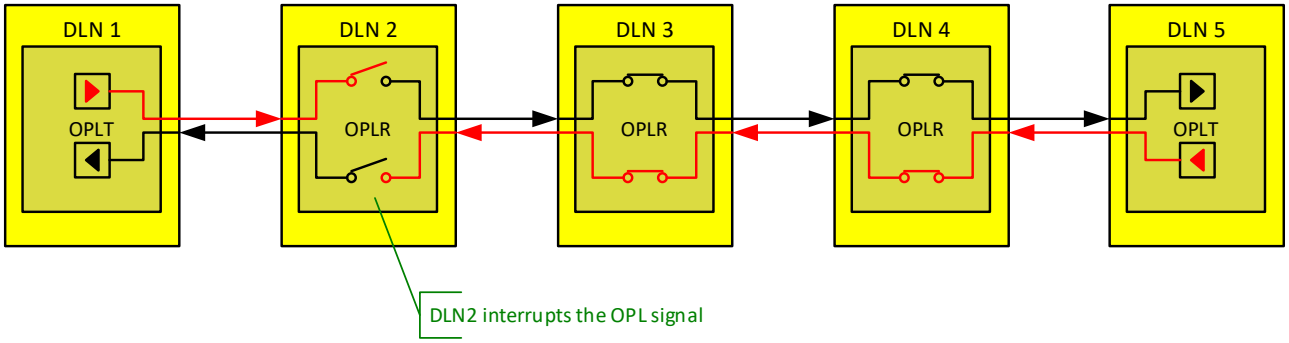


Figure 21: Situation when DLN2 interrupts the OPL signal.

4.1.5 Interrupt Line

The Mezzanine Card slots on the SCU-Carrier and the DLN-RTM feature a hard-wired interrupt line. Every Mezzanine Card is connected to the interrupt line. On the SCU-Carrier the interrupt line is also connected to the FGPAs (see Figure 13). On the DLN-RTM the interrupt line is connected via the Zone 3 connector to the FPGA on the DLN-Carrier (see Figure 17 and Figure 16).

Normally the interrupt line is pulled to high. This represents the state “No Interrupt”. When one of the Mezzanine Cards or FPGAs pull the line to ground this represent the state “Interrupt”.

The interrupt line is used in the context of Actuation System interfaces and the Optical Protection Line as follows:

Scenario 1: Actuation System Control based on OPL state

The Interrupt Line allows “triggering” Actuation System directly when an interruption of the Optical Protection Line is detected. This feature has already been mentioned in chapter 3.5. Figure 22 shows the setup:

- The OPL Mezzanine Card detects that the Global Beam Permit is “NOK” (i.e. no light is detected at the OPL input
- The OPL Mezzanine Card triggers an interrupt by pulling the Interrupt Line to ground
- The LEBT Chopper Actuation System Mezzanine Card detects the interrupt
- The LEBT Chopper Actuation System Mezzanine Card “triggers” the Actuation System as necessary

The little arrow of the interrupt line in Figure 22 represents that the OPL Mezzanine Card is the “sender” of the interrupt.

Note that this scenario does not base on any functionality implemented in the FPGA (shown on the very left in Figure 22). However, the FPGA may take over a supervising role and interfere if necessary.

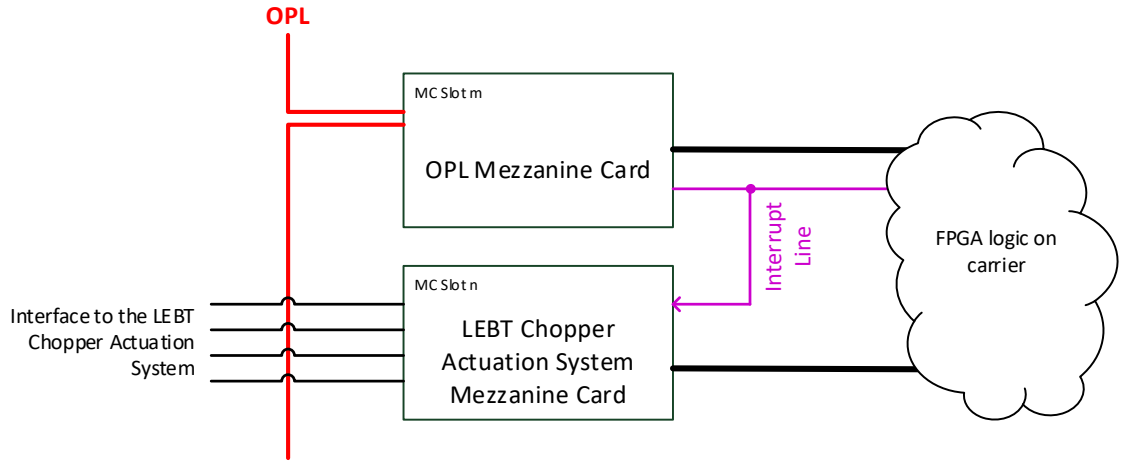


Figure 22: Setup which the Optical Protection Line to directly “trigger” Actuation System. In this figure the LEBT Chopper as example.

Scenario 2: Direct OPL interruption via MP-related System

The Interrupt Line allows MP-related Systems to directly interrupt the Optical Protection Line. In other words: the MP-related Systems have direct means to force the Global Beam Permit to “NOK” and through this request a beam switch-off. This feature has already been mentioned in chapter 3.6 and may for example be used by PLC based local protection systems (LPS). Figure 23 shows the setup:

- The PLC based LPS Mezzanine card detects a NOK input
- The PLC based LPS Mezzanine Card triggers an interrupt by pulling the Interrupt Line to ground
- The OPL Mezzanine Card detects the interrupt and interrupts the Optical Protection Line
- The interruption of the Optical Protection Line results in a beam switch-off

The little arrow of the interrupt line in Figure 23 represents that the OPL Mezzanine Card is the “receiver” of the interrupt.

Note that this scenario does not base on any functionality implemented in the FPGA (shown on the very left in Figure 23). However, the FPGA may take over a supervising role and interfere if necessary.

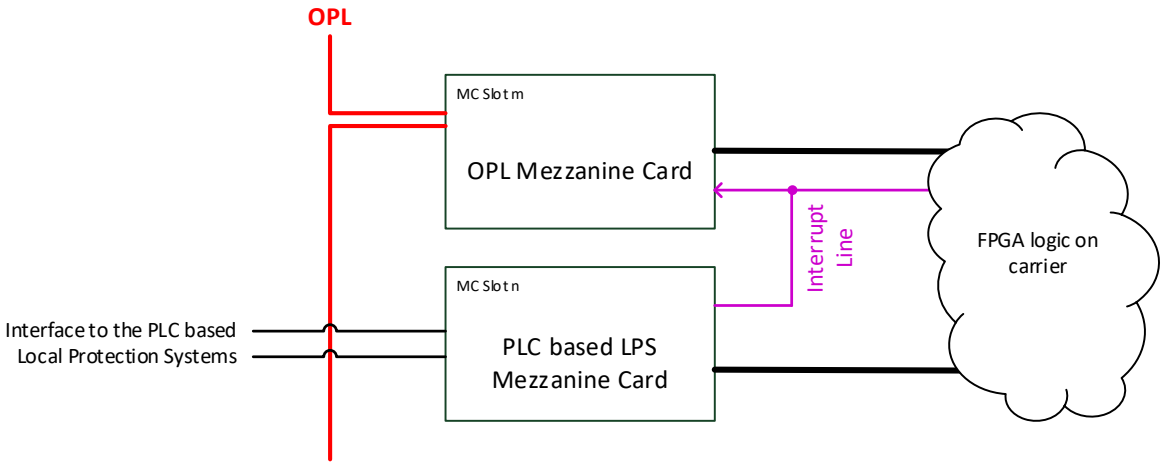


Figure 23: Setup which allows MP-related Systems to directly interrupt the Optical Protection Line.

4.1.6 Mezzanine Cards

Different types of Mezzanine Cards are developed depending on the requirements of the Sensor System, respectively Actuation System.

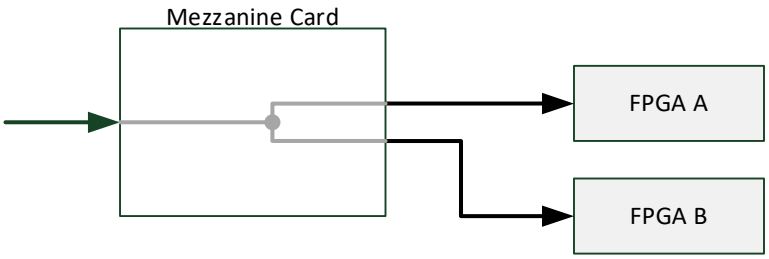
While chapter 4.1.6.1 describes the signalling patterns which can be achieved chapters 4.1.6.2 through 4.1.6.4 describe concrete Mezzanine Cards. Only a subset of cards is described. Additional ones will have to be defined.

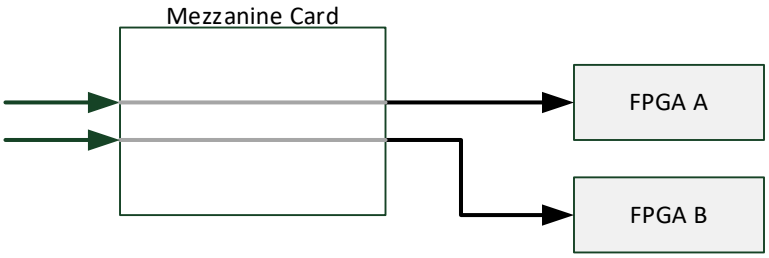
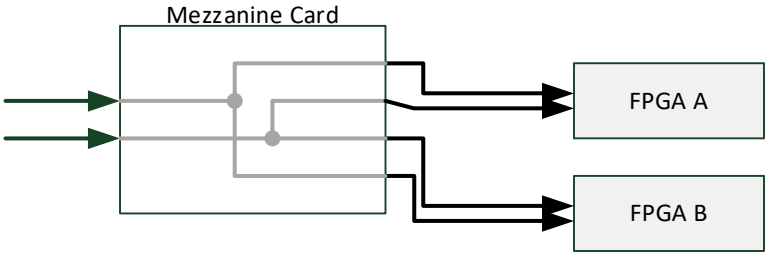
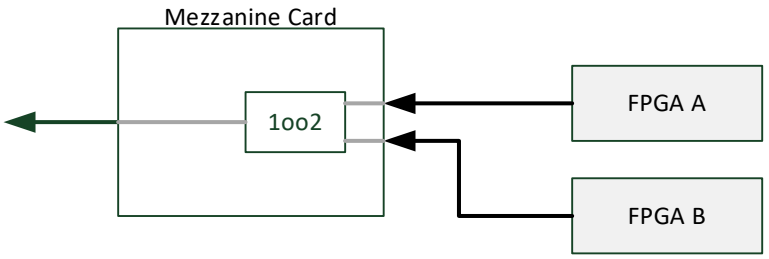
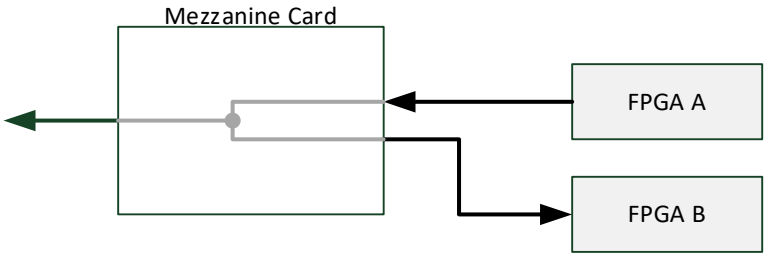
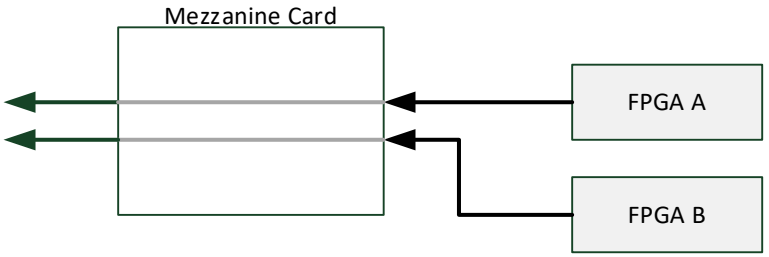
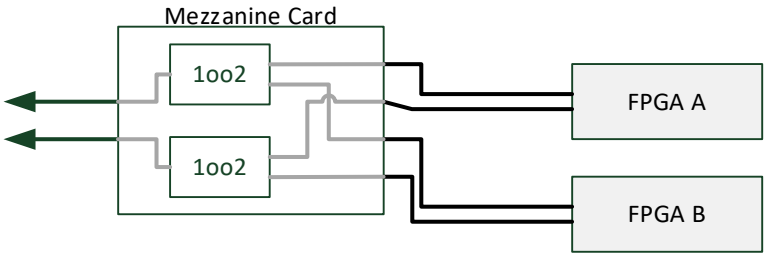
4.1.6.1 Signalling Patterns

This chapter describes the architectural signalling patterns which can theoretically be implemented. Chapter **Fehler! Verweisquelle konnte nicht gefunden werden.** describes the concrete Mezzanine Cards needed for ESS which base on these patterns.

As every Mezzanine Card-Slot interfaces directly with both FPGAs a wide range of architectural signalling patterns can be realized. A subset of the patterns is described in Table 3.

Table 3: MC signaling patterns (non-exhaustive list)

Signalling Patterns for Input Signals	
A single input signal may be routed to both FPGAs. Ideally via a driver which decouples the two outputs to FGPA A and FPGA B.	

A redundant input signal may be split and each single signal connected to a FPGA.	
Alternatively, a redundant input signal may be redundantly connected to both FPGAs.	
Signalling Patterns for Output Signals	
A single output signal may be driven by both FPGAs with the help of a 1oo2 circuit.	
Alternatively an output signal may be driven by only one FPGA and supervised by the redundant FPGA.	
A single signal from each FPGA may be used to drive a redundant output signal.	
Analogously to the pattern above, redundant signals from both FPGAs may be used to drive a redundant output signal with the help of two 1oo2 circuits.	

In the context of the ESS FBIS primarily Mezzanine Cards processing input signals will be used. The signalling pattern can be chosen according to the interface realized. A mixture between different signalling-patterns is possible.

4.1.6.2 OPL Mezzanine Card

The OPL MC features the following interfaces and functions:

- Two pairs of optical receivers and transmitters
- Two fast switches evaluating a Boolean “Enable”-signal as switching-input (when the boolean signal is “low” the OPL signal is interrupted)
- Two dynamic switches evaluating a rectangular “Heartbeat”-waveform as switching-input (when waveform is missing or too slow, the OPL signal is interrupted)
- A unique ID to unambiguously identify each single MC
- An interface towards the carrier featuring the following signals:
    - I2C interface
    - Signal strength of both receivers
    - OPL signals as detected by receivers and as transmitted
    - Enable signals
    - Heartbeat signals
    - Interrupt line
    - Power for the MC

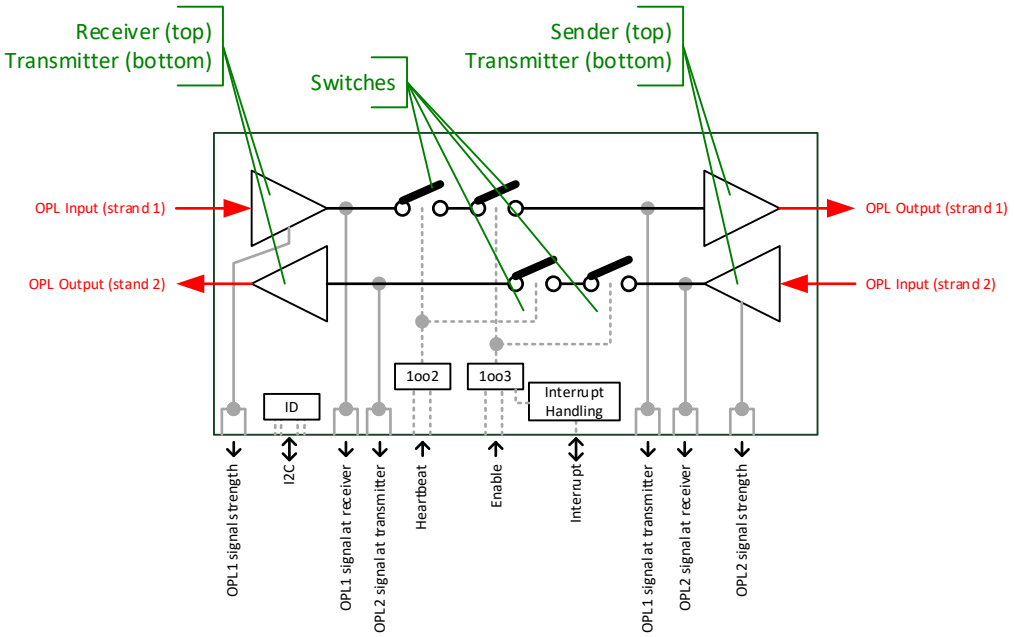


Figure 24: OPL MC configured as bi-directional repeater. (OPL repeater configuration, OPLR)

The MC can be used on SCU-Carriers but also DLN-RTMs. The 1oo2 and 1oo3 circuits is foreseen when used on a SCU-Carrier. One signal will be provided by FPGA A, the second by FPGA B. The third signal for the 1oo3 voter can be connected to the Interrupt.

The Interrupt Handling can be configured as follows:

- Either the OPL reacts to interrupts by interrupting the OPL signal, or
- The OPL itself creates an interrupt when no OPL signal is received on one or both strands

All outputs are made available to both FPGAs.

When used on a DLN-RTM the redundancy pattern will not be available as the DLN-RTM interfaces with only one DLN-Carrier and not two. The DLN-RTM will therefore have to take care of the correct signal routing and interface with all signals of the MC. The ones assigned to Channel A and Channel B.

A simple interface (e.g. I2C) allows to readout a unique ID and eventually configuration information of the MC. This interface is routed to FPGA A and B as well.

Figure 24 shows the standard configuration of the OPL MC as used by the majority of the DLN-RTMs. Figure 25 shows an alternative configuration (assembly variant, the PCB could be the same). This configuration is used at the “start” and “end” of the optical protection line and realized the protection line termination.

The main difference to the standard configuration is the following:

- Only one pair of optical receiver and transmitter is provided
- The transmitter is connected to a OPL modulation signal provided by the carrier

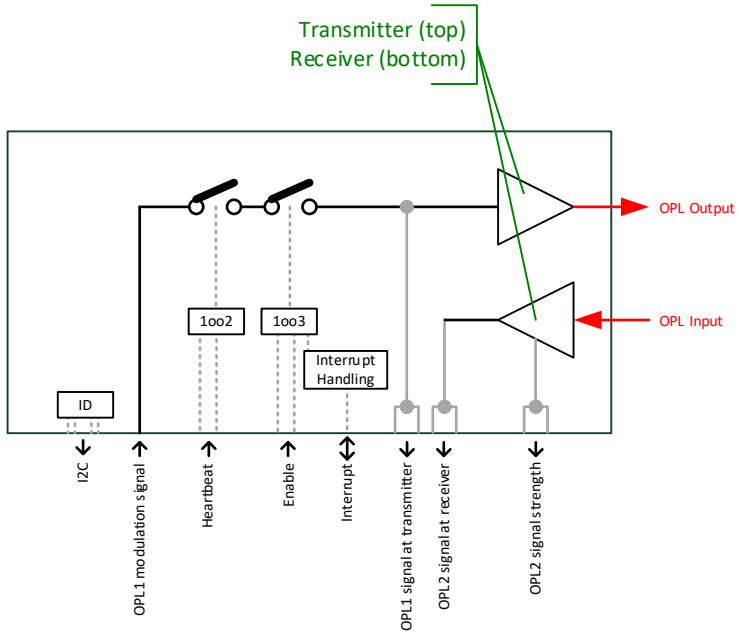


Figure 25: OPL MC configured as “start or “end” of the Optical Protection Line. (OPL termination configuration, OPLT)

Table 4 shows the interface signals towards the carrier board of the OPL MC. The carrier may be either a SCU-Carrier or DLN-RTM.

Table 4: OPL MC interface. The last two columns specify whether the signal is routed to Channel A or B of the MC carrier. In case of the OPL MC this can either be a SCU-Carrier or DLN-RTM.

	OPL repeater configuration		OPL termination configuration		Channel	
	Signal	Direction[1)]	Signal	Direction[1)]	A	B
1	OPL1 signal strength	Out	-	-	X	X
2	OPL1 signal at receiver	Out	OPL1 modulation signal	-	X	X
3	OPL1 signal at receiver	Out	OPL1 modulation signal [2)]	-	X	X
4	OPL1 signal at transmitter	Out	OPL1 signal at transmitter	Out	X	X
5	Enable	In	Enable	In	X	X
6	Heartbeat	In	Heartbeat	In	X	X
7	OPL2 signal strength	Out	OPL2 signal strength	Out	X	X

8	OPL2 signal at receiver	Out	OPL2 signal at receiver	Out	X	X
9	OPL2 signal at transmitter	Out	-	-	X	X
10	SCL (I2C) 3)	In	SCL (I2C) 3)	Input	X	X
11	SDA (I2C) 3)	InOut	SDA (I2C) 3)	InOut	X	X
12	Interrupt 3)	InOut	Interrupt 3)	InOut	X	X
13	VCC (power supply) 3)	-	VCC (power supply) 3)	-	-	-
14	GND (power supply) 3)	-	GND (power supply) 3)	-	-	-

1) Directions as seen from MC

2) Only one of the Channels may actively drive the signal. Using a 1oo2 pattern to drive the signal would be possible when the OPL signal is a DC-signal or when the OPL signal is a square waveform and it could be ensured that Channel A and B are in sync

3) Identical for all Mezzanine Cards

4.1.6.3 Struck Mezzanine Card

The Struck MC features the following interfaces and functions:

- Three RJ45 connectors featuring 4 LVDS lines each
- A galvanic isolation of the LVDS signals from the rest of the MC
- A unique ID to unambiguously identify each single MC
- An interface towards the carrier featuring the following signals:
  - I2C interface
  - Three READY signals
  - Three BEAM-PERMIT signals
  - Three RX/TX pairs to realize three bidirectional DataLink interfaces
  - Power for the MC

Figure 26 shows a sketch of the MC.

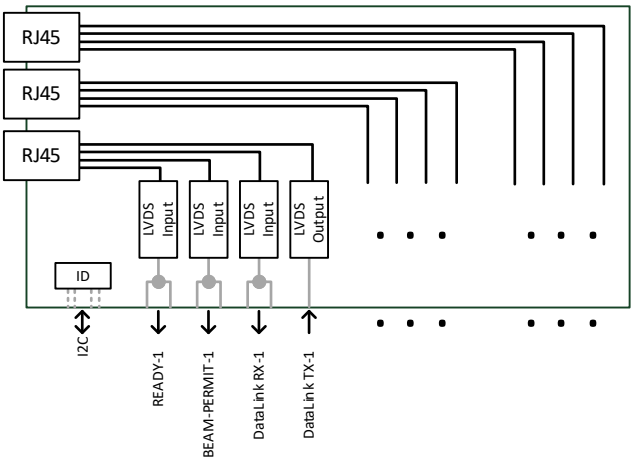


Figure 26: Struck MC.

Table 5 lists the interface to the MC carrier. Although principally usable on a DLN-RTM it is expected that this MC will only be used on the SCU-Carrier.

Table 5: Stuck MC interface. The last two columns specify whether the signal is routed to SCU Channel A or B.

Signal	Direction 1)	Channel

			A	B
1	READY-1	Out	X	X
2	BEAM-PERMIT-1	Out	X	X
3	DataLink RX-1	Out	X	X
4	DataLink TX-1	In	X	-
5	READY-2	Out	X	X
6	BEAM-PERMIT-2	Out	X	X
7	DataLink RX-2	Out	X	X
8	DataLink TX-2	In	X	-
9	READY-3	Out	X	X
10	BEAM-PERMIT-3	Out	X	X
11	DataLink RX-3	Out	X	X
12	DataLink TX-3	In	X	-
13	SCL (I2C) [2)]	In	X	X
14	SDA (I2C) [2)]	InOut	X	X
15	VCC (power supply) [2)]	-	-	-
16	GND (power supply) [2)]	-	-	-

1) Directions as seen from MC

2) Identical for all Mezzanine Cards

One Struck MC can hence interface with up to three Struck boards.

4.1.6.4 IFC Mezzanine Card

The IFC MC features the following interfaces and functions:

- One RJ45 connectors featuring a bi-directional 100 Bits/s Ethernet interface
- Two discrete READY inputs using the electrical specification of RS422
- Two discrete BEAM-PERMIT inputs using the electrical specification of RS422
- A galvanic isolation of the RS422 signals from the rest of the MC
- A unique ID to unambiguously identify each single MC
- An interface towards the carrier featuring the following signals:
    - I2C interface
    - Three READY signals
    - Three BEAM-PERMIT signals
    - Three RX/TX pairs to realize three bidirectional DataLink interfaces
    - Power for the MC

Figure 27 shows a sketch of the MC.

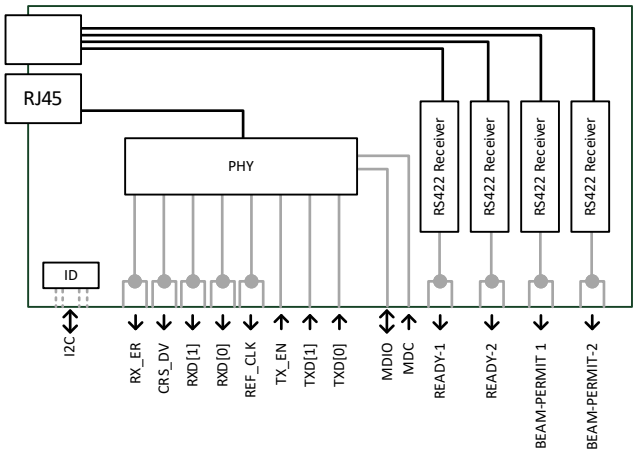


Figure 27: IFC MC.

Table 6 lists the interface to the MC carrier. Although principally usable on a DLN-RTM it is expected that this MC will only be used on the SCU-Carrier.

Table 6: IFC MC interface. The last two columns specify whether the signal is routed to SCU Channel A or B.

	Signal	Direction [1)]	Channel	
			A	B
1	RX_ER	Out	X	X
2	CRS_DV	Out	X	X
3	RXD[1]	Out	X	X
4	RXD[0]	Out	X	X
5	REF_CLK	Out	X	X
6	TX_EN	In	X	-
7	TXD[1]	In	X	-
8	TXD[0]	In	X	-
9	MDIO	InOut	X	-
10	MDC	In	X	-
11	READY-1	Out	X	X
12	READY-2	Out	X	X
13	BEAM-PERMIT-1	Out	X	X
14	BEAM-PERMIT-2	Out	X	X
15	SCL (I2C) [2)]	In	X	X
16	SDA (I2C) [2)]	InOut	X	X
17	VCC (power supply) [2)]	-	-	-
18	GND (power supply) [2)]	-	-	-

1) Directions as seen from MC

2) Identical for all Mezzanine Cards

4.1.7 FBIS Network

The FBIS Network bases on standard Ethernet technology and connects all DLN-Carriers. The FBIS Network is used to distribute DLN mode information and for diagnostic purposes.

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5 The Architecture Layout for ESS

The structure of the DLNs and SCUs is based on the physical beam line sections of the LINAC and the racks, rack lines and rack islands[3].

Chapter 5.1 and 5.2 discuss the layout for the Klystron Gallery and Front-End-Building. Chapter 5.3 contains a latency evaluation.

5.1 Along the Klystron Gallery

Along the Klystron Gallery the following basic pattern is used:

- Every beam line section (for example the DTL-section) is equipped with one DLN featuring redundant DLN-Carriers and DLN-RTMs.
- The DLN is installed in the rack closest to the beginning of the Gallery (closest to the front-end-building) in a rack owned by MPS. This location is chosen in order to minimize cable lengths. For the DTL-section this is rack line DTL-010, rack number 5.
- In every rack island, including the one with the DLN, a SCU is installed. This is a rack owned by MPS as well. Unless the rack island spans across two sections - an SCU for each section is installed.
- The SCU is equipped with MC modules as necessary to interface with the Sensor and Actuation Systems[4]. The type of the modules depend on the Sensor and Actuation Systems installed in the rack line and may vary from SCU to SCU.
- The SCU interfaces with the Sensor and Actuation System via local patch cables (local refers here to “within the same rack island”).
- The SCU interfaces with the DLN via a SLink interface.
- The DLN interfaces with the Control System and ESS Timing System.

Figure 28 shows a schematic sketch of the pattern.

[3] Sometimes also called “rack enclosures”.

[4] The only Actuation System located on the Klystron Gallery is the ESS Timing System Event Generator.

Figure 28: Deployment of a DLN and SCUs along the Klystron Gallery. The orange lines represent SLink interfaces.

As in chapter 4 described both, the DLN and SCU feature redundant channels (In the following referred to as “Channel A” and “Channel B”):

- The structure of the SCU, respectively the SCU-Carrier itself already features two channels (see Figure 13)
- According to chapter 4.1.2.1 (and as shown Figure 15) every DLN is equipped with two DLN-Carriers including DLN-RTMs
- Out of the four available SLink Interfaces of the DLN-RTM one is used to interface to the SCU, the other is used to interface with the redundant DLN-Carrier for cross-verification.

- If more SCUs need to be connected the FMC slots of the DLN-Carriers are used. This allows to connect up to 11 SCUs to one single DLN-Carrier.

Figure 29 shows a sketch of the redundancy pattern.

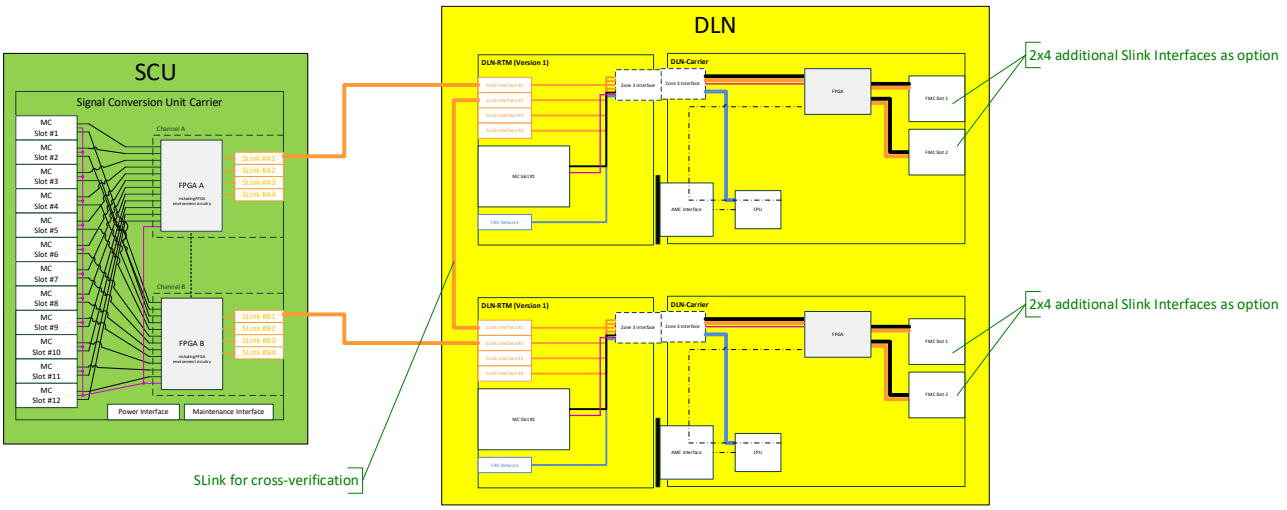

Figure 29: The redundant channels span across SCU and DLN.

Figure 30 shows the deployment along the Klystron Gallery as Figure 28 but the redundant channels of the SCU, DLN and the redundant SLink interface between them is explicitly indicated. If a Sensor System already provides redundant signals, they are directly connected to Channel A and Channel B of the SCU. If not the SCU itself takes care about the replication (the Mezannine Cards need to be designed accordintly).

Figure 30: Similar sketch to Figure 28 but the redundant channels of the SCU, DLN and SLink are explicitly shown.

Every DLN computes according to its own decision logic a local beam permit. The local beam permit is used to interrupt the optical protection line which represents the Global Beam Permit. The Optical Protection line is bi-directionally routed from DLN to DLN in a daisy-chain pattern as described in chapter 4.1.4. There exists one protection line for Channel A and one for Channel B as illustrated in Figure 31. If any of the DLN interrupts the line the DLNs upstream and downstream detect the interruption.

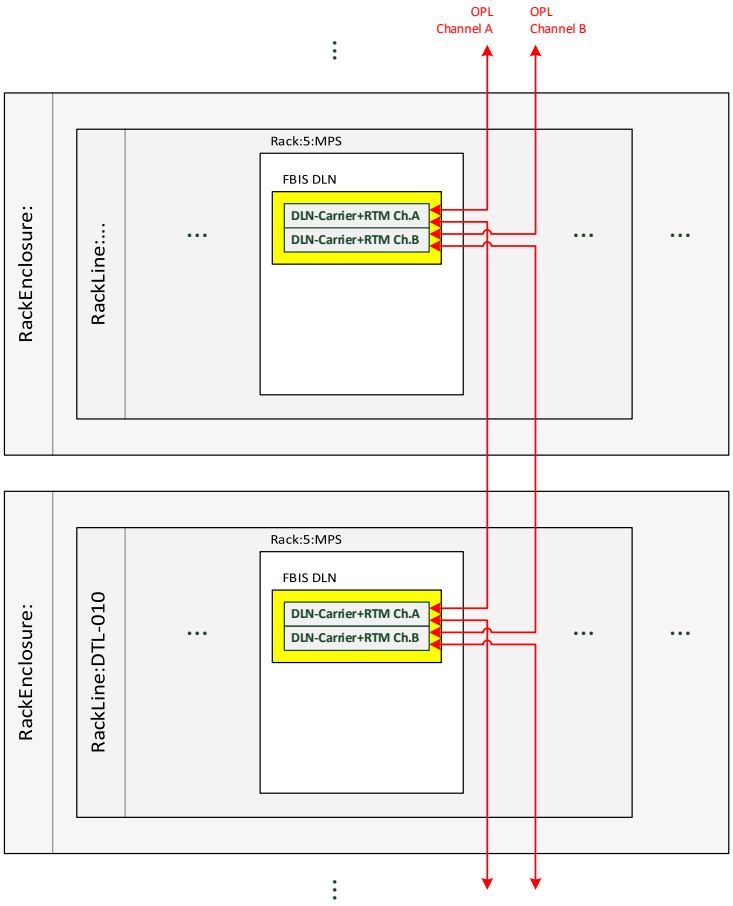

Figure 31: Two bi-directional optical protection lines are daisy-chained from DLN to DLN along the Klystron Gallery.

A DLN-Carrier interrupts the Global Beam Permit line when:

- the decision logic computation results in a beam switch-off request
- it detects an inconsistency with the computation of the partner channel (cross-verification)
- it detects any internal problem (e.g. power failure, clock problem, …)

While the DLN-Carrier requests the interruption it is the OPL-MC mounted on the DLN-RTM which actually interrupts the optical protection line.

5.2 In the Front-End-Building

The pattern in the Front-End-Building is slightly different from the pattern along the Klystron Gallery. First of all, there are no Rack islands in that building but simply a number of rack lines standing close to each other. Additionally, the pattern is different as the majority of Actuation Systems is located within that building. Figure 32 shows a sketch of the pattern. The redundancy pattern is identical to the Klystron Gallery and therefore not explicitly shown in the sketch:

- Principally one SCU per Actuation System exists with the exception of the Ion Source for which two SCUs are foreseen:
  - FBIS SCU (LEBT Ch.) manages the interface to the LEBT Chopper. This SCU is directly connected to the OPL.
  - FBIS SCU (MEBT Ch.) manages the interface to the MEBT Chopper. This SCU is directly connected to the OPL.
  - FBIS SCU (IS BIF/RBIF) manages the interface to the Ion Source but only with respect to the Beam Inhibit function (BIF) and Regular Beam Interlock functions (RBIF). This SCU is directly connected to the OPL.

- FBIS SCU manages the interface to all Sensor Systems located in the Front-End-Building including PLC based Local Protection Systems. Later is the reason why this SCU is directly connected to the OPL as well (see chapter 3.6 for further information)
- FBIS SCU (IS EBIF) manages the interface to the Ion Source but only with respect to the Emergency Beam Interlock functions (EBIF). This SCU is not connected to the OPL. If the FBIS escalates to an Emergency Beam Interlock Function the DLN initiates the request (communicated via SLink and the SCU to the Ion Source) to interrupt the power to the Plasma and High-Voltage Platform of the Ion Source.

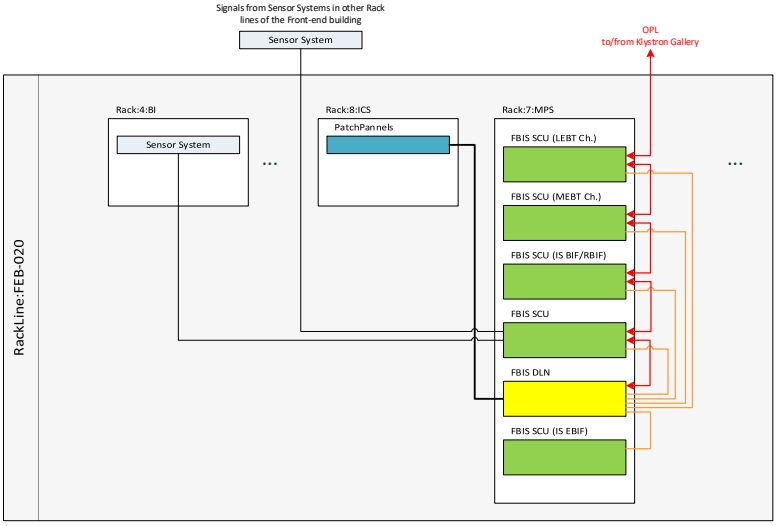

Figure 32: Deployment of a DLN and SCUs in the Front-End-Building.

Figure 33 shows a sketch of the redundancy pattern for the DLN and one SCU.

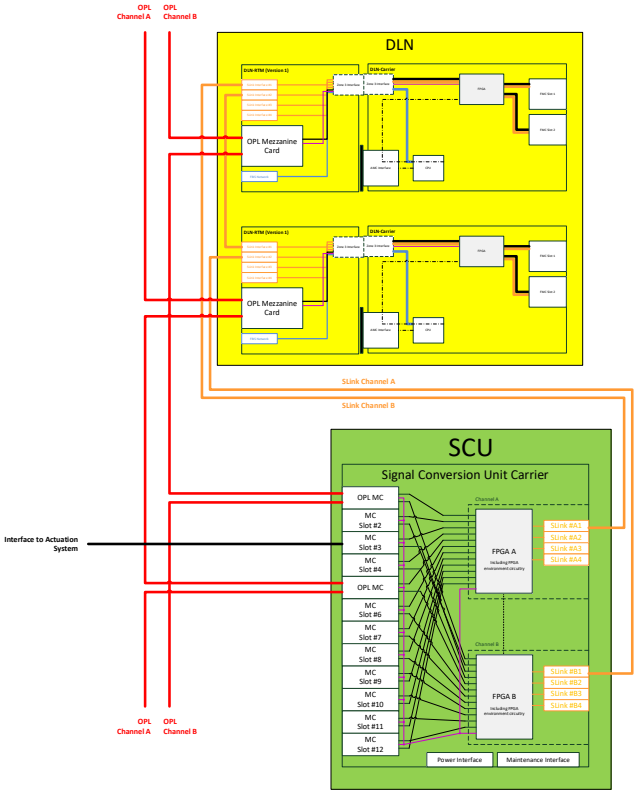

Figure 33: Redundancy pattern in the Front-End-Building. Only the DLN and one SCU is shown.

The FBIS Network follows the redundancy pattern of Channel A and Channel B as well. Two separate networks exist as illustrated in Figure 34.

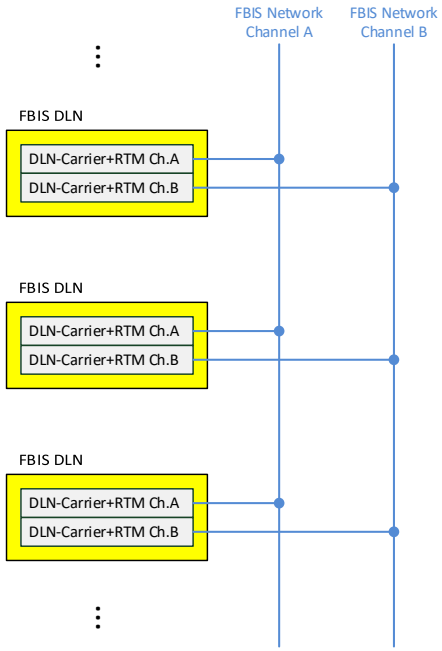

Figure 34: FBIS Network pattern.

5.3 Latency Evaluation

Figure 35 shows the layout of SCUs and DLNs for ESS including the expected latencies.

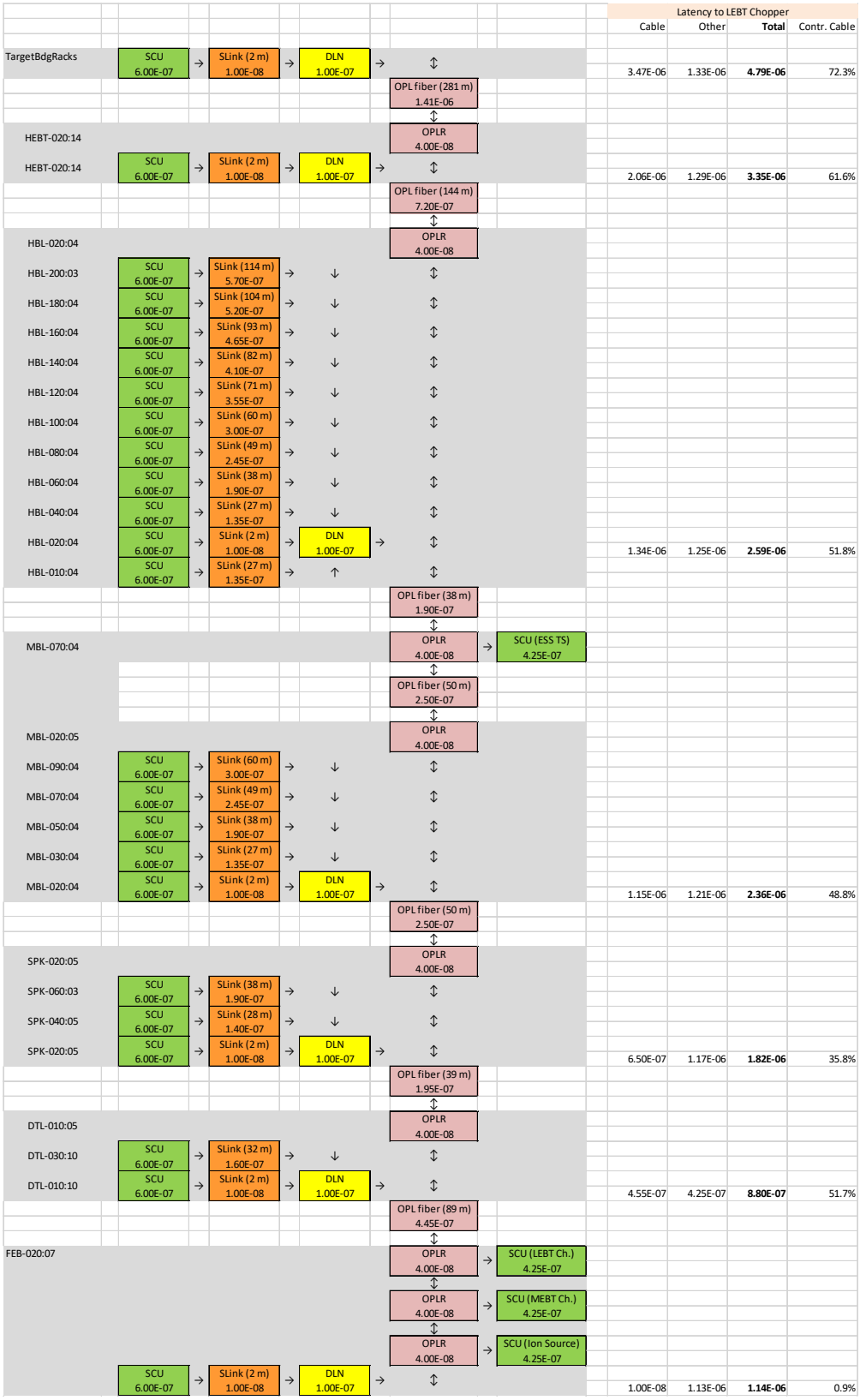

Figure 35: Expected signal latencies.

The columns at the right side show the added up latency from Sensor System SCUs at different locations to the LEBT Chopper SCU. The values need to be interpreted as following:

- "Cable" represents the latency introduced by the SLink and the OPL fibers
- "Other" represents the latency introduced by the SCU, DLN and OPLR
- "Total" represents the overall latency
- "Contr. Cable" expresses the contribution of the cable to the total latency

The latency evaluation in Figure 35 is based on the assumptions given in Figure 36 and Figure 37.

SCU (used to interface Sensor Systems)

Parameter	Value
FPGA Clock [Hz]	4.00E+08

Action		Latency [s]
Input processing [Clock Cycles]	40	1.00E-07
SLink Latency [s]	5.00E-07	5.00E-07
Total		6.00E-07

DLN

Parameter	Value
FPGA Clock [Hz]	4.00E+08

Action		Latency [s]
Input processing [Clock Cycles]	40	1.00E-07
Disabling OPL line [s]	2.00E-08	2.00E-08
Total		1.00E-07

For simplification the latency to disable the OPL line is assigned to the DLN.
As a consequence of that the OPL Termination does not need to be explicitly modelled

OPL Repeater

Action		Latency [s]
Propagate OPL input to output [s]	4.00E-08	4.00E-08
Total		4.00E-08

Optical Fibre

Parameter	Value
Optical fiber signal latency [s/m]	5.00E-09

SCU (used to interface Actuation Systems)

Parameter	Value
FPGA Clock [Hz]	4.00E+08
OPL Frequency [Hz]	5.00E+06

Action		Latency [s]
OPL Interruption detection [cycles]	2	4.00E-07
Input processing [Clock Cycles]	10	2.50E-08
Total		4.25E-07

Figure 36: Parameters assumed for the latency evaluation.

Guessed values
Fields to edit

	From	To	Total Distance [m]	Rack to cable tray	location "From" to rack 1	rack 1 to wall	island to island	wall to rack 1	rack 1 to location "To"	Cable tray to rack	Building to Building	Rack internal	Distance "intra" rackline	Distance "inter" rackline	Total Distance	Ratio intra/inter rackline
OPLR location to OPLR location	TargetBdgRacks	HEBT-020:14	281.0				66.0	2.9	9.1	3.0	200.0		15.0	266.0	281.0	0.06
(very similar to DLN location to DLN location)	HEBT-020:14	HBL-020:04	144	3.0	9.1	2.9	121.0	2.9	2.1	3.0			23.0	121.0	144.0	0.19
	HBL-020:04	MBL-070:04	38	3.0	2.1	2.9	22.0	2.9	2.1	3.0			16.0	22.0	38.0	0.73
	MBL-070:04	MBL-020:05	50	3.0	2.1	2.9	33.0	2.9	2.8	3.0			16.7	33.0	49.7	0.51
	MBL-020:05	SPK-020:05	50	3.0	2.8	2.9	33.0	2.9	2.8	3.0			17.4	33.0	50.4	0.53
	SPK-020:05	DTL-010:05	39	3.0	2.8	2.9	22.0	2.9	2.8	3.0			17.4	22.0	39.4	0.79
	DTL-010:05	FEB-020:07	89	3.0	2.8	2.9		2.9	4.2	3.0	70.0		18.8	70.0	88.8	0.27
	From	To	Total Distance [m]													
SCU location to DLN location	TargetBdgRacks	TargetBdgRacks	2									2.0	2.0		2.0	
	HEBT-020:14	HEBT-020:14	2									2.0	2.0		2.0	
	HBL-200:03	HBL-020:04	114	3.0	1.4	2.9	99.0	2.9	2.1	3.0			15.3	99.0	114.3	0.15
	HBL-180:04	HBL-020:04	104	3.0	2.1	2.9	88.0	2.9	2.1	3.0			16.0	88.0	104.0	0.18
	HBL-160:04	HBL-020:04	93	3.0	2.1	2.9	77.0	2.9	2.1	3.0			16.0	77.0	93.0	0.21
	HBL-140:04	HBL-020:04	82	3.0	2.1	2.9	66.0	2.9	2.1	3.0			16.0	66.0	82.0	0.24
	HBL-120:04	HBL-020:04	71	3.0	2.1	2.9	55.0	2.9	2.1	3.0			16.0	55.0	71.0	0.29
	HBL-100:04	HBL-020:04	60	3.0	2.1	2.9	44.0	2.9	2.1	3.0			16.0	44.0	60.0	0.36
	HBL-080:04	HBL-020:04	49	3.0	2.1	2.9	33.0	2.9	2.1	3.0			16.0	33.0	49.0	0.48
	HBL-060:04	HBL-020:04	38	3.0	2.1	2.9	22.0	2.9	2.1	3.0			16.0	22.0	38.0	0.73
	HBL-040:04	HBL-020:04	27	3.0	2.1	2.9	11.0	2.9	2.1	3.0			16.0	11.0	27.0	1.45
	HBL-020:04	HBL-020:04	2									2.0	2.0		2.0	
	HBL-010:04	HBL-020:04	27	3.0	2.1	2.9	11.0	2.9	2.1	3.0			16.0	11.0	27.0	1.45
	MBL-090:04	MBL-020:05	60	3.0	2.1	2.9	44.0	2.9	2.1	3.0			16.0	44.0	60.0	0.36
	MBL-070:04	MBL-020:05	49	3.0	2.1	2.9	33.0	2.9	2.1	3.0			16.0	33.0	49.0	0.48
	MBL-050:04	MBL-020:05	38	3.0	2.1	2.9	22.0	2.9	2.1	3.0			16.0	22.0	38.0	0.73
	MBL-030:04	MBL-020:05	27	3.0	2.1	2.9	11.0	2.9	2.1	3.0			16.0	11.0	27.0	1.45
	MBL-020:04	MBL-020:05	2									2.0	2.0		2.0	
	SPK-060:03	SPK-020:05	38	3.0	1.4	2.9	22.0	2.9	2.8	3.0			16.0	22.0	38.0	0.73
	SPK-040:05	SPK-020:05	28	3.0	2.8	2.9	11.0	2.9	2.8	3.0			17.4	11.0	28.4	1.58
	SPK-020:05	SPK-020:05	2									2.0	2.0		2.0	
	DTL-030:10	DTL-010:05	32	3.0	6.3	2.9	11.0	2.9	2.8	3.0			20.9	11.0	31.9	1.90
	DTL-010:10	DTL-010:05	2									2.0	2.0		2.0	
	FEB-020:07	FEB-020:07	2									2.0	2.0		2.0	

Parameter	Value
Distance rack to cable tray [m]	3.0
Distance between wall and first rack [m	2.9
Distance between adjacent racks [m]	0.7
Distance between rack islands [m]	11.0

We assume the same parameters for the FEB

Figure 37: Distances assumed for the latency evaluation.

Appendix

6 List of Figures

7 List of Tables