Zurich University
of Applied Sciences

School of
Engineering

IAMP Institute of Applied
Mathematics and Physics

FBIS Architectural Design Options

14.08.2017

Agenda

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  - Decision Logic Node
  - Special Considerations
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  - Decision Logic Node
  - SLink
  - Optical Protection Line
  - Hardware Interrupt Line
  - Mezzanine Cards
- Architectural Layout for ESS
  - Along the Klystron Gallery
  - Front-End Building
- Latency Evaluation

Slide deck is not self-explaining.
Please read respective documents!

Architectural Design Proposal

Basic Structure – Architectural Building Blocks

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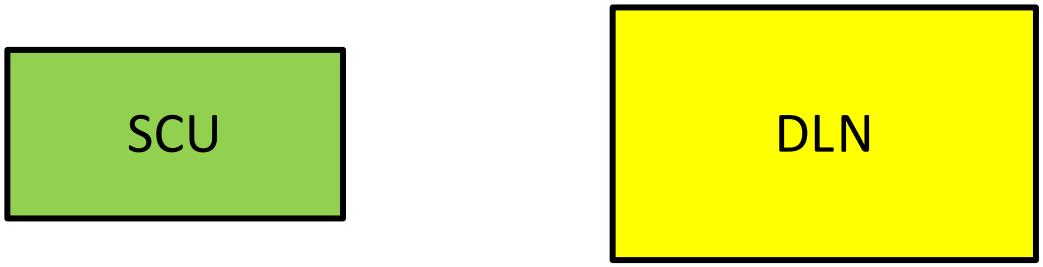
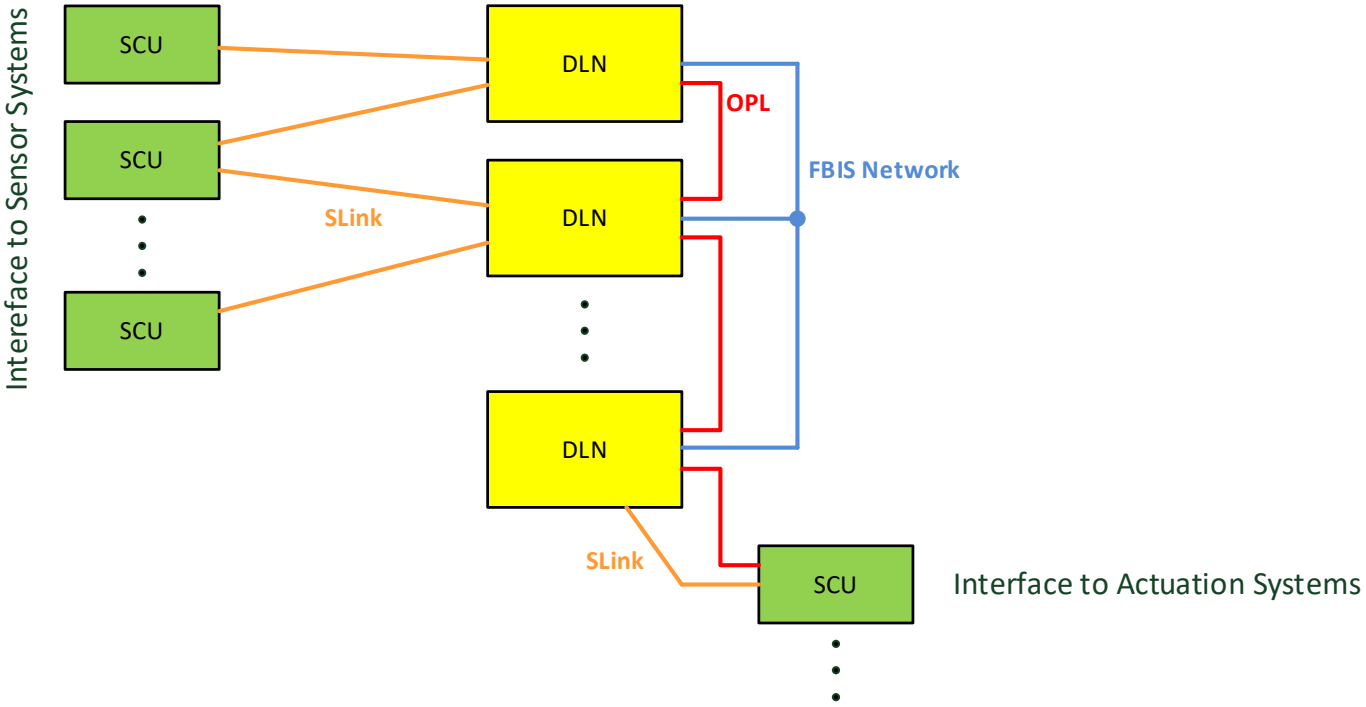
Two basic architectural elements:

- Decision Logic Node (DLN)
  - Calculate protection logic
  - Interface with Higher-Level Safety, Control System and Timing System
- Signal Conversion Unit (SCU)
  - Interface with Sensor Systems
  - Interface with Actuation Systems



Basic Structure – Interfaces

- SLink realizes interface between SCU and DLN
- Optical Protection Line for requesting beam switch-off
- FBIS Network



SCU – Concept and Interfaces
(when used to interface with Sensor Systems)

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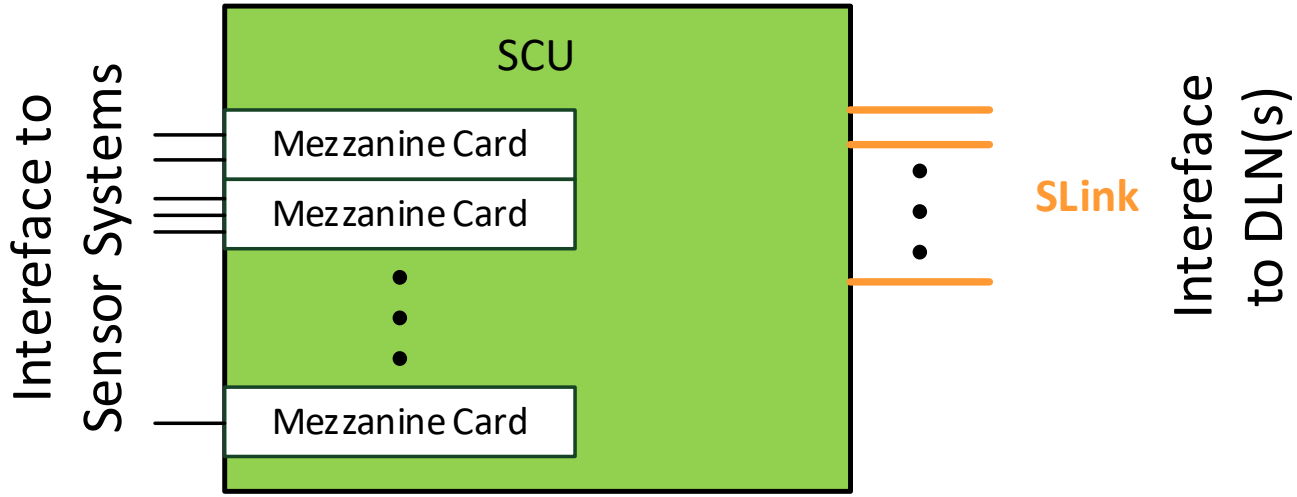
- One SCU may interface with multiple diverse Sensor Systems
- Actual interface realized on Mezzanine Cards
- Serves as «local concentrator»
- SLink interface to DLN(s)



SCU – Functional Behavior
(when used to interface with Sensor Systems)

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- Sample discrete input signals
- Sample data link inputs and decode data
- Detect failures with respect to the discrete and data link inputs
- Serialize input data and send it via the Slink

Additionally:

- Perform self-diagnostic tests
- Verify SCU hardware configuration
- Provide read/write acces to status and control registers

SCU – Architectural Application Options
(when used to interface with Sensor Systems)

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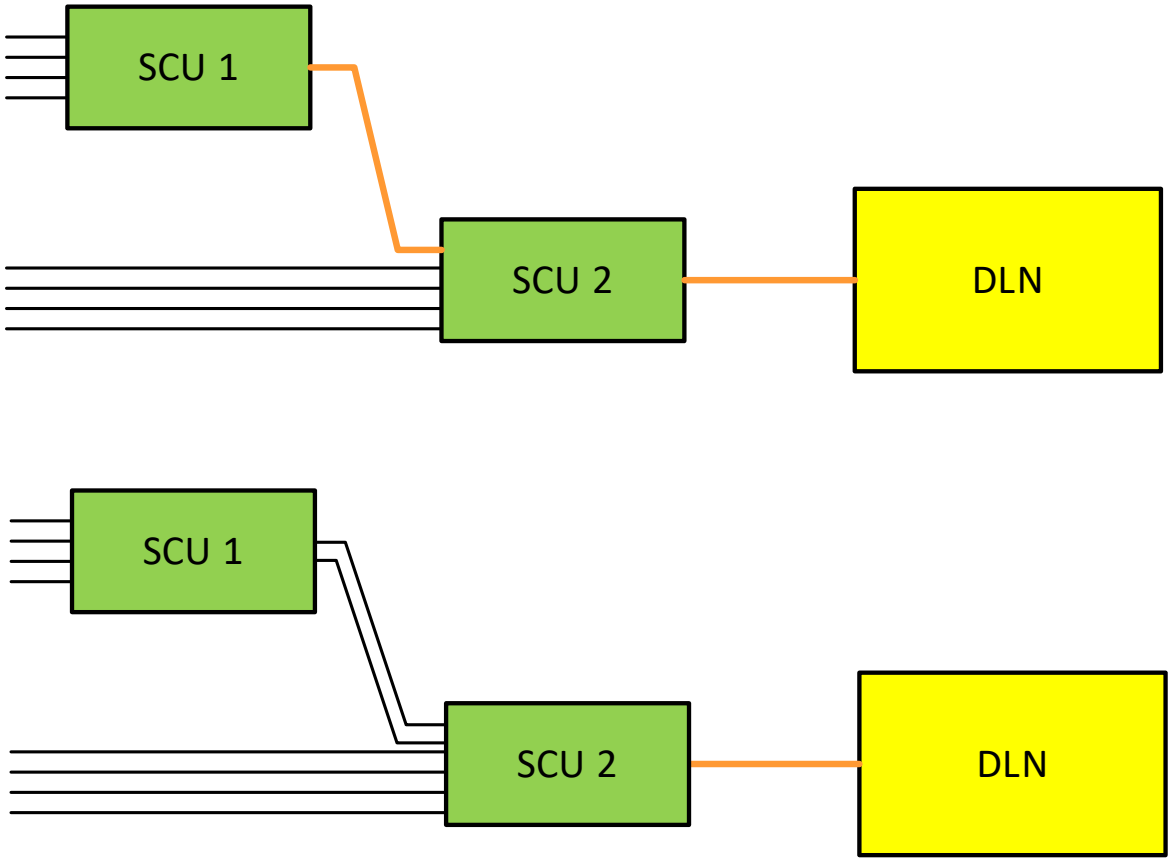
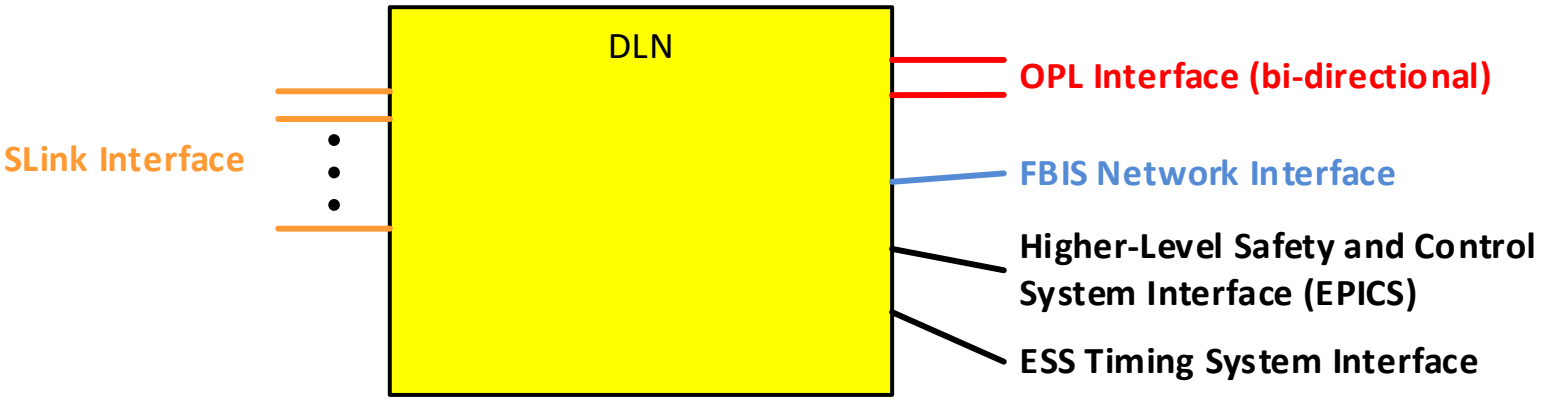


DLN – Concept and Interfaces

- Σ DLN ≙ FBIS Decision Logic
- Single DLN processes «local part» of FBIS Decision Logic
- Compute Local Beam Permit
- Force Global Beam Permit to NOK to request switch-off
- Provide SLink interfaces
- Interface with Higher-Level Safety, Control Systems, TS
- Interface with OPL and FBIS Network



DLN – Functional Behavior

Basic Functionalities:

- Deserialize SLink datastream
- Provide Latching and Masking features
- Provide Diagnostic Information
- Logging

Compute FBIS Logic:

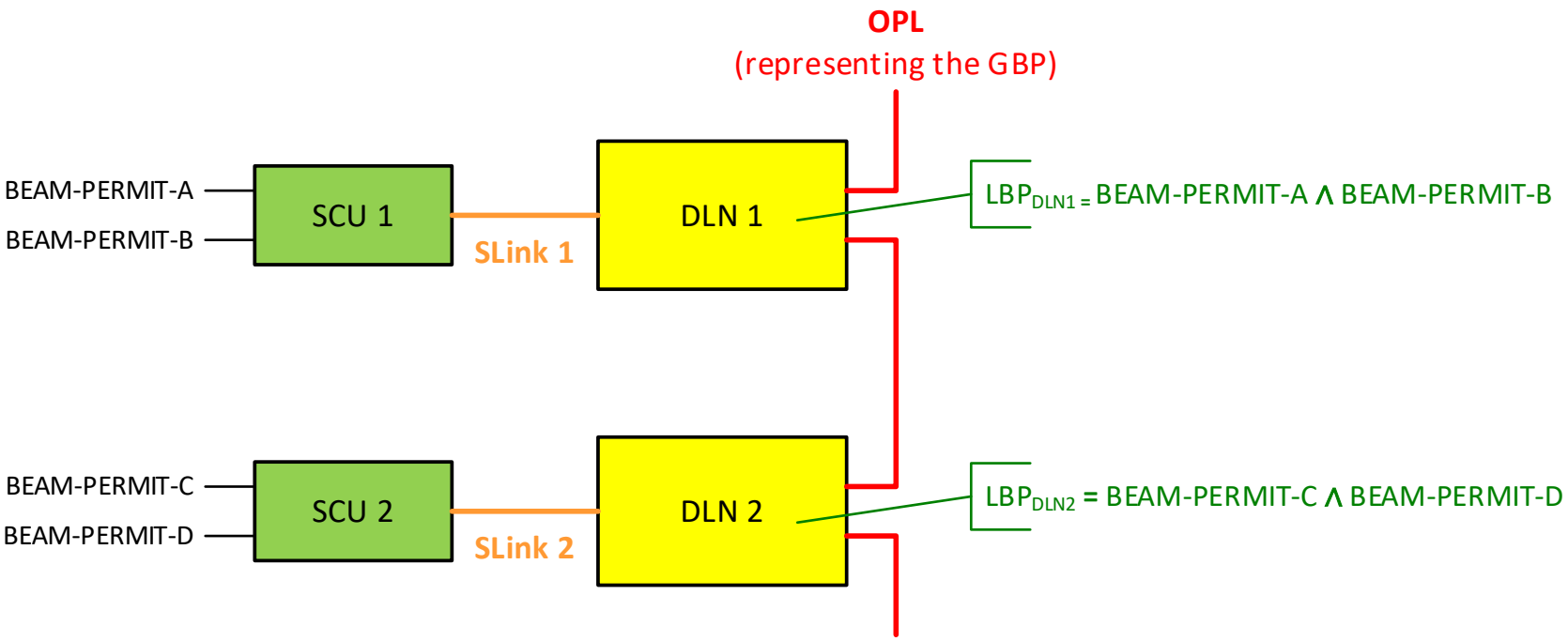
- State Evaluation
- Compute Local Beam Permit (+ Broadcast it)
- Control Global Beam Permit
- Compute «Enforced Modes»
- Verify mode Consistency among DLNs

DLN – Functional Behavior

Additionally:

- Perform self-diagnostic tests
- Verify the SCUs are operational and functioning correctly
- Perform SCU diagnostic checks:
- OPL Integrity Check:
- Software Beam Permit:
- Inform ESS TS about Latched Local Beam Permits

DLN – Logic Example: Simple OR



DLN – Logic Example: 2oo3

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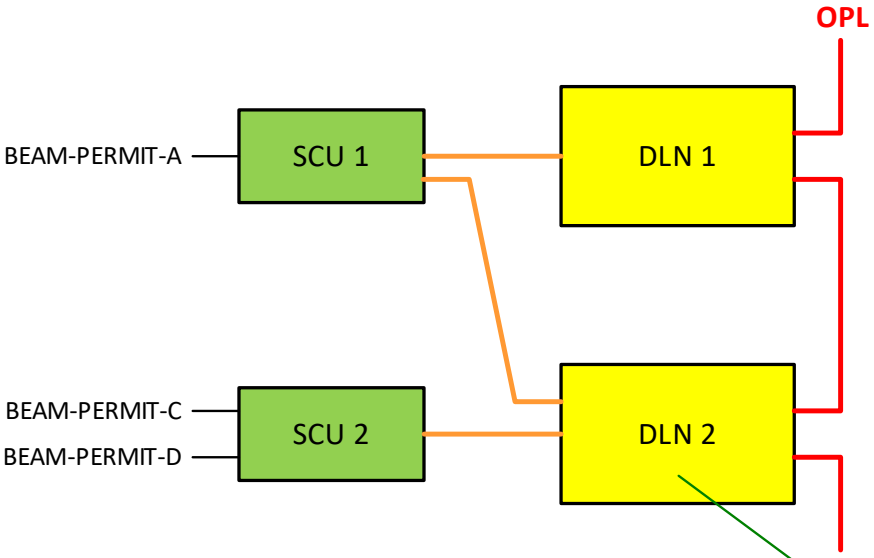

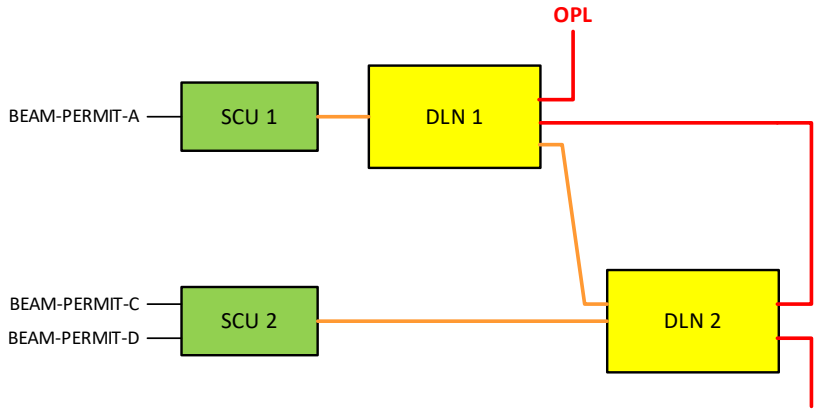

LBP = 2oo3(BEAM-PERMIT-A; BEAM-PERMIT-C; BEAM-PERMIT D)

DLNs and SCUs Interfacing with Actuation Systems

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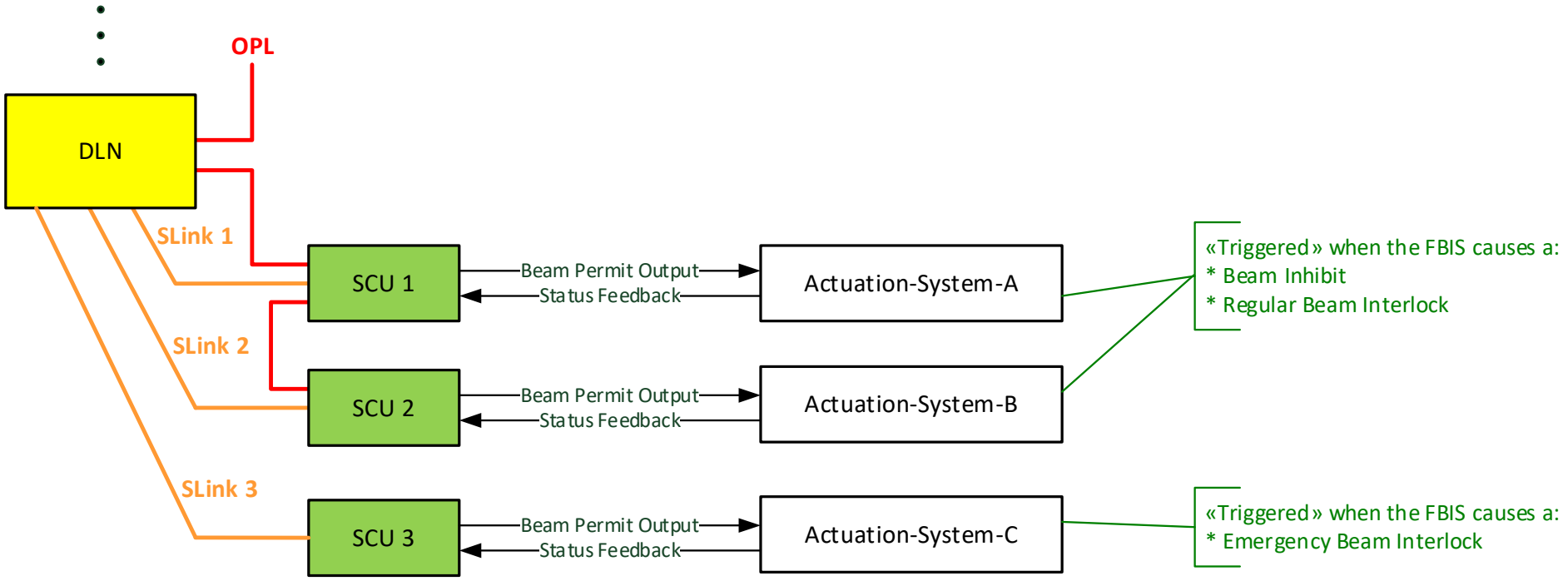

MP-related Systems Directly Interfacing with the Optical Protection Line

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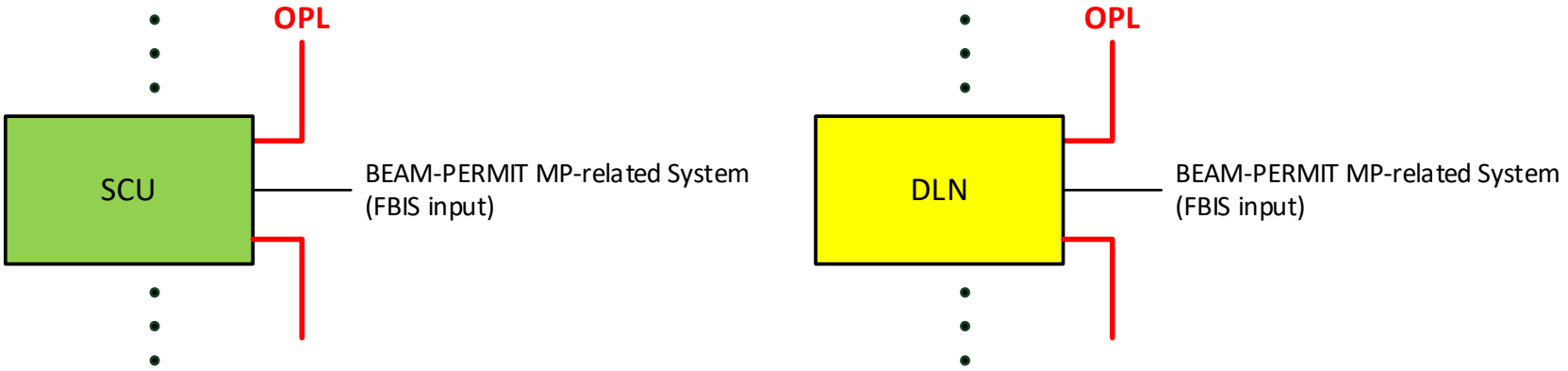

Realization Idea

SCU – Breakdown Structure

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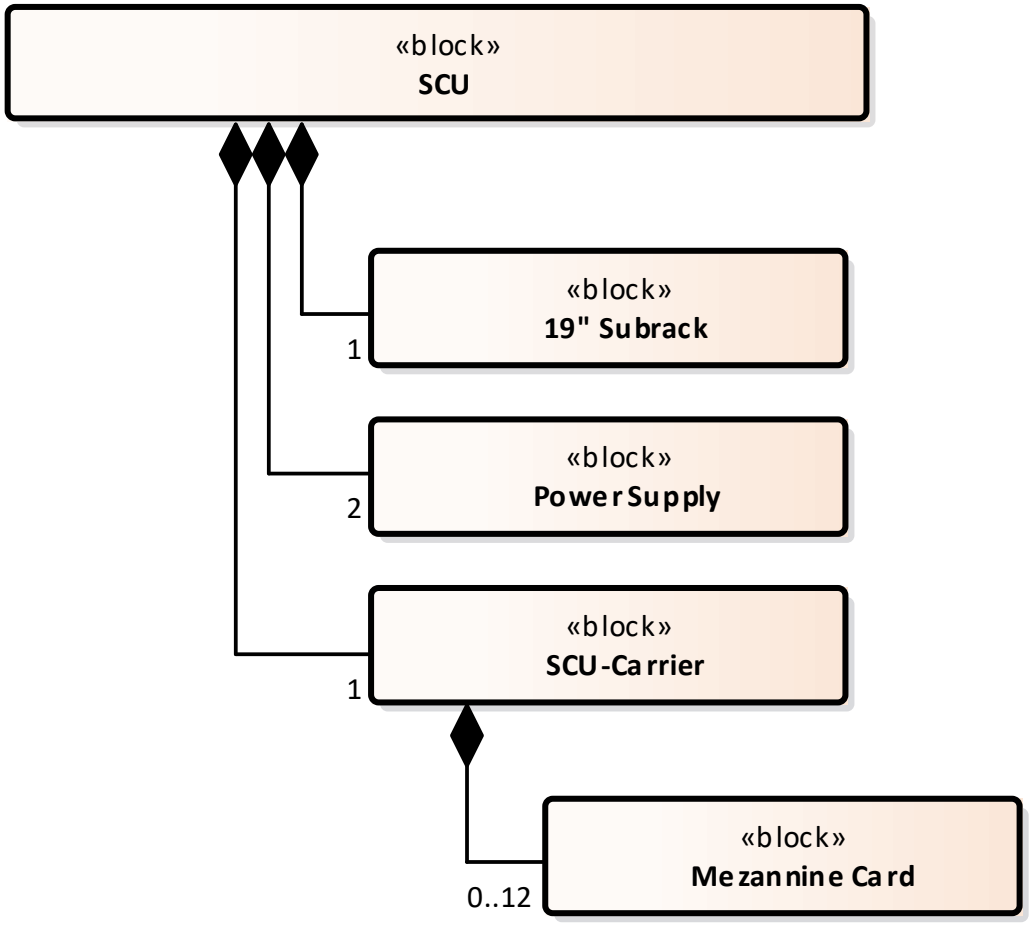

SCU – 19” Subrack and Redundant Power Supply

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SCU – Carrier

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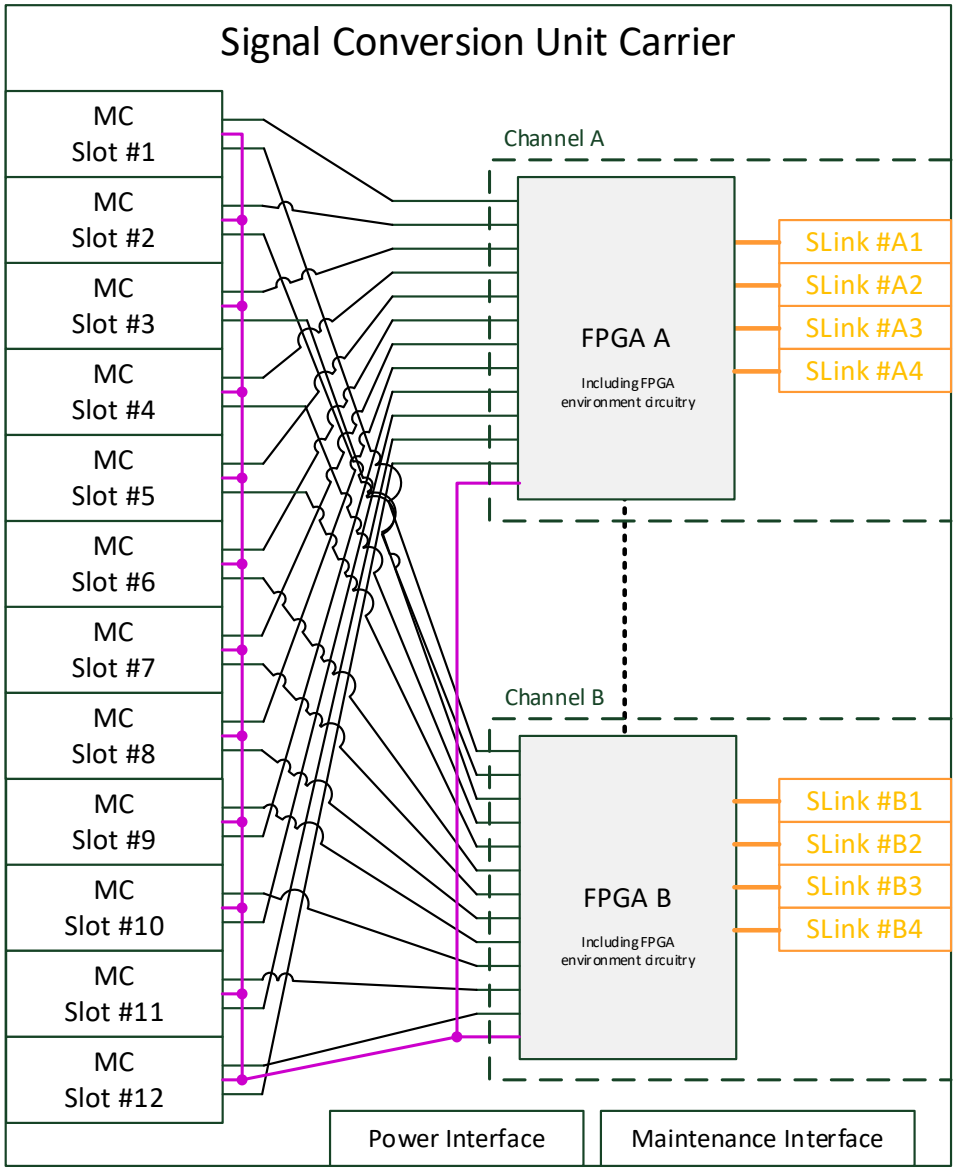

DLN – Breakdown Structure

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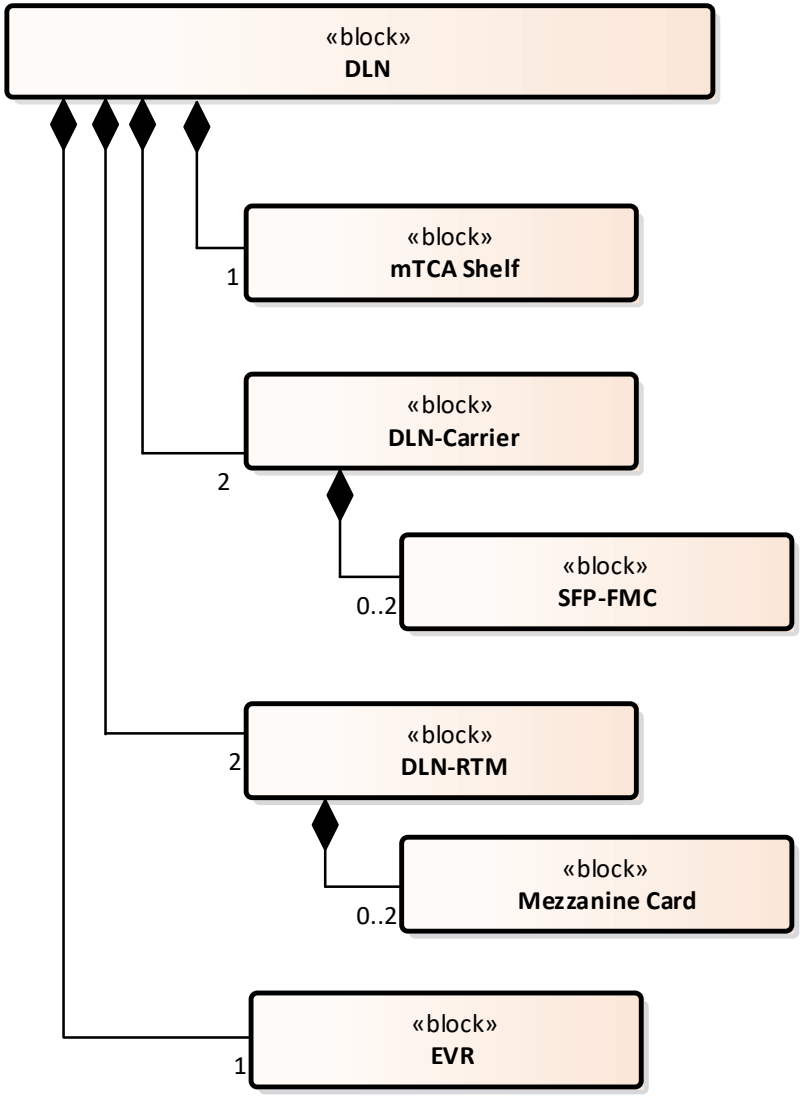

DLN – mTCA Shelf, DLN-Carrier and EVR

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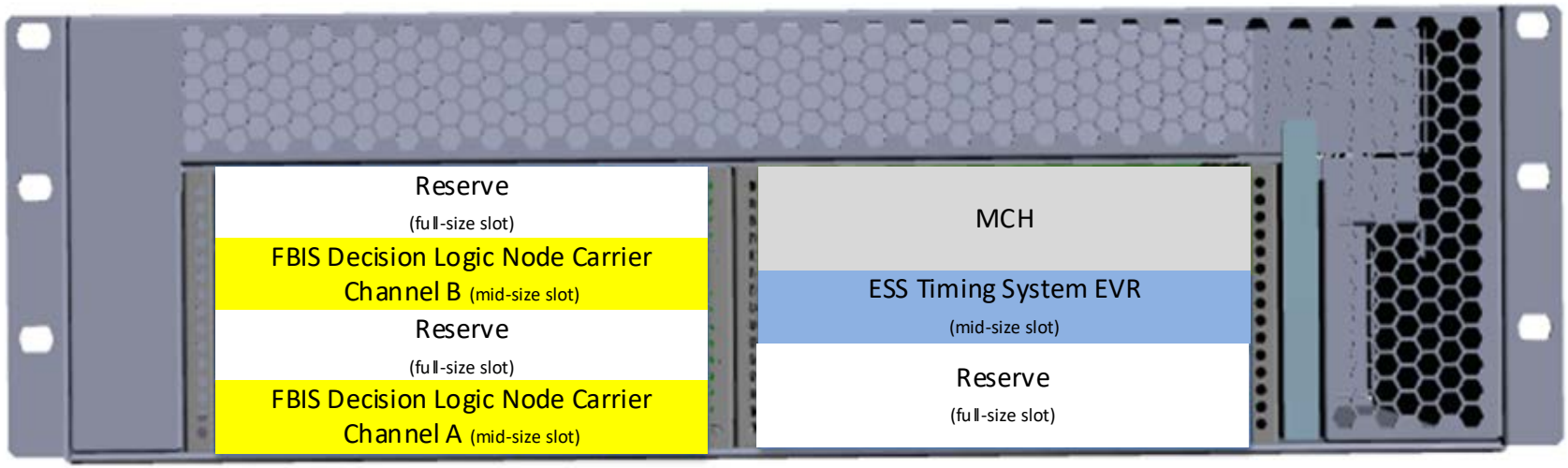

DLN – Carrier and RTM

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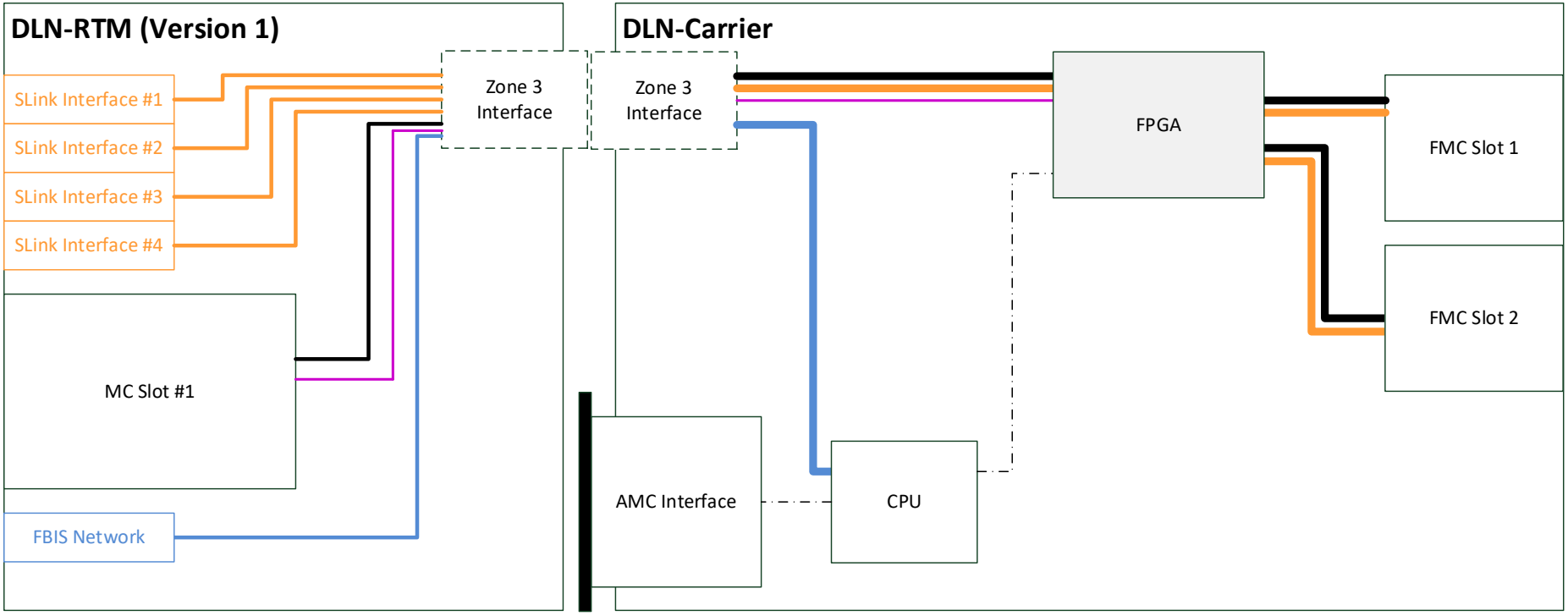

DLN – Carrier and RTM (with 2 MC Slots)

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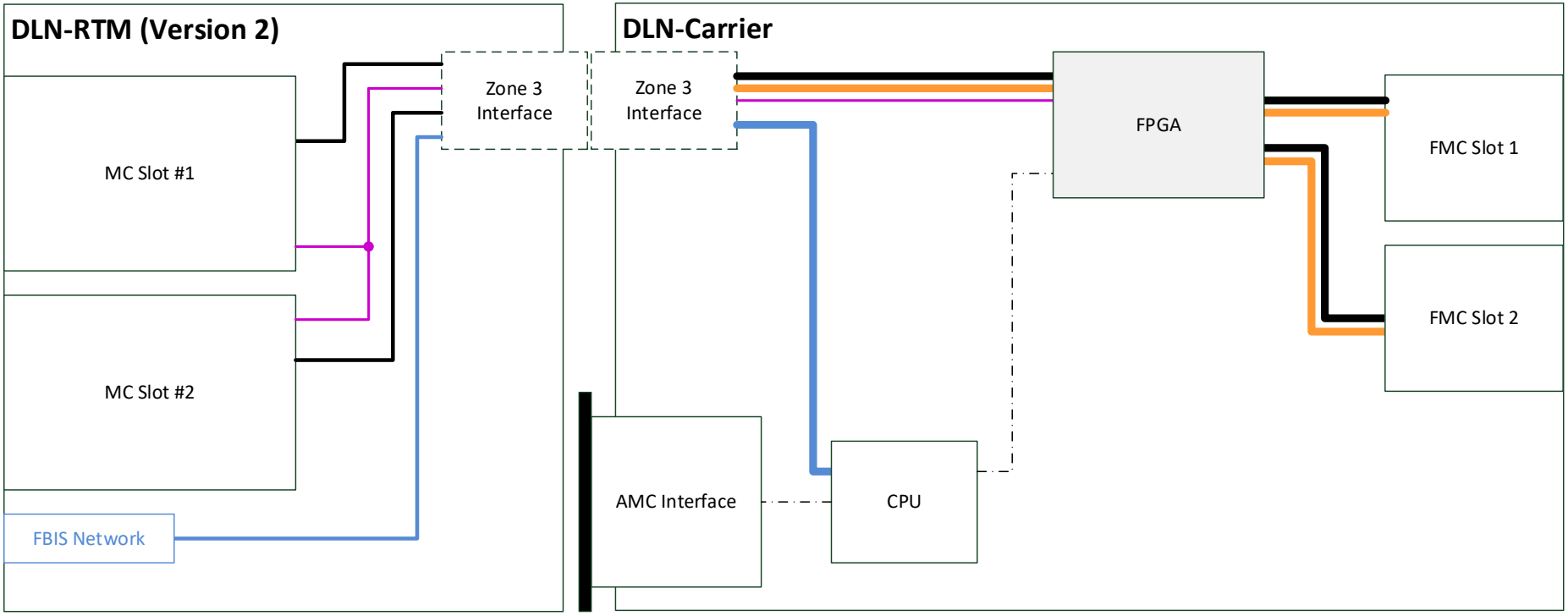
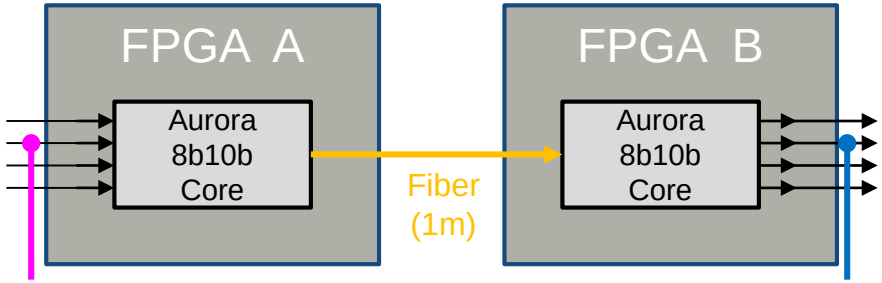
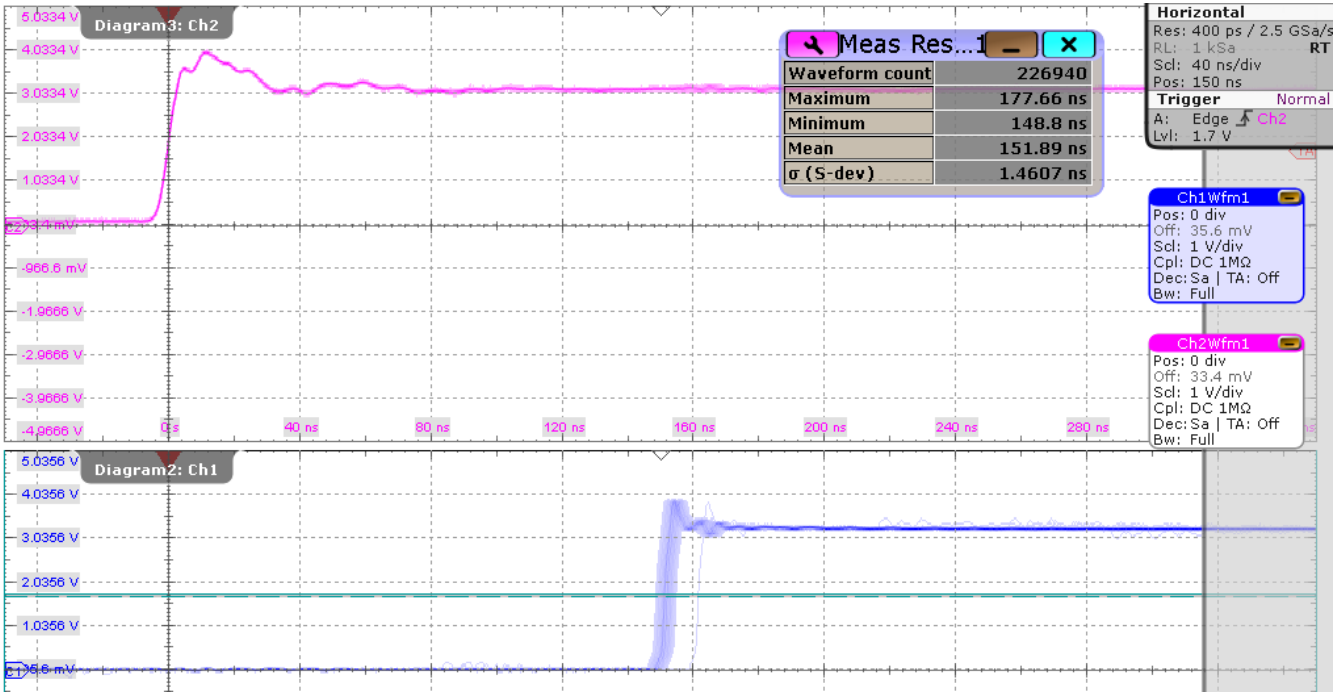
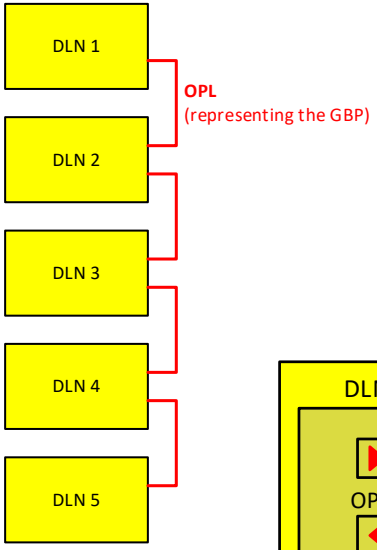


SLink Interface

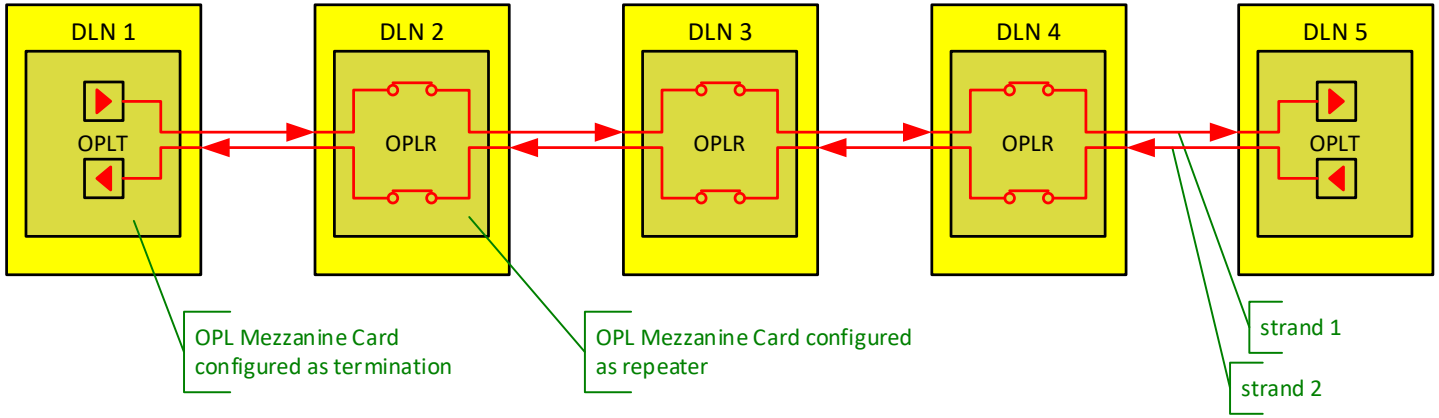




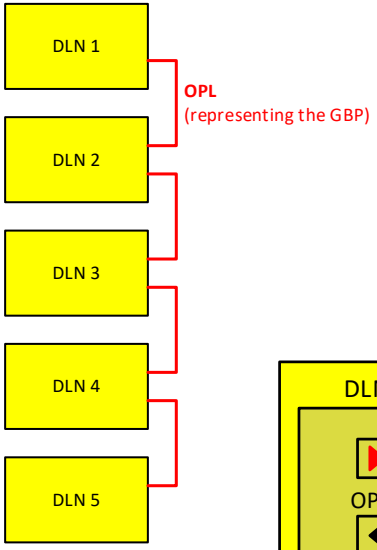
Optical Protection Line



Global Beam Permit states:
OK = square waveform
NOK = no light



Optical Protection Line



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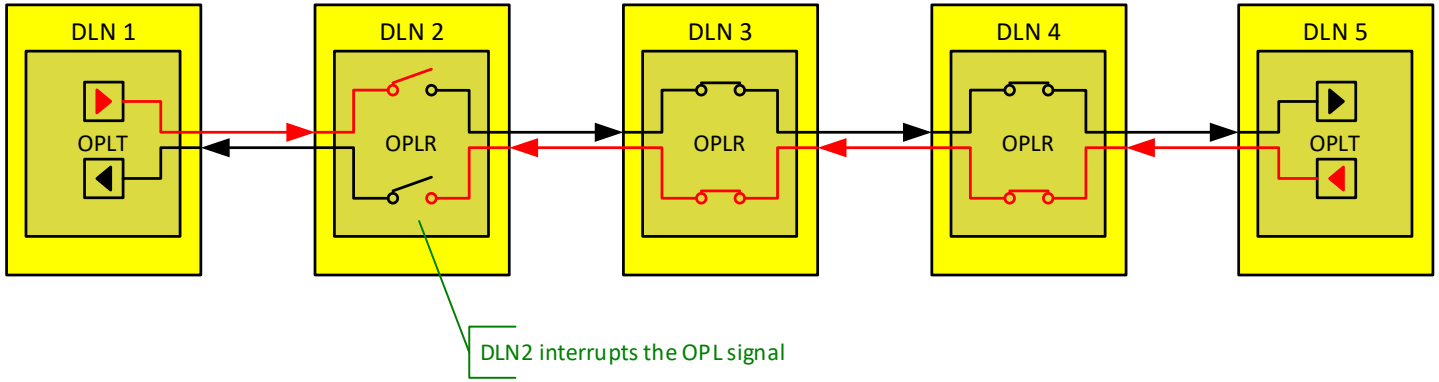
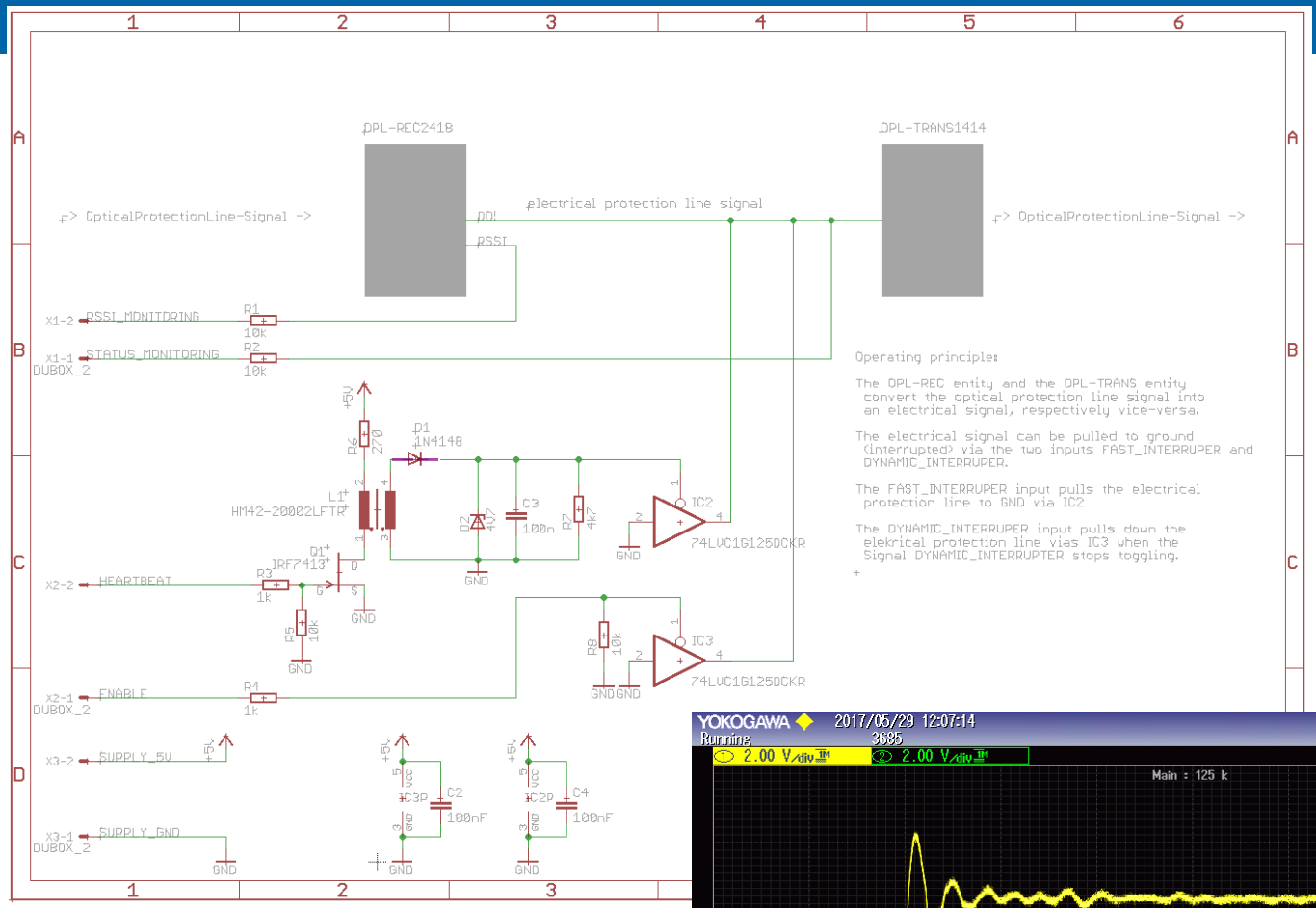
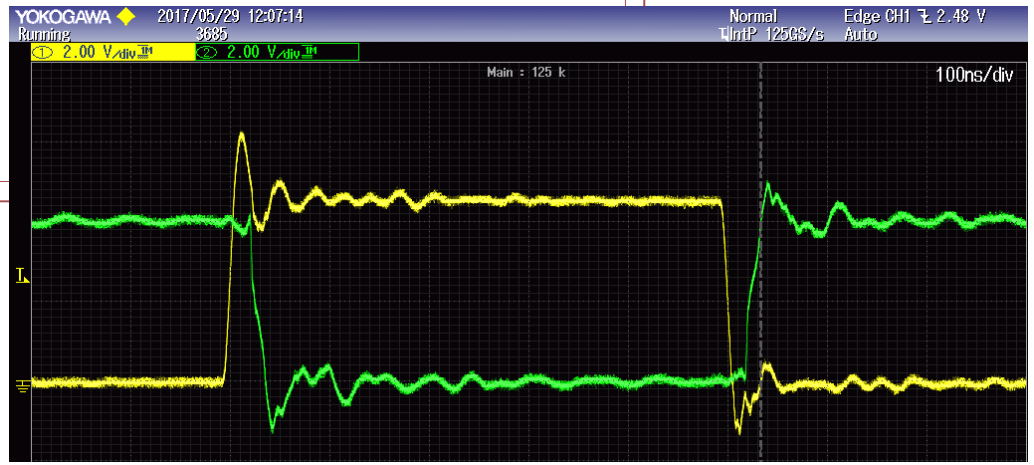
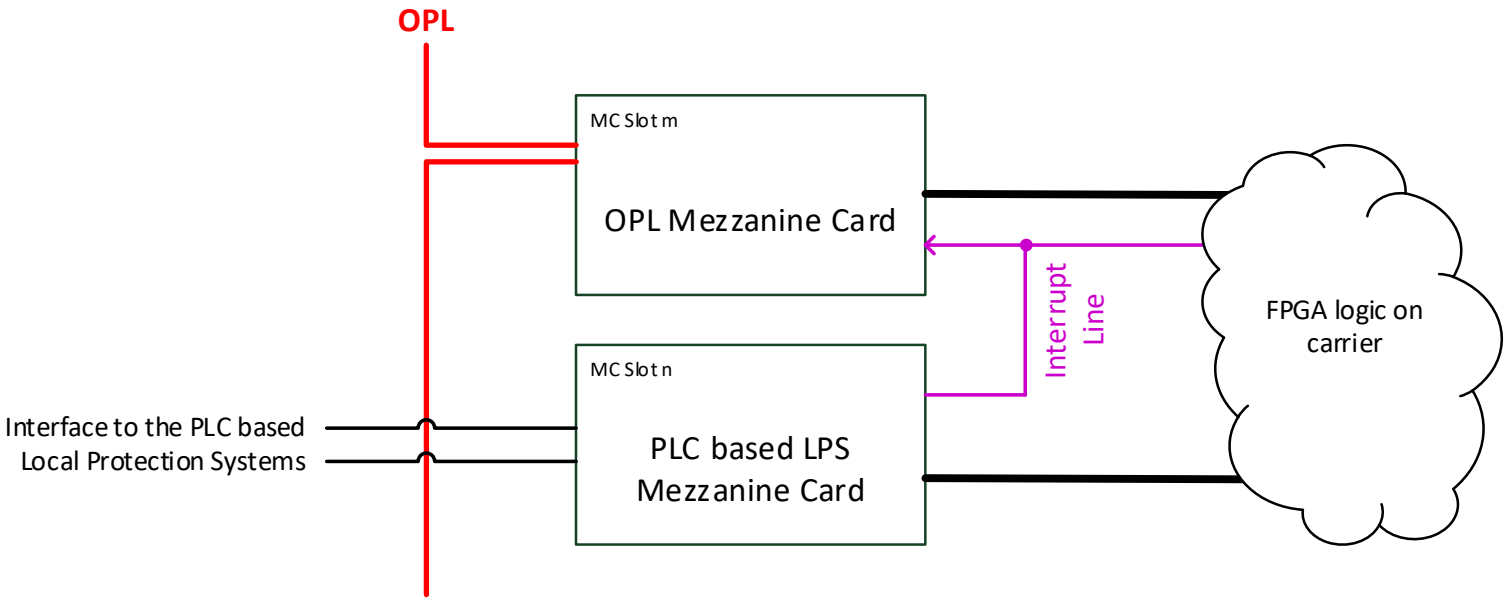


OPL – Proof of Concept

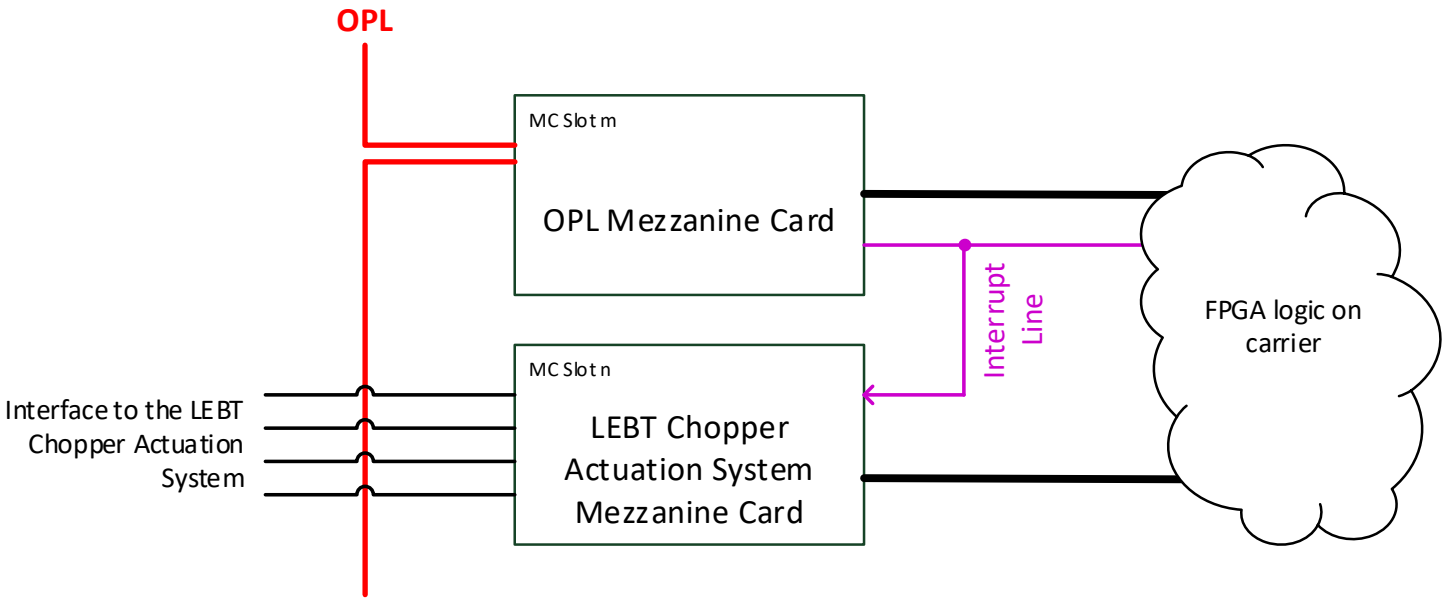




Hardware Interrupt Line



Hardware Interrupt Line



MC – Signalling Patterns

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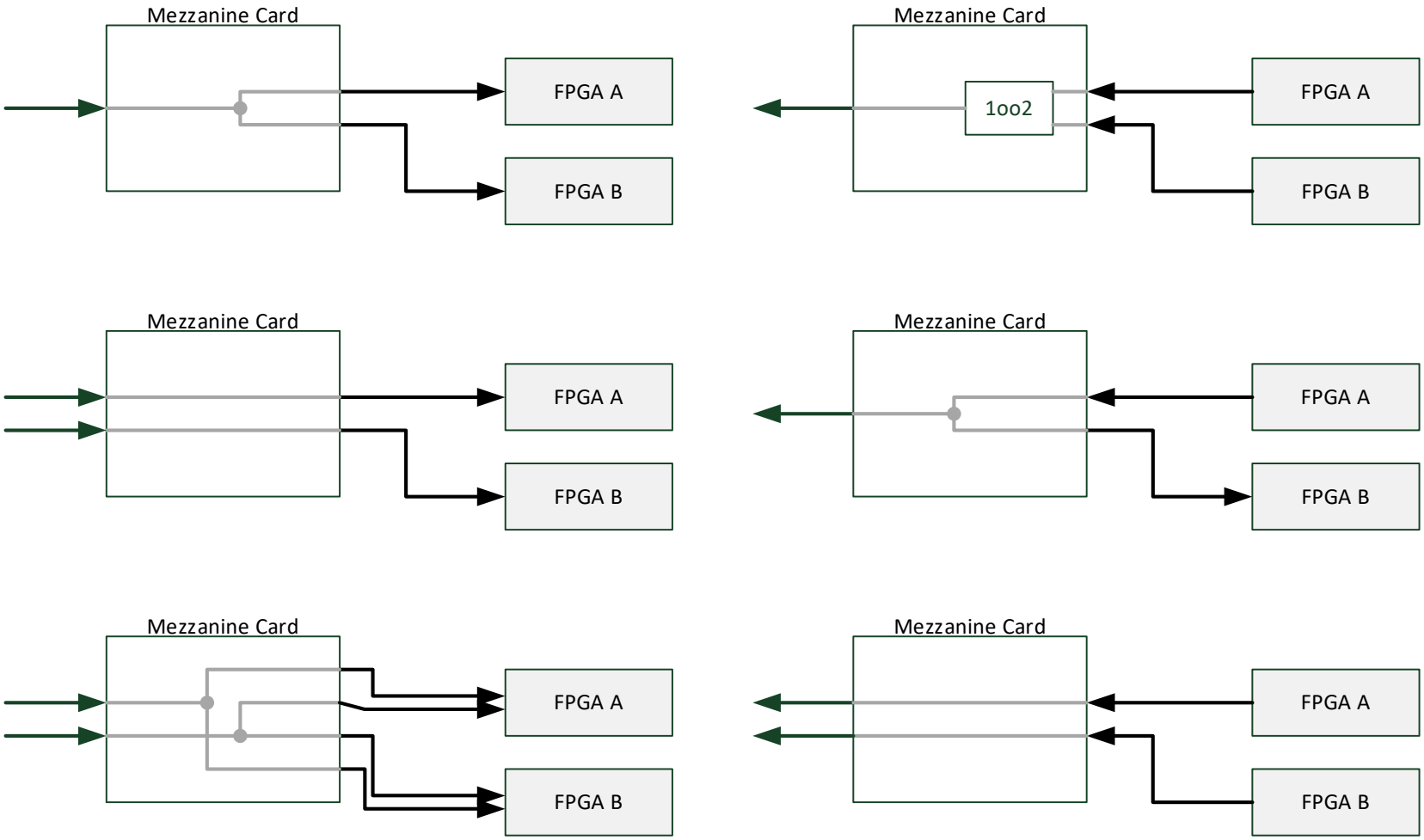

OPL Mezzanine Card
(When used as Repeater)

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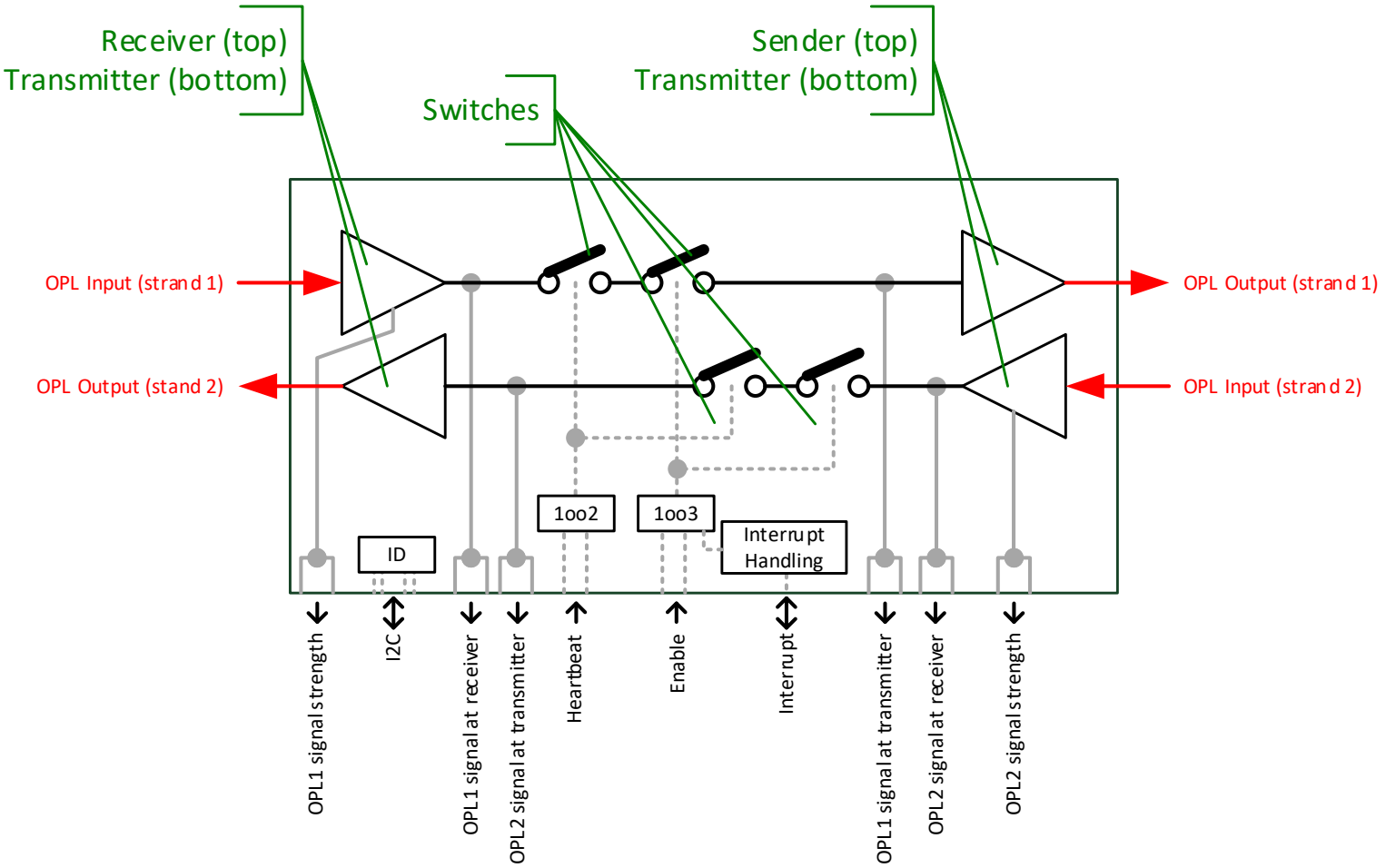

OPL Mezzanine Card
(When used as Termination)

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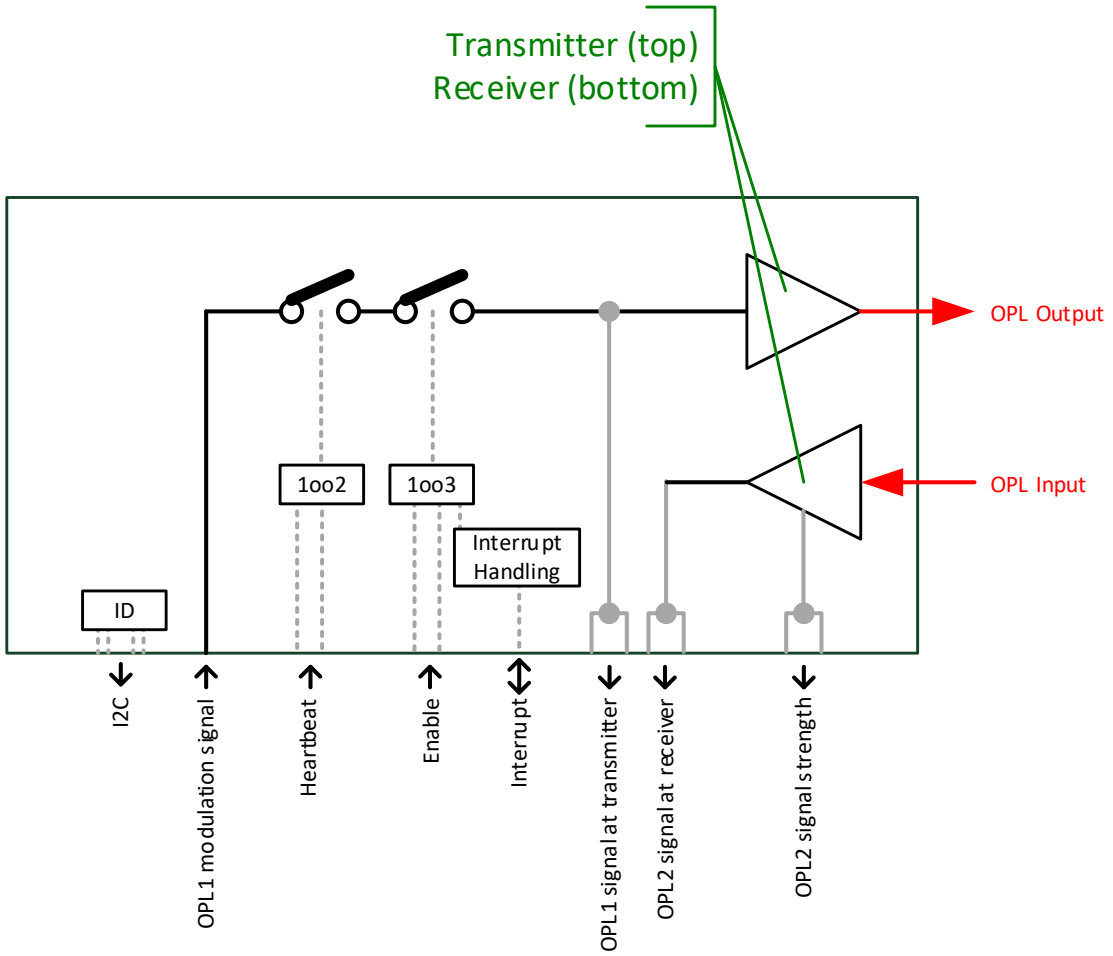
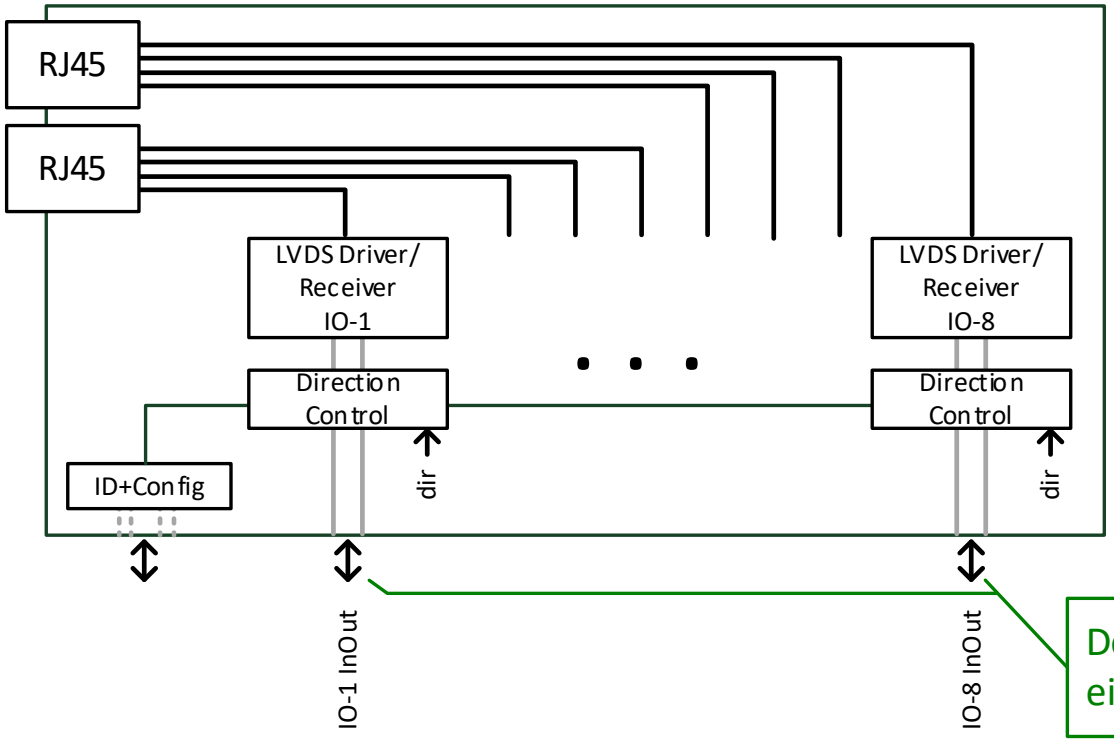
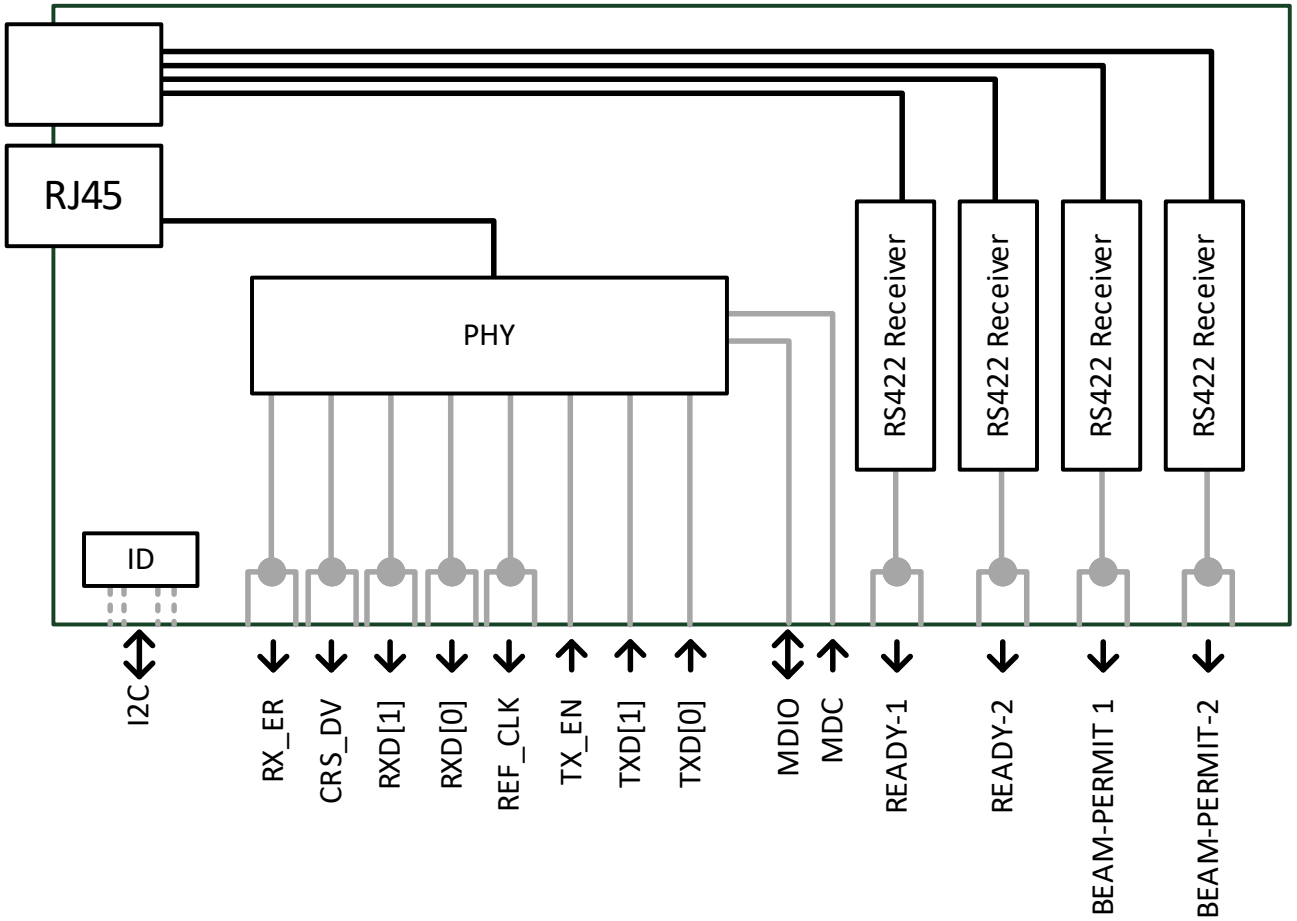


LVDS Mezzanine Card



RS422 + Ethernet Mezzanine Card



Carrier Pin Assignment

	OPL repeater configuration		OPL termination configuration		Channe	
	Signal	Direction[1)]	Signal	Direction[1)]	A	B
1	OPL1 signal strength	Out	-	-	X	X
2	OPL1 signal at receiver	Out	OPL1 modulation signal	-	X	X
3	OPL1 signal at receiver	Out	OPL1 modulation signal [2)]	-	X	X
4	OPL1 signal at transmitter	Out	OPL1 signal at transmitter	Out	X	X
5	Enable	In	Enable	In	X	X
6	Heartbeat	In	Heartbeat	In	X	X
7	OPL2 signal strength	Out	OPL2 signal strength	Out	X	X
8	OPL2 signal at receiver	Out	OPL2 signal at receiver	Out	X	X
9	OPL2 signal at transmitter	Out	-	-	X	X
10	SCL (I2C) [3)]	In	SCL (I2C) [3)]	Input	X	X
11	SDA (I2C) [3)]	InOut	SDA (I2C) [3)]	InOut	X	X
12	Interrupt [3)]	InOut	Interrupt [3)]	InOut	X	X
13	VCC (power supply) [3)]	-	VCC (power supply) [3)]	-	-	-
14	GND (power supply) [3)]	-	GND (power supply) [3)]	-	-	-

1) Directions as seen from MC

2) Only one of the Channels may actively drive the signal. Using a 1oo2 pattern to drive the signal would be possible when the OPL signal is a DC-signal or when the OPL signal is a square waveform and it could be ensured that Channel A and B are in sync

3) Identical for all Mezzanine Cards

Architectural Layout for ESS

Along the Klystron Gallery

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- One DLN for every Beam Line Section
- Installation in the rack closest to FEB
- One SCU per Rack Island
- MC and local patch kabels to Sensor Systems
- Redundant SLink to DLN

Along the Klystron Gallery

Simplified view. Does not show redundancy

Along the Klystron Gallery

Along the Klystron Gallery – Close-Up

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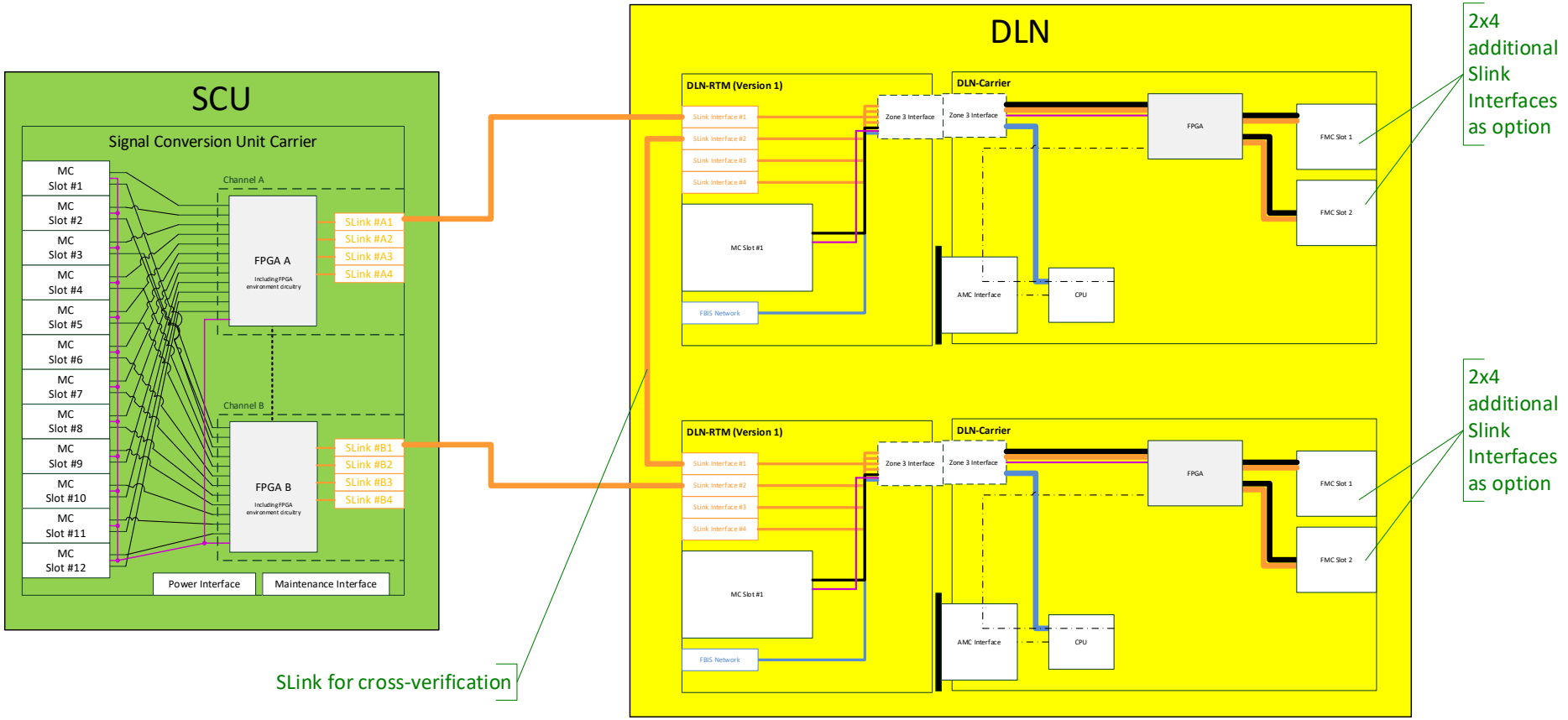

Front-End Building

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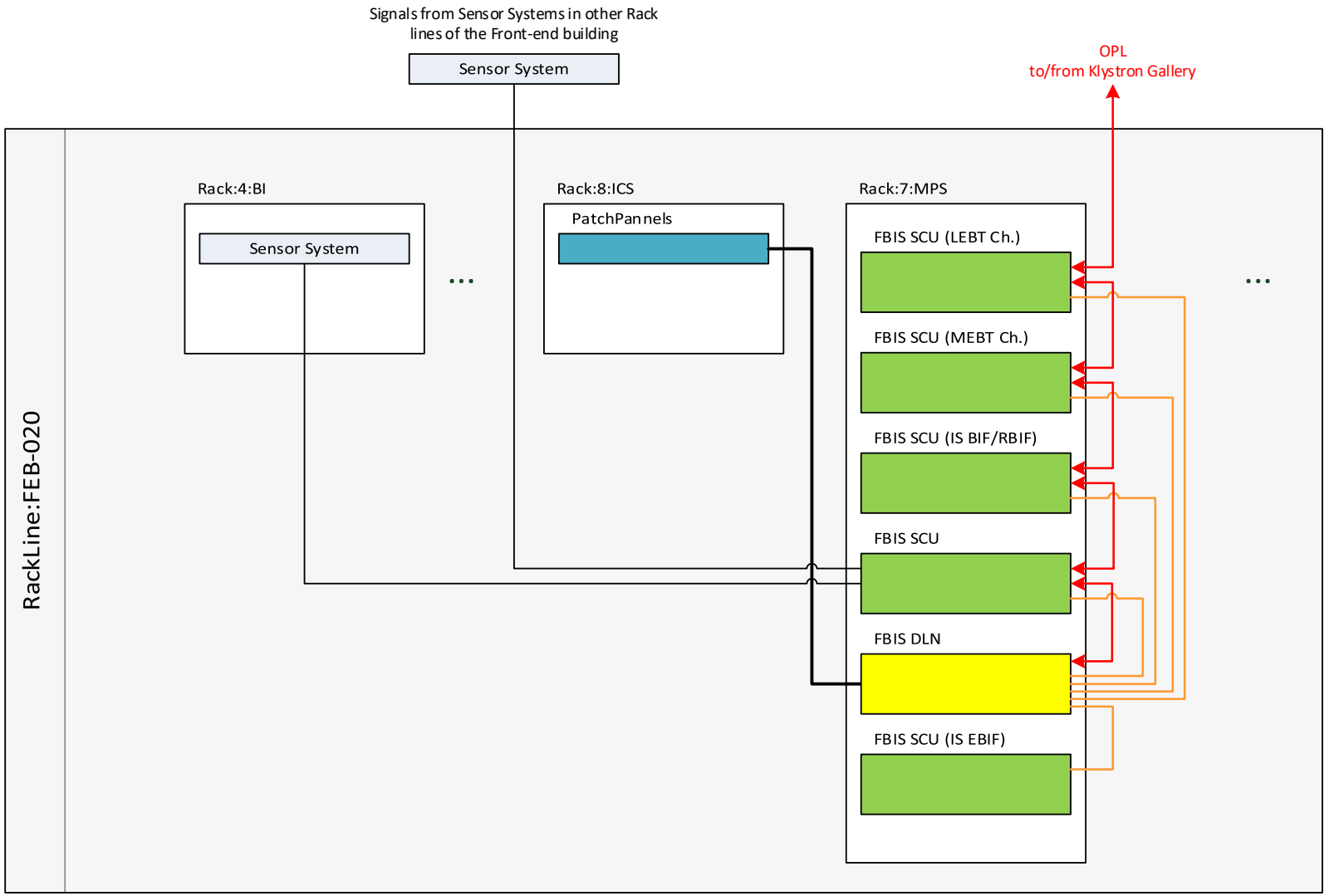
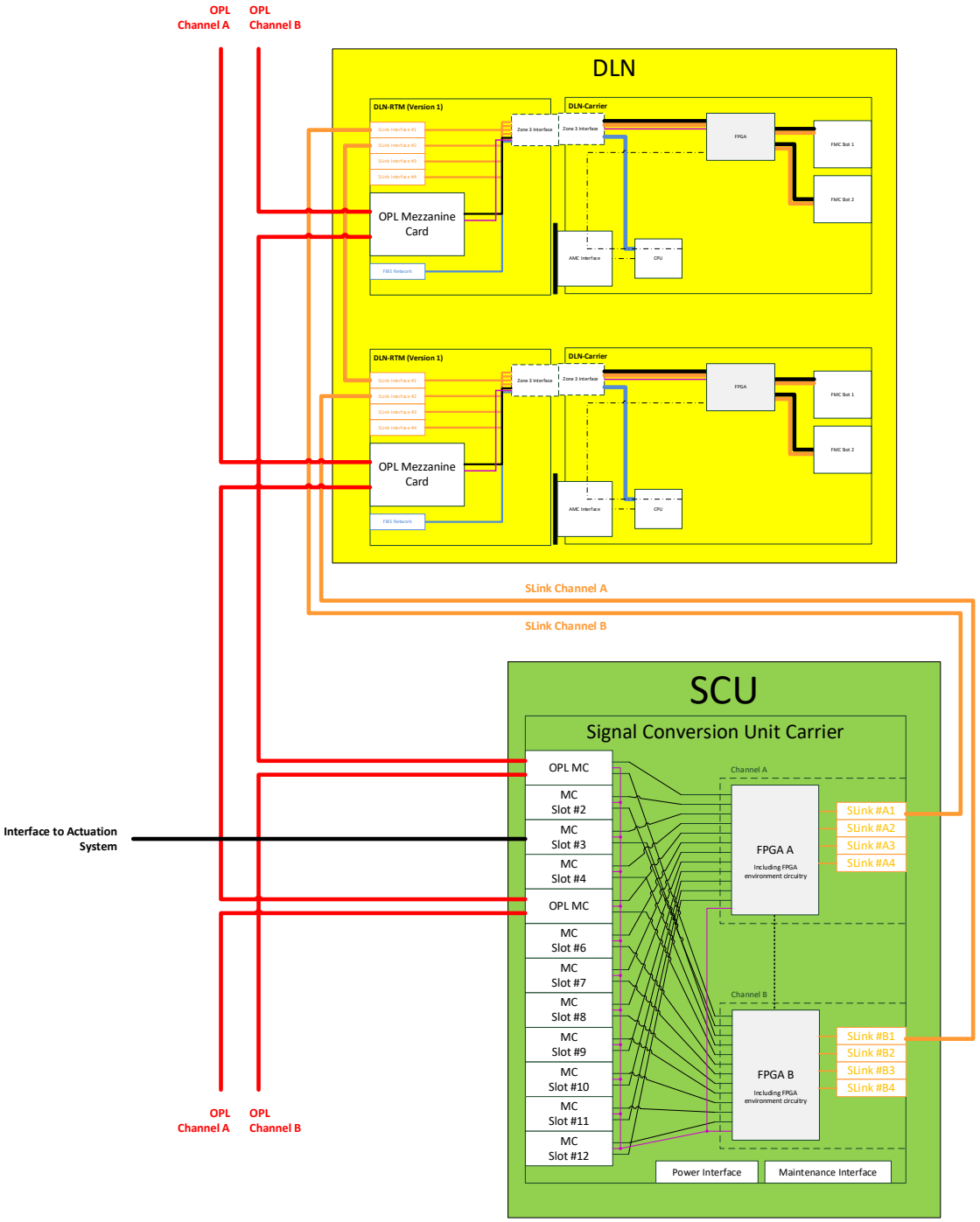
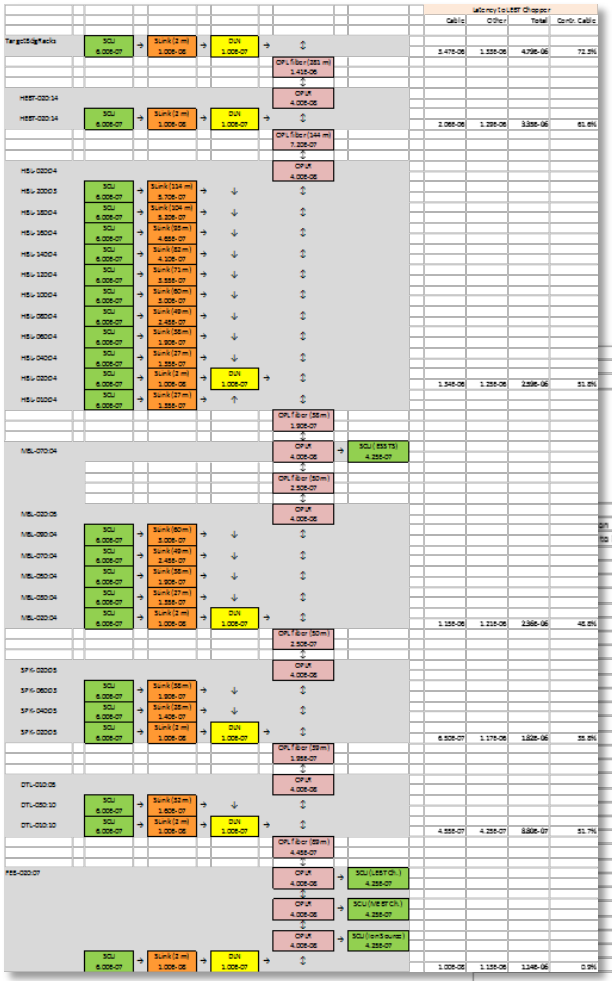
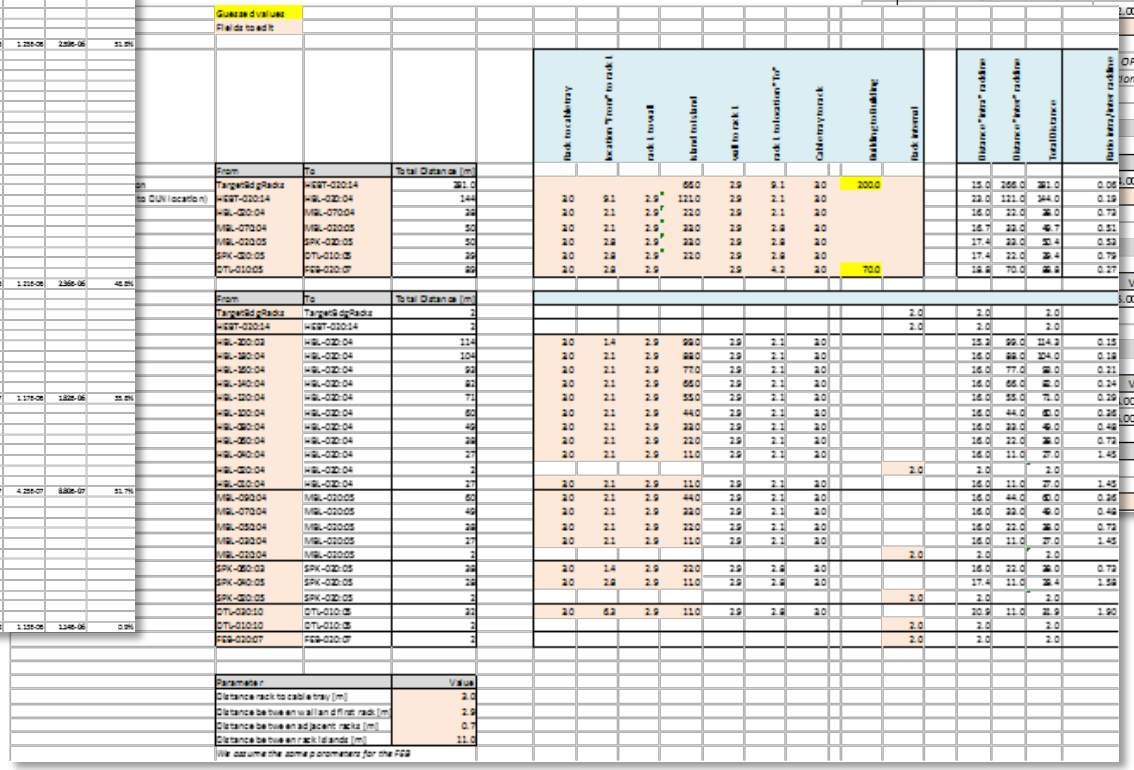



OPL Channel A
OPL Channel B
DLN
DLN-RTM (Version 1)
DLN-Carrier
OPL Mezzanine Card
FPGA
FMC Slot 1
FMC Slot 2
AMC Interface
CPU
SLink Channel A
SLink Channel B
SCU
Signal Conversion Unit Carrier
Interface to Actuation System
OPL MC
MC Slot #2
MC Slot #3
MC Slot #4
OPL MC
MC Slot #6
MC Slot #7
MC Slot #8
MC Slot #9
MC Slot #10
MC Slot #11
MC Slot #12
Channel A
FPGA A
Including FPGA environment circuitry
SLink #A1
SLink #A2
SLink #A3
SLink #A4
Channel B
FPGA B
Including FPGA environment circuitry
SLink #B1
SLink #B2
SLink #B3
SLink #B4
Power Interface
Maintenance Interface

Latency Evaluation

Latency Evaluation





SCU (used to Interface Sensor Systems)

Parameter	Value
FPGA Clock [Hz]	4.00E+08

Action		Latency [s]
Input processing [Clock Cycles]	40	1.00E-07
SLink Latency [s]	5.00E-07	5.00E-07
Total		6.00E-07

DLN

Parameter	Value
FPGA Clock [Hz]	4.00E+08

Action		Latency [s]
Input processing [Clock Cycles]	40	1.00E-07
		2.00E-08
		1.00E-07

OPL line is assigned to the DLN. ion does not need to be explicitly

	Latency [s]
1.00E-08	4.00E-08
	4.00E-08

	Value
	3.00E-09

	Value
	1.00E+08
	2.00E+06

	Latency [s]
2	4.00E-07
10	2.50E-08
	4.25E-07

Parameter	Value
Distance rack to cable tray [m]	2.0
Distance between cable and first rack [m]	2.9
Distance between adjacent racks [m]	0.7
Distance between rack islands [m]	11.0

We assume the same parameters for the FBIS

Latency Evaluation

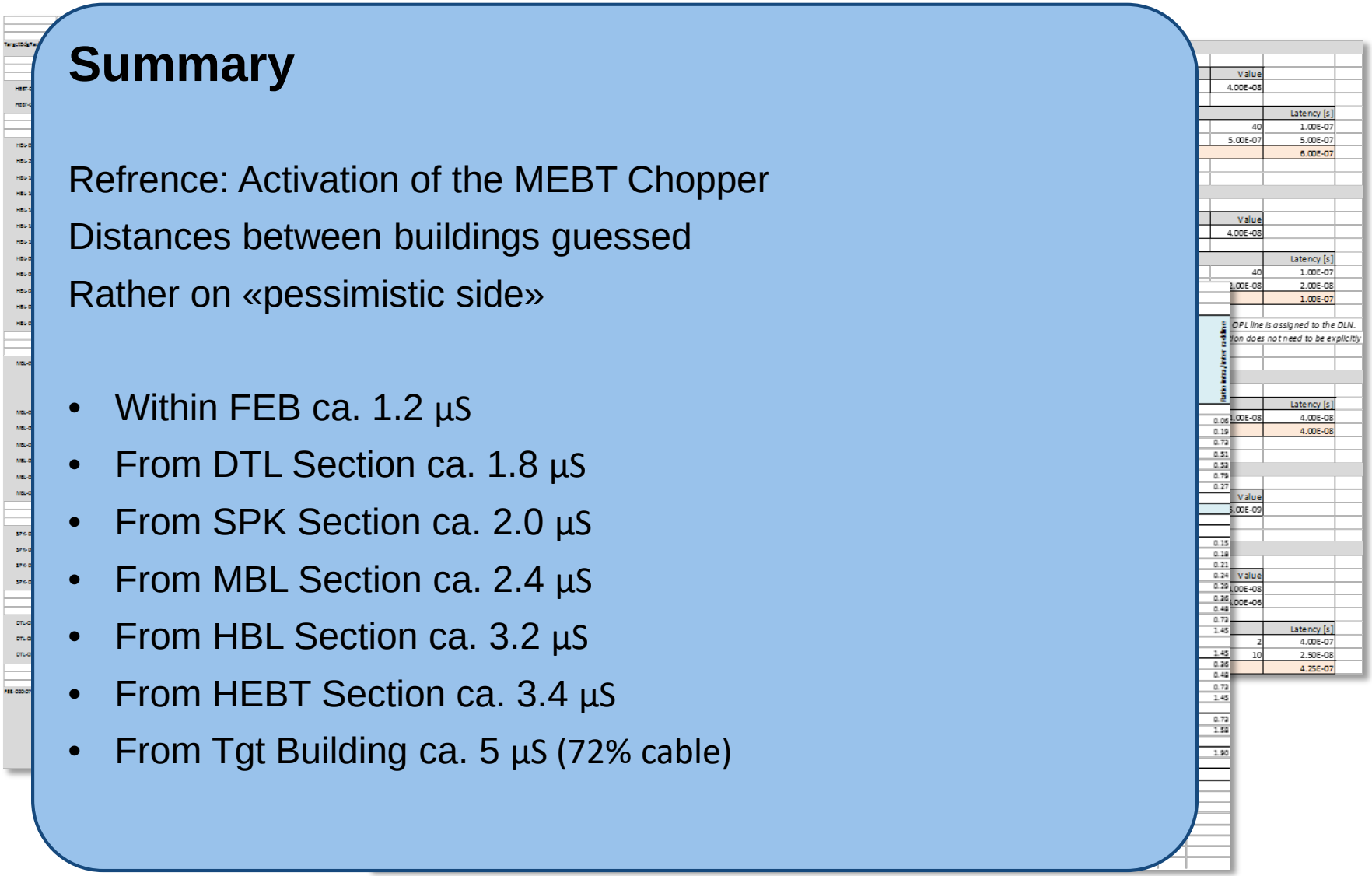
Summary

Refrence: Activation of the MEBT Chopper

Distances between buildings guessed

Rather on «pessimistic side»

- Within FEB ca. 1.2 µs
- From DTL Section ca. 1.8 µs
- From SPK Section ca. 2.0 µs
- From MBL Section ca. 2.4 µs
- From HBL Section ca. 3.2 µs
- From HEBT Section ca. 3.4 µs
- From Tgt Building ca. 5 µs (72% cable)



For more information see document:

FBIS_Architectural_Design_Proposal

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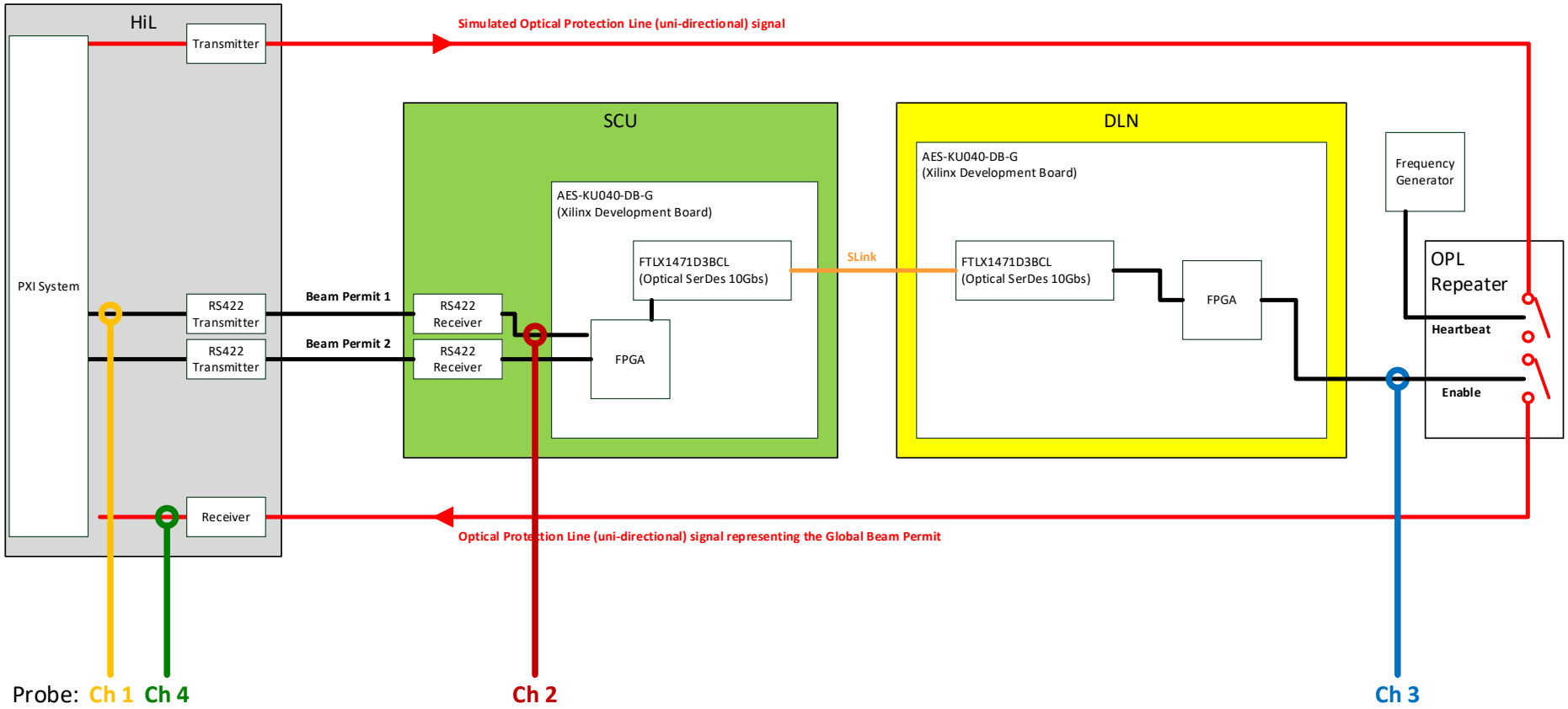
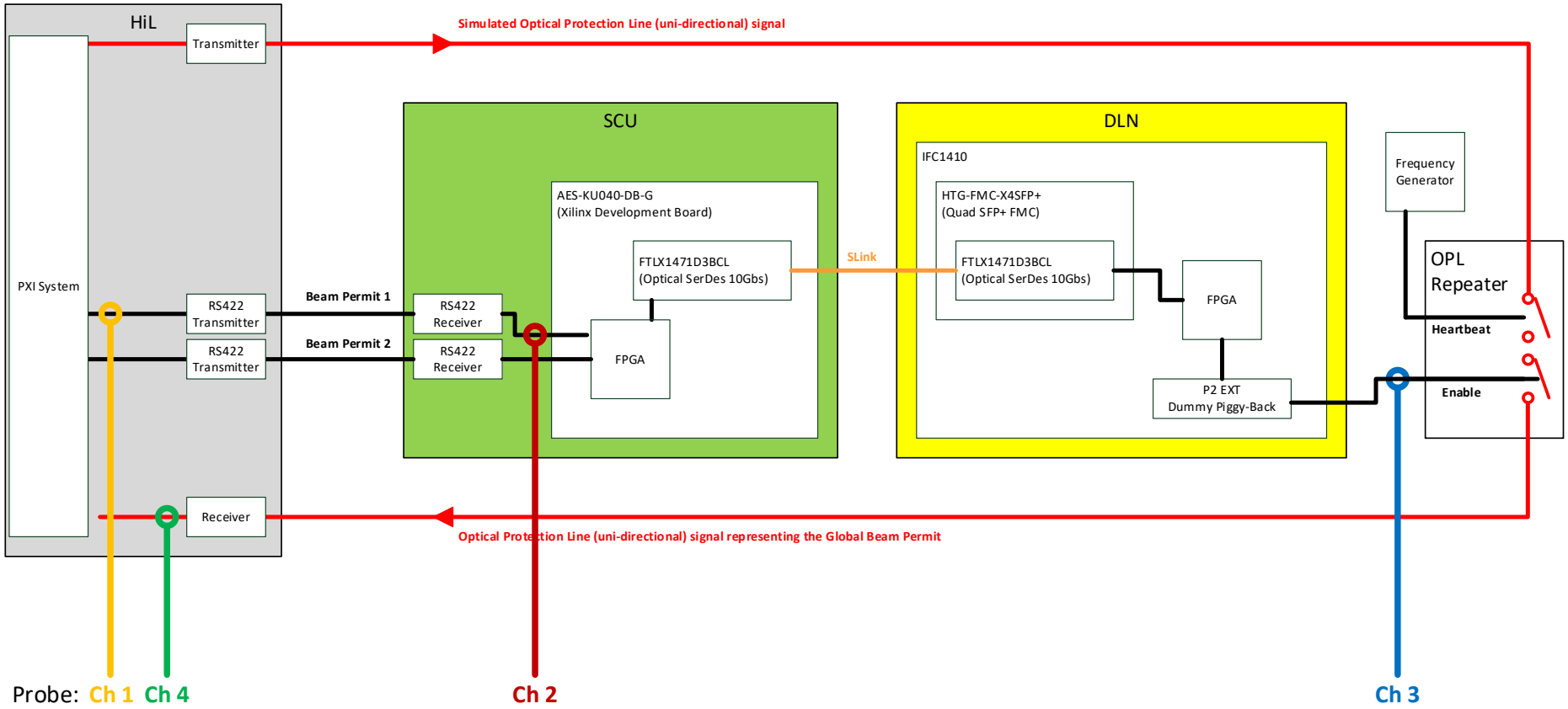
martin.rejzek@zhaw.ch

http://www.iamp.zhaw.ch/sks

Demonstration



Demonstration



Measurement (SLink = 1 m)
Beam Permit 1 = OK
Beam Permit 2 = OK

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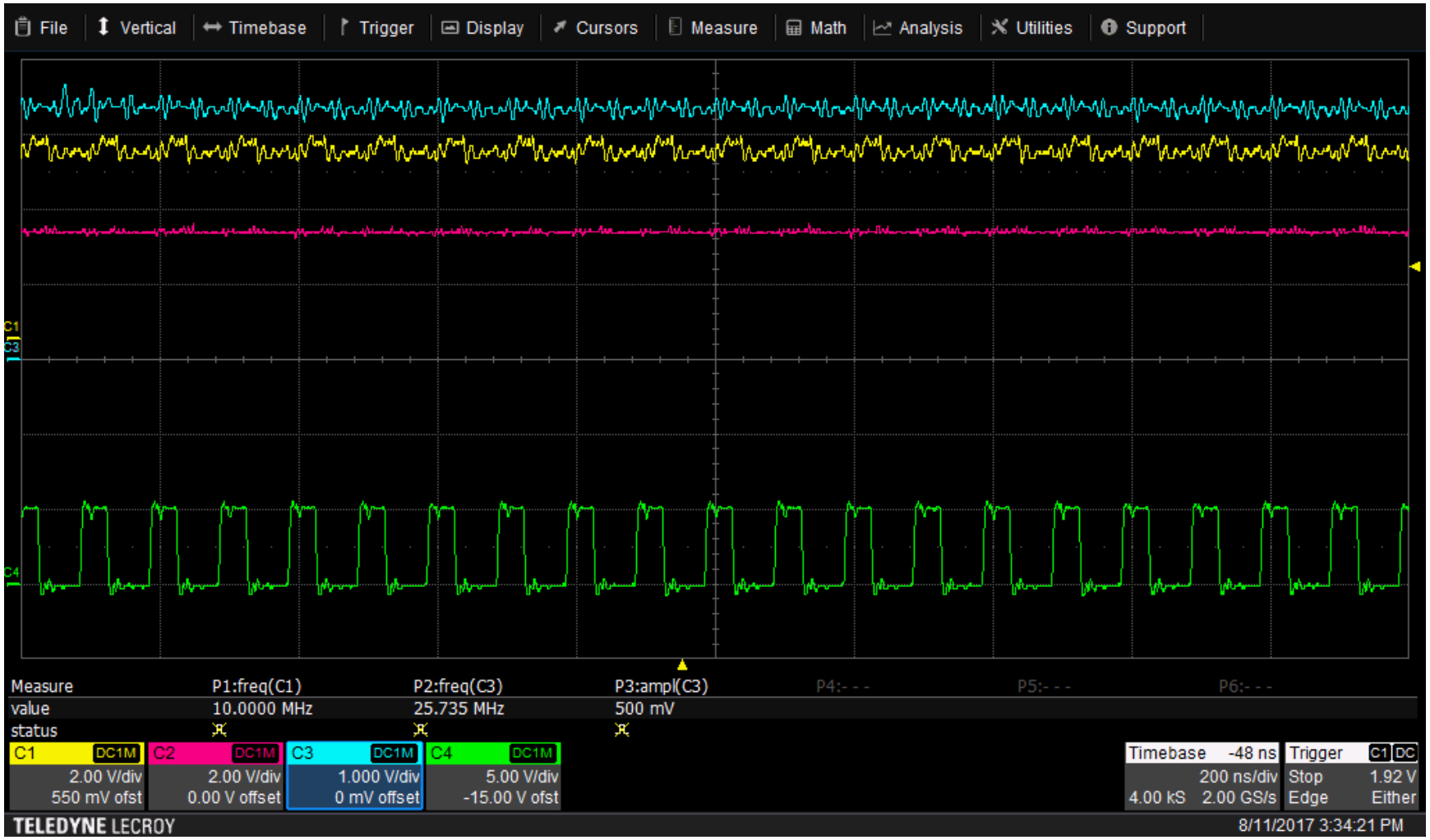

Measurement (SLink = 1 m)
Beam Permit 1 = OK->NOK
Beam Permit 2 = OK

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t=0 ns
t=35 ns
t=170 ns

Measurement (SLink = 1 m)
Beam Permit 1 = NOK->OK
Beam Permit 2 = OK

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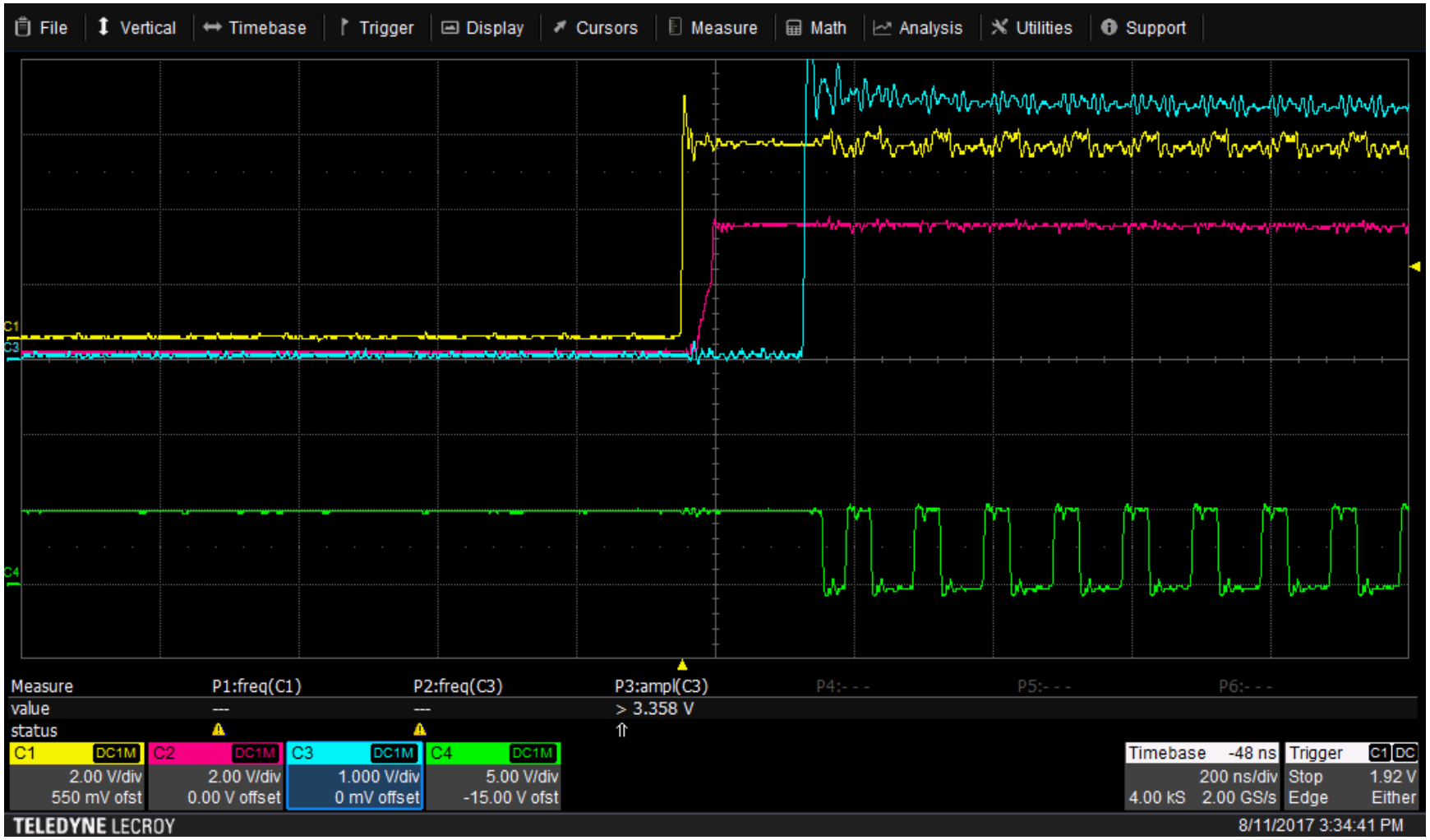

Measurement (SLink = 21 m)
Beam Permit 1 = OK->NOK
Beam Permit 2 = OK

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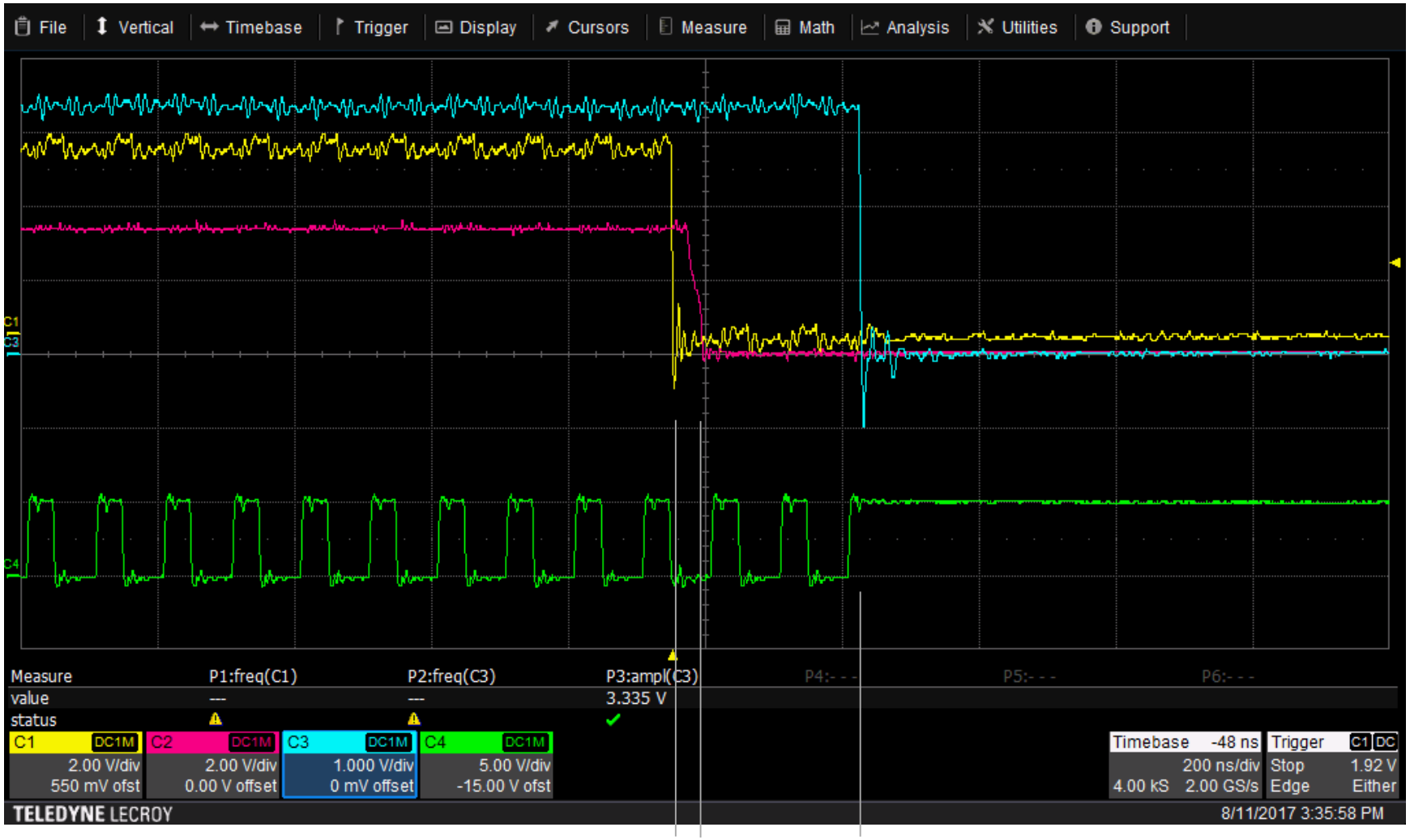

t=0 ns
t=35 ns
t=270 ns

Measurement (SLink = 21 m)
Beam Permit 1 = NOK->OK
Beam Permit 2 = OK

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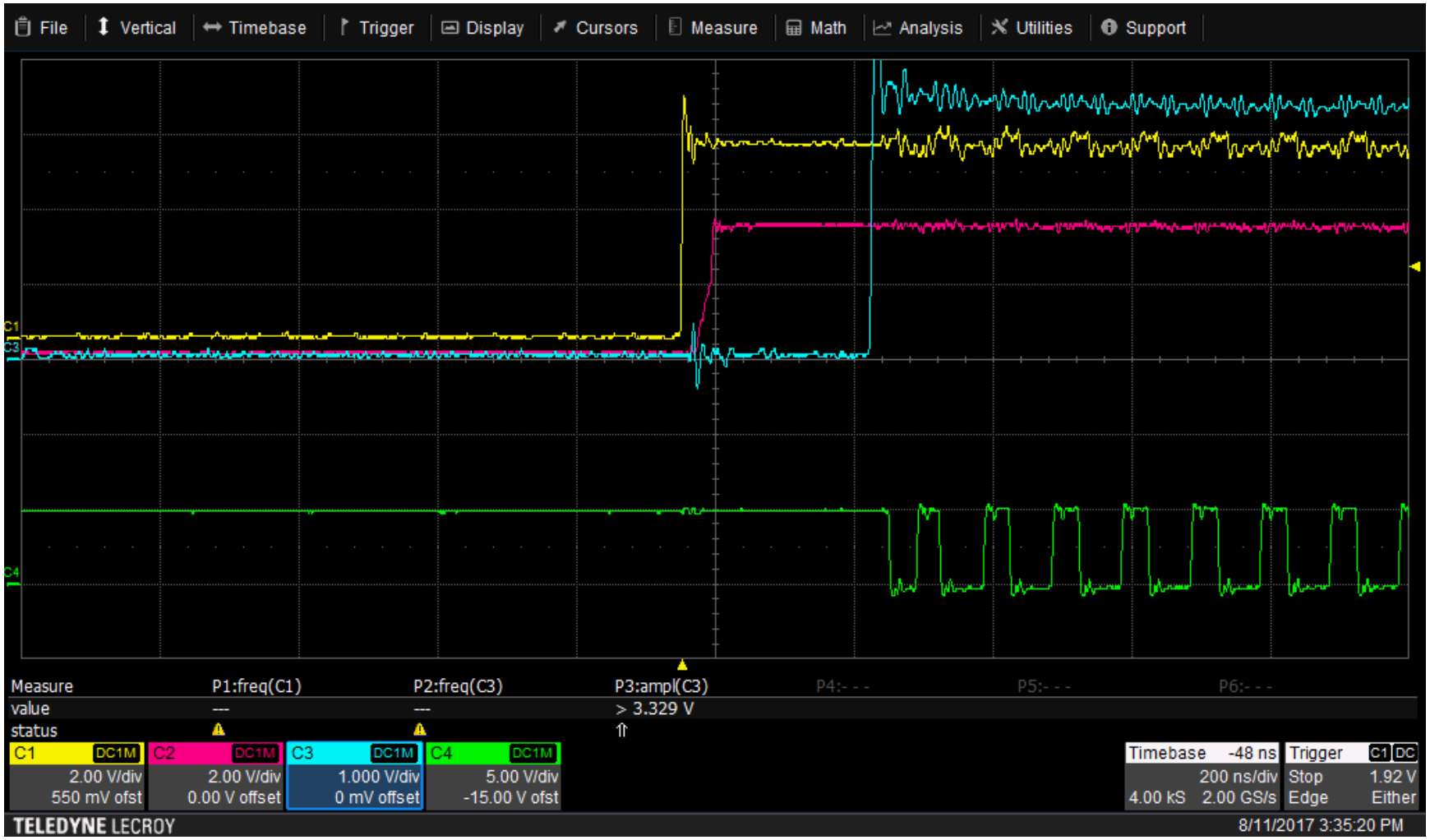

Backup Slides

DLN Integration into SCU

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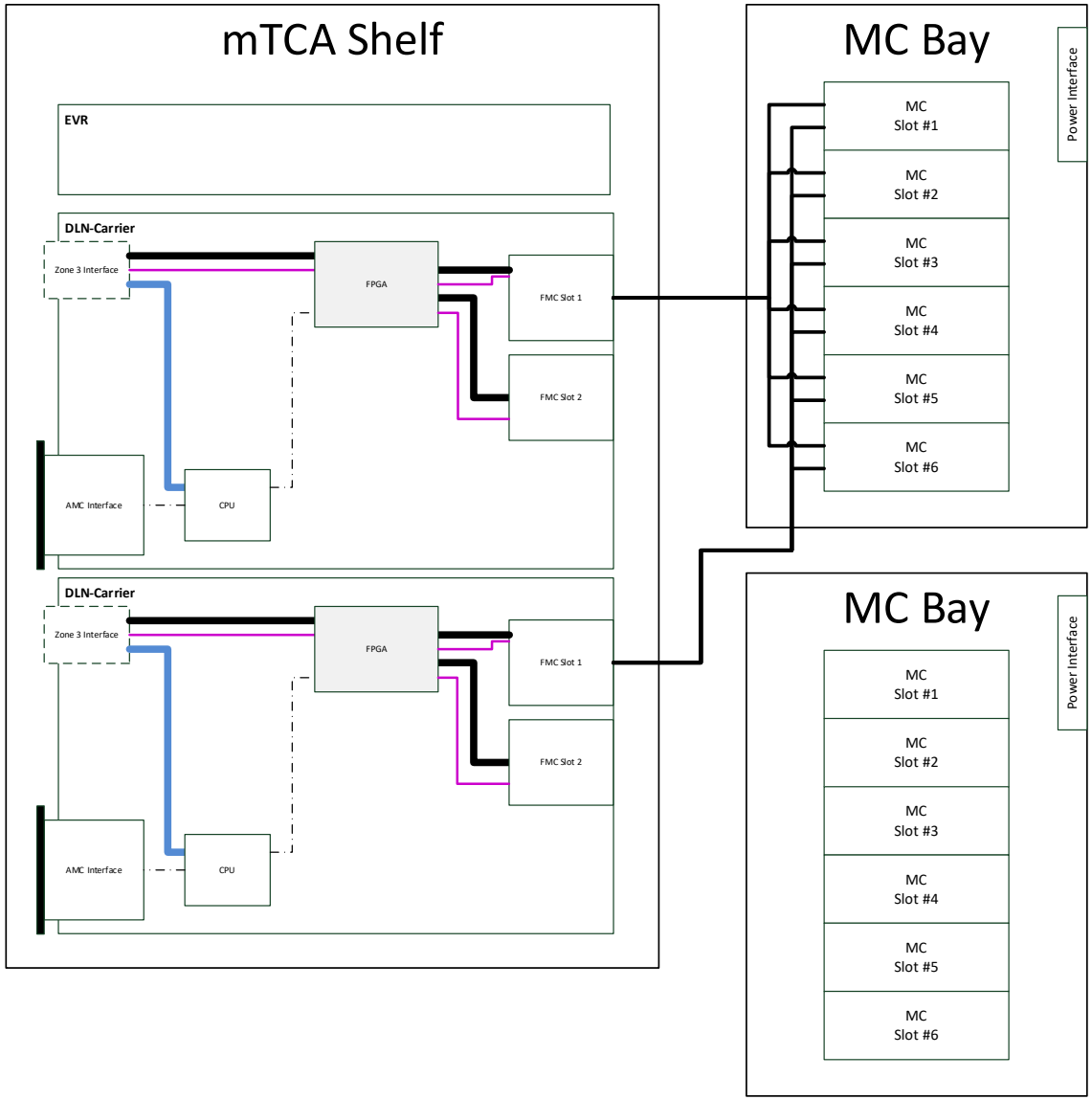

Latency Evaluation (complete Daisy Chain)

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Summary

Refrence: Activation of the MEBT Chopper

Distances between buildings guessed

Rather on «pessimistic side»

DLN integrated into SCU (no SLink)

Daisy Chain through all SCUs

- Within FEB ca. 1 µs
- From DTL Section ca. 1.2 µs
- From SPK Section ca. 1.9 µs
- From MBL Section ca. 2.8 µs
- From HBL Section ca. 4.5 µs
- From HEBT Section ca. 4.8 µs
- From Tgt Building ca. 5.8 µs (75% cable)

Values from previous slide:

- Within FEB ca. 1.2 µs
- From DTL Section ca. 1.8 µs
- From SPK Section ca. 2.0 µs
- From MBL Section ca. 2.4 µs
- From HBL Section ca. 3.2 µs
- From HEBT Section ca. 3.4 µs
- From Tgt Building ca. 5 µs (72% cable)

PSI Center For Proton Therapy – Patient Safety System

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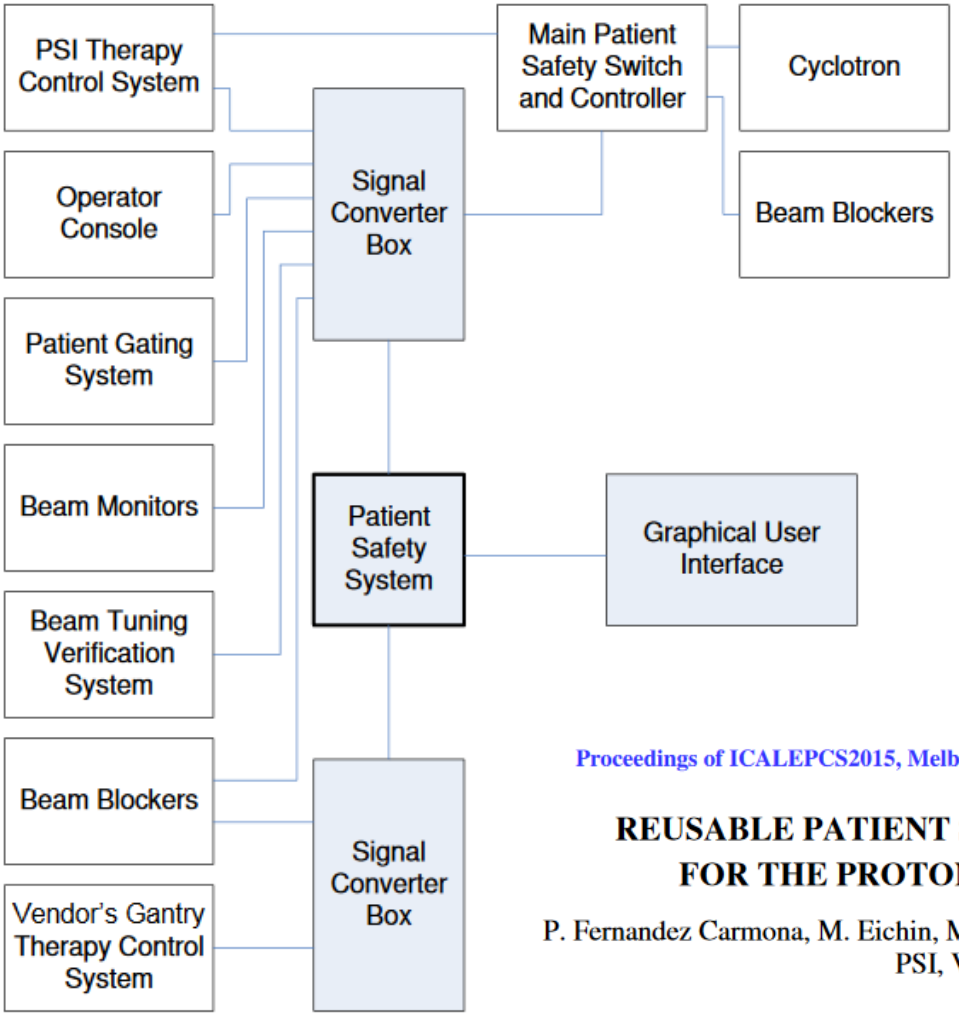

Proceedings of ICALEPCS2015, Melbourne, Australia - Pre-Press Release 23-Oct-2015 11:00TUC3O04

REUSABLE PATIENT SAFETY SYSTEM FRAMEWORK FOR THE PROTON THERAPY CENTRE AT PSI

P. Fernandez Carmona, M. Eichin, M. Grossmann, E. Johansen, A. Mayor, H.A. Regele
PSI, Villigen, Switzerland

PSI Center For Proton Therapy – Patient Safety System

Zurich University of Applied Sciences
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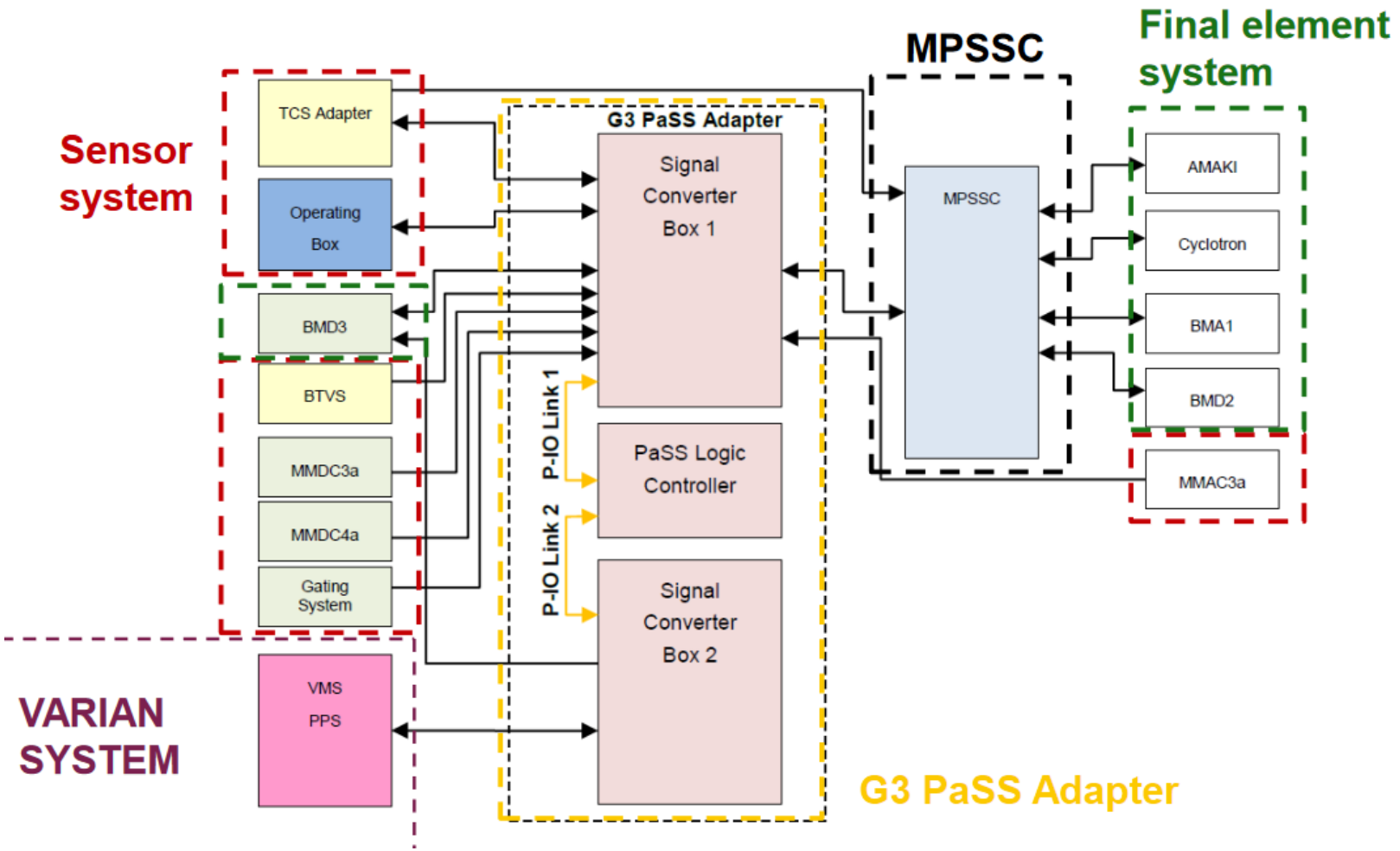
G3 PaSS System Overview



Zone 3 and FMC IO's

DESY Zone 3 Connector Pin Assignment Recommendation for Digital Applications

MTCA.4 management zone:

- Power, I^2C, optional JTAG support

Digital signals in the user zone:

- Class D1.0: 48 LVDS I/O signals
- Class D1.1: 42 LVDS I/O signals, 2 high-speed links
- Class D1.2: 38 LVDS I/O signals, 4 high-speed links
- Class D1.3: 28 LVDS I/O signals, 8 high-speed links
- Class D1.4: 8 LVDS I/O signals, 16 high-speed links

Digital signals with a fixed direction:

- 2 LVDS low phase noise clocks
- 1 LVDS timing output signal
- 3 LVDS outputs for user applications

FMC Standard:

Clocks
JTAG
I2C
Power

LPC:

- 34 pairs user-defined signals
- 1 MGT pair

HPC:

- 80 pairs user-defined signals
- 10 MGT pairs
- Additional clocks