EUROPEAN SPALLATION SOURCE

Technical report
Document Number ESS-0150746
Date: October 11, 2017
Revision 1
State Preliminary
Classification
Page 1 (6)

Electronics arcitechture (physical design)

	Name
Owner	**O. M. Røhne**
Reviewer	Erik Adli and Håvard Gjersdal
Approver	

1 Scope

This document describes the architectural design and preliminary implementation directions for the following components:

- cameras and read-out links
- image processing hardware
- hardware and software algorithms
- auxiliary systems

1.1 Operational requirements

The purpose of the system is to capture and process images from the proton window and target imaging systems and provide real-time feedback to the operator and, potentially also to the machine protection system. The differing latency- and thru-put requirements mandates a two-tier imaging processing architecture:

The first stage sensor calibration (pixel mapping) and feature extraction (beam profile bounds) will happen in programmable gate arrays (FPGA). The output of FPGA-processing stage has the lowest possible latency, allowing operational limits to be applied in synchronization with the $14\ \mathrm{Hz}$ repetition rate of the machine.

More refined processing algorithms will run on conventional CPU cores. These will perform e.g. geometric corrections and scaling, intensity normalization, and pseudo-coloring. The output of the CPU-processing stage will obviously have longer latency and larger jitter than the FPGA-stream.

2 Hardware system components

The implementation strategy for the image processing hardware is to rely to the largest possible extent on commercial off the shelf (COTS) components, selected and supported by the ESS ICS group.

2.1 Cameras and read-out links

There are three main cameras in the system. Of these, the tuning beam dump (TD) camera has distinctly different requirements from the two cameras for the target wheel (TW) and proton beam window (PBW).

2.1.1 Target wheel and proton beam window cameras

Two lines of cameras are specified for the PBW- and BEW application. Prototyping and initial deployment will make use of *standard performance* GigE Vision industrial cameras, while reaching the ultimate dynamic range will require a *low noise* scientific camera.

The selected low-noise camera is Hamamatsu ORCA-Flash4.0 V3. This model offers both Camera Link and USB 3.0, the choice between the two options will follow recommendations by ESS ICS.

For the prototyping work the Allied Vision Manta G-235B has been employed. At a later stage type-1 sensor size camera like Manta G419B might be preferred, as this camera is geometrically similar to ORCA-Flash4.0.

Figure 1: Image capture and processing hardware overview. *Can we still use this? Probably at least change to selected HW*

2.1.2 Tuning beam dump camera

For the tuning dump imaging a *standard performance* GigE Vision camera is specified, e.g. Allied Vision Manta G-235B or Manta G419B depending on the sensor size requirements.

2.2 The MicroTCA.4 chassis

The Micro Telecommunications Computing Architecture (MicroTCA) is a family of standards for chassis based modular electronics with provisions for forced cooling, hot-swapping, and multiple redundancy.

A chassis hosts a number of Advanced Messanine Cards (AMC). High-speed serial data flow between modules is provided by a multi-standard (PCIe, Ethernet, SRIO) interconnect switch fabric backplane. The switch fabric is controlled by a MicroTCA carrier hub (MCH), which also performs a number chassis service functions.

The MicroTCA.4 enhancement augments the base standard by defining a rear I/O area for specialized AMC modules, as well as Rear Transition Modules (RTM). The RTM allows high-density I/O as well as high-speed timing and synchronization.

2.3 Frame grabber and processing - Advanced Mezzanine Card

Each camera link end-point is served by a high-performance processing card in the AMC form-factor. For this role ESS has selected the IOxOS IFC_1410 Intelligent FMC Carrier AMC. The available processing resources include an PPC-type CPU and a Xilinx Kintex UltraScale FPGA. The AMC includes two FPGA Mezzanine Card (FMC) sites, and can host directly a camera read-out link.

2.4 External system interface - Rear Transition Module

A dedicated Rear Transition Module (RTM) might be needed to connect to the timing system as well as Machine Protection System Beam Interlock Signal (MPS/BIS). The RTM could also host the camera read-out link, either directly, or through a Small Form-factor Pluggable transceiver (SFP) site, or through an FMC daughter board.

3 Image processing pipeline

The two-tier image processing strategy is illustrated in Figure 2. The general idea is that minimal processing is implemented in FPGA, using a small but terse set of image operators. Further calibration, corrections and presentation adaptions will happen in software, running on conventional multi-core CPUs or GPGPUs.

3.1 Hardware processing system

The validation strategy for the low-latency hardware processing running in FPGA has two stages. First, a software-only implementation (golden model) reviewed for correctness, then the software- and hardware implementations are run against a set of test images. The hardware implementation is validated provided it gives identical result to the software.

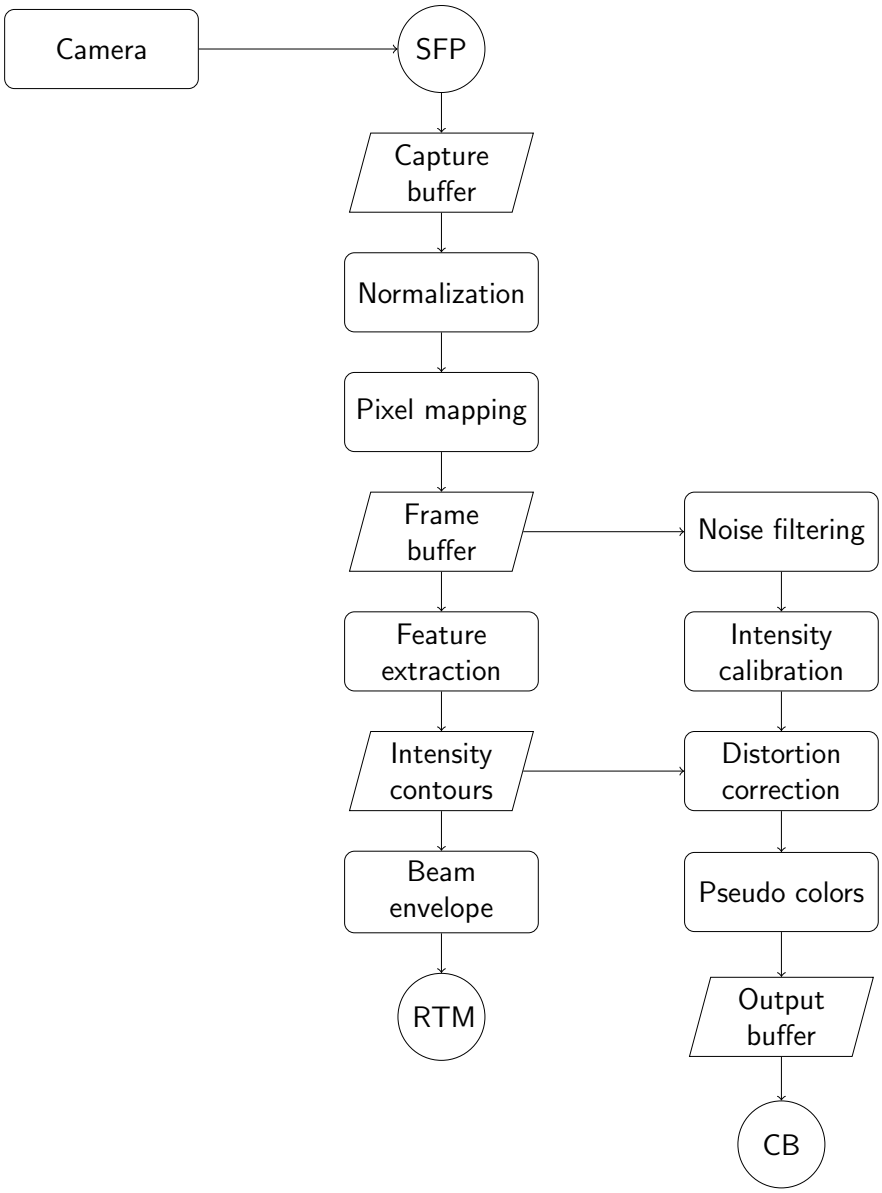

Figure 2: Data flow overview. The left-hand side processing chain will be implemented in FPGA hardware, the right-hand side in software running on CPU or GPGPU.

3.2 Software processing system

The CPU will receive pre-calibrated video frames, and then perform soft-real time processing using conventional software imaging algorithms. On the downstream system interface, the CPU will pose as an EPICS Control box, presenting imaging data in the form of an EPICS Area detector.

4 Auxiliary systems

A number of auxiliary systems are required for the settting up, monitoring and diagnosing the imaging system.

4.1 Mirror alignment correction

- number of axes: TBD
- must have controls outside the radiation environment

4.2 Final focus and iris

- could be conventional glass-objective focus drive

4.3 Filter wheels - neutral density

- 2x per imaging system

4.4 Tuning beam dump screen shuttle

- possible to swap or replace luminous screen during operation

4.5 Spectrometers

Two spectrometers are installed on beam-splitter ports in each imaging system. In order to maximize their diagnostic utility they need to accomodate a wide range of sensitivity/integration time and they must also support beam-synchronous acquisition

4.6 Illumination system

A laser based back-illumination system is expected to be critical for the alignment of the optical system. The illumination system requires controls, including:

- laser power level
- synchronization and timing
- mecahnical motion of alignment axes

4.7 Environmental monitoring

Thermo-mechanically induced deformation of the optical path is a primary concern for its light yield and image quality.

- Expect target to provide environmental monitoring
- Need support for own monitoring of mirrors and mounts

5 Commissioning GUIs

The IMG will be read out through the integrated control system (ICS). For the system commissioning *commissioning GUIs* will be made in order to test the system, first without beam then with beam. Commissioning without beam can be down once the IMG is installed in is final location, using the illumination system. Commissioning with beam can be done once the first beam reaches the target and tuning beam dump.

ESS will provide EPICS support, code review services and standard FPGA and software frame-works. In particular, ESS will provide all layers of device drivers and control system software for cameras, up to the point of delivering a demo software which acquires images

Contribution of the Oslo group: the Oslo group work will be based on an ESS demo application, delivered by ESS, acquiring images. The task of the Oslo group is thus to work within the application layer in order to make GUIs and panels to provide the tools for an efficient commissioning of the IMS.

6 Prototyping work and outlook

Prototyping work is currently starting at Oslo. An ESS EPICS Environment (EEE) server has been installed. There is also a laptop configured as a Development Machine (DM). Next steps include procurement of an EEE/DM supported camera, as well as the implementation and integration of software processing algorithms into Control Box. Any hardware prototyping is pending the availability of the ESS-selected FPGA platform.