



Elettra Sincrotrone Trieste

- *Critical Design Review* -

WS acquisition system

planning, budget, reliability &

response to PDR

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Elettra Sincrotrone Trieste

There is an overall **6-M net delay** due to late ***Test at Partner Lab***

- ✓ from our side, the Test at Partner Lab was a strong & agreed **pre-requisite for CDR & Series prod.**
- ✓ Main concerns were:
- ✓ ***AFE sensitivity***
- ✓ ***AFE EMC in-tunnel & AFE+BE for analogue signal transmission***

CDR marks the end of the project phase, including testing of prototype, and releases the construction phase

Currently, we have:

- CDR-1 DEC 2016
- CDR-2 MAY 2017fine, in principle, but....
- prototype Test at PARTNER Lab : **MAY 2017 !!!**

After Test@P_LAB, it makes sense to foresee a **Design Review** to cope with any possible issue should have emerged

Our proposal would be to unify CDRs (1&2): **MAY 2017**

Carry out the **Test @P_LAB by FEB 2017**

Include a **Design Review in the MAR-APR** time frame

Last but not least this avoids to have **PDR-2** and **CDR-1** in the same DEC 2016 time frame



ESS WS ACQ SYS PDR-1

Mario Ferianis June 28, 2016



- ✓ Originally (at PDR-1 - June 2016) scheduled for May 2017 in Paris;
- ✓ Finally done in **Nov 2017 at CERN!!!**

Running tasks to completion: **critical item**

- ✓ **Scintillator prototype development** *external - ESS leads effort*
- ✓ **SCINT prototype test at Partner Lab.** **OFE+BE_{mod}+SCINT+beam**
- ✓ Test is scheduled at **HiRadMat** test facility at CERN

High-Radiation to Materials Facility of CERN/SPS



- ✓ It is a multi lab effort: ESS, Elettra, CERN and IHEP (SCINT development)
- ✓ In tunnel installation in April - beginning of May (courtesy of Slava G.)
- ✓ 1st beam time at week 19-20 of May
- ✓ On *WSAS schedule* is from **April, 27th** to **May 31st**

Vertical Integration Test (VIT) at ESS

- ✓ Scheduled for **April, 19th** to **May, 18th**

Running tasks to completion: Series Production

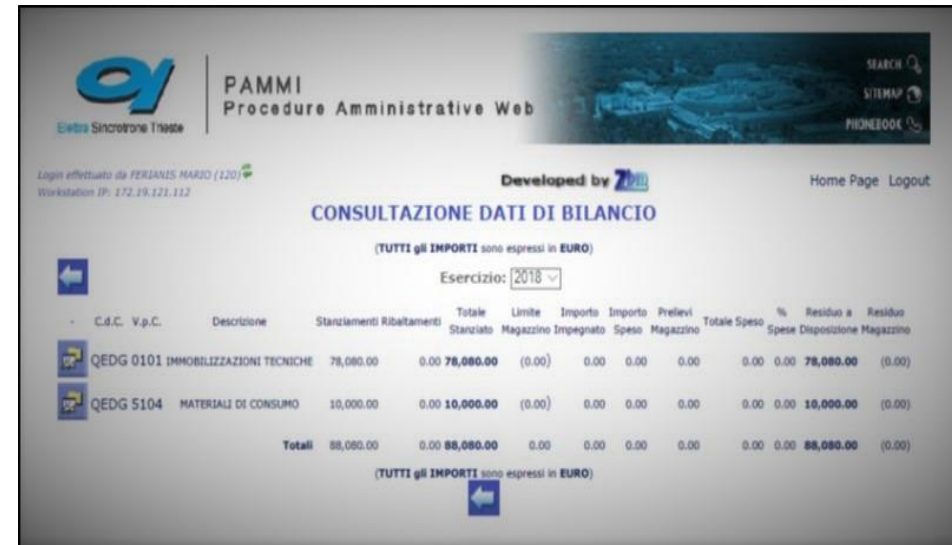
- ✓ Budget has been allocated and is (almost) **READY TO GO**
- ✓ IK contract signed between parts...Board of Director empowered CEO to go ahead...
- ✓ ...this week: **CEO in Rome**, to solve one general VAT issue with INFN big BOSS
- ✓ **SEM section production** is actually scheduled from Feb, 23rd to Oct, 10th

We have figured out 2 batches:

a) 3 x (AFE + BE) >>> MEBT: due by June, 20th

b) all the rest: due by Oct.10th

- ✓ **SAR-1 due on Oct, 12th 2018**



The screenshot shows the 'CONSULTAZIONE DATI DI BILANCIO' (Balance Sheet Data Consultation) interface. It displays a table with columns for C.d.C. V.p.C., Descrizione, Stanziamenti Ribattamenti, Totale Stanziamento, Limite, Importo, Importo Impegnato, Prelevi, Totale Speso, % Residuo a Spese, and Residuo a Disposizione. The data is for the exercise year 2018. The table shows two rows of data: QEDG 0101 IMMOBILIZZAZIONI TECNICHE and QEDG 5104 MATERIALI DI CONSUMO. The total for both rows is 88,080.00.

Construction budget release after Signature	0 days	23/02/18	23/02/18
SEM PO for: Components; PCB; Assembly	24 days	23/02/18	28/03/18
Delivery of first series to ESS (SEM)	60 days	29/03/18	20/06/18
Manufacturing of SEM module series	56 days	21/06/18	06/09/18
In-house acceptance test of SEM module series	19 days	07/09/18	03/10/18
Shipment to ESS – SEM modules	5 days	04/10/18	10/10/18

Running tasks to completion: Series Production

- ✓ **SCINT section production** is actually scheduled from Jun, 6th to Jan, 11th 2019
- ✓ We have figured out a single batch: **shipment to ESS, due by Jan, 11th 2019**
- ✓ SAR-2: Full SCINT system **due on Jan, 11th 2019**

Delivery of SCINT prototype by ESS	0 days	27/04/18	27/04/18	
SCINT detector prototype test at Partner facility (SCINT)	25 days	27/04/18	31/05/18	44
SCINT mode TESTED	0 days	31/05/18	31/05/18	45
SCINT PO for: Components; PCB; Assembly	50 days	01/06/18	09/08/18	46
Manufacturing of SCINT Module series	80 days	10/08/18	29/11/18	47
In-house acceptance test of SCINT module series	20 days	30/11/18	27/12/18	48
SAR-1 SEM only	0 days	12/10/18	12/10/18	43
Shipment to ESS – OFE modules	11 days	28/12/18	11/01/19	49
COTS hardware available & tested at ESS site	0 days	01/06/18	01/06/18	
SAR-2 Full system SCINT	0 days	11/01/19	11/01/19	51

Series Production synoptic table: SEM + SCINT + SW...

item	Number pieces	Start date	End date	Notes
AFE, BE 1st batch	4, 4	23-02-2018	20-06-2018	Including shipment
AFE, BE 2nd batch	9, 9	23-02-2018	10-10-2018	Including shipment
OFE, BE_{mod}	5, 5	01-06-2018	11-01-2019	Including shipment
SAR-1	-	12-10-2018	-	At ESS
SAR-2	-	11-01-2019	-	At ESS
WS ACQ SYS SW	-	12-10-2018	-	official delivery date for SW is SAR-1

No major issues on this...which is good!

- ✓ We had been assigned the requested resources (€€€ !!!)
- ✓ At the beginning, one issue only needed to be worked out:
WS ACQ SYS COTS supply by ICS (*the Piso-Fabris agreement*)
- ✓ No EU tenders needed for this project *faster procedure!*
- ✓ Elettra will pay for VAT (less than INFN overhead costs) *faster procedure!*
- ✓ **Purchase Orders (PO)** will be issued for:
 - ✓ - printed circuit boards: 4 codes (AFE, OFE, 2 x BE), small quantities
 - ✓ - PCB pick & place & visual inspected
 - ✓ - AFE module, case & assembly (partially in-house)
 - ✓ - BE module, case & assembly (partially in-house)
 - ✓ - OFE photodiodes and avalanches (by Hamamastu, usual supplier)
 - ✓ - OFE metal machining
- ✓ Usually we give to the manufacturer a tested prototype and our quality specs and they just cut & paste & test

Quality: a key ingredient for reliability

- ✓ Accurate analysis carried out on the in-house developed HW modules and on In-house developed software

Quality starts at:

- ✓ Technical Annex, WS Conceptual Design and Specifications by ESS
- ✓ Installation constraints (in-tunnel AFE installation)
- ✓ Elettra in-house expertise

Quality attitude by design:

- ✓ team of senior designers & programmers at Elettra
- ✓ quality tested PCB manufacturing and supplier chain
- ✓ adoption of commercial rad-tolerant components from known manufacturers
- ✓ adoption of high quality components for the HW modules

Specifically on electronics board manufacturing

- ✓ Standard formats for PCB cards, standard size and component series (SMD resistances or capacitances), standard frames (crates)
- ✓ Altium Designer™ software for the creation of schematics, gerber files, BoM standard copper thickness for PCB, and standard connectors for interfacing
- ✓ Standard proven procedures already used many times in the past (Cavity BPM and Machine Protection System of FERMI, like:
 - ✓ to use electronic components easily available on the European market
 - ✓ to use electronic components tested, but far from possible obsolescence
 - ✓ before delivery, all HW modules are 100% tested and calibrated in-house
- ✓ For the design of mechanical part the standard CAD tools have been used
- ✓ All mechanical parts are manufactured in the ELETTRA workshop using numerical machinery
- ✓ The assembly of all mechanical parts will be carried out in the Instrumentation Laboratory at ELETTRA or under its direct supervision

RAMI: foreword

- ✓ Although the WS is not a mission critical system, in the sense that a malfunction of a WS sub-system will not prevent ESS Accelerator to operate, a RAMI analysis has been carried out as requested by ESS IKC procedure
- ✓ Typically, (ITER) the Board evaluates RAMI adoption, which has a cost, and compares it to the expected benefits
- ✓ A system has to be designed and verified in order to meet:
 - ✓ **Reliability** to provide continuous correct operation
 - ✓ **Availability** to perform the required function it has been designed for
 - ✓ **Maintainability** to design for performance without neglecting failure effects
 - ✓ **Inspectability** in-situ monitoring of equipment, capable to predict fault

One example: AFE design

- ✓ AFE is a critical HW module for required performance and for installation site
- ✓ Servicing a faulty AFE in the accelerator tunnel may not be easy and rapid
- ✓ You could not even take it out the tunnel for diagnose and debug
- ✓ Therefore, specific design actions have been taken to increase its reliability:
- ✓ Do not use digital electr., do not use PS, use rad tolerant analogue ICs

RAMI also for software?

- ✓ Actually, dealing with software usually we'd rather talk about:

RAS: Reliability, Availability and Serviceability

- ✓ SW is intangible; SW failures are due to design and/or implementation errors or
- ✓ SW failures may occur due to underlying hardware or low-level element faults
- ✓ In the SW section (RAS) of our RAMI document we have analyzed its specific operation environment and have identified some CAVEAT (do not use virtual machines or implement automatic updating procedures) which could contribute the correct and fault free operation of the SW
- ✓ Some other key issues for SW RAS are part of ICS procedures (data archiving)

Source of failure analysis / preventive actions

- ✓ It has been carried out for both HW modules and SW blocks
- ✓ AFE: wire integrity check, amplifiers check, power supply monitoring
- ✓ BE is equipped with on-board PIC μ -controller running also house keeping and monitoring functions, both on it and on the attached Front End

IEC voltage range	AC (V_{rms})	DC (V)	Defining risk
High voltage (supply system)	> 1000	> 1500	Electrical arcing
Low voltage (supply system)	50–1000	120–1500	Electrical shock
Extra-low voltage (supply system)	< 50	< 120	Low risk

item	location	power supply voltage	PS source	generated voltages / amps / to	Extra Low Voltage
AFE	MEBT/ tunnel	+/- 5V	BE	<100V DC / 1mA / wire	yes
BE	service gallery	220V AC	mains	+5V / AFE 100V DC / wire	yes
OFE	service gallery	+/- 5V	BE	none	yes
BE_{mod}	service gallery	220V AC	mains	+5V / OFE 120V DC / wire	yes

Thank You!

item	MEBT	SPOKE	ELLIPTICAL	A2T	Total	notes
AFE	3	3	4	1	11	+ 2 spares = 13 in total
BE	3	3	4	1	11	+ 2 spares = 13 in total
OFE	0	0	4	1	5	+1 spare + 3 FAST WS = 9
BE_{modified}	0	0	4	1	5	+1 spare + 3 FAST WS = 9
SCINT	0	0	4x4	1x4	20	not part of ST IKC
uTCA CPU	3	3	4	1	11	not part of ST IKC
ADC SIS-8300	3	3	8	2	16	not part of ST IKC
EV_RX	3	3	4	1	11	not part of ST IKC
Motion axis	3	6	8	2	19	not part of ST IKC

acronyms

✓ **AFE** analogue front end **OFE** optical front end **BE** back end