CDR of the

Wire Scanner Acquisition System

- System Description -

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1.1. Purpose of the document

The Wire Scanners (WS) are used at different locations on the ESS accelerator to measure the transverse beam profile.

Several WS are located at the Medium-Beta Linac, the High-Beta Linac, the High Energy Beam Transport and at the Accelerator to Target of ESS accelerator.

The WS Acquisition System presented in this document is formed by in-house designed electronic modules at Elettra Sincrotrone Trieste as well as by control software, on purpose developed by Elettra under EPICS.

In this document, the characteristics and performances of the developed modules and of the control software are presented as well as the results of the tests carried out both at Elettra Sincrotrone Trieste Instrumentation Laboratory and at CERN on LINAC4 complex test run.

1.2. Definitions, acronyms and abbreviations

Throughout this document, we have used the abbreviations reported in Table 1.

Abbreviation	***Explanation of abbreviation***
WS	Wire Scanner
ST	Elettra Sincrotrone Trieste
ESS	ESS ERIC
ACQ SYS	Acquisition System
AFE	Analogue Front End module
OFE	Optical Front End module
BE	Back End module
BE_{mod}	Modified Back End module
SEM	Secondary Emission Monitor
SCINT	Scintillator
MEBT	Medium Energy Beam Transport ESS accelerator section
A2T	Accelerator to Target ESS accelerator section
ICS	ESS ERIC Control Group
WS IOC	Wire Scanner In-Out Controller
SbS	Step By Step WS IOC procedure
OtF	On The Fly WS IOC procedure

Table 1 – Abbreviations

1.3. References

[1] ESS-0020237 **European Spallation Source wire scanner conceptual design,** Rev. 1.0, November 21, 2014.

[2] ESS-0048680 **Technical Specifications Wire Scanner Acquisition**, Jan25, 2016, Rev. 1.0, State: Released.
[3] CDR 1
[4] CDR 2
[5] ESS-0059909 **Wire Scanner Controls In-Kind Technical Specification** – Rev. 1.

1. WS ACQUISITION SYSTEM CHARACTERITICS

The ESS diagnostic system adopts Wire Scanners for the measurement of the transverse beam profile, though not on delivery beam. The WS diagnostics is based on two main sub-systems: the WS itself and the WS Acquisition System. The WS mechanical/vacuum assemblies are being developed by other IKC Partners or Suppliers; the WS ACQ SYS, presented in this document, is part of the Italian IKC to the ESS diagnostics, from ST to ESS.

1.1. System general outline

The purpose of the WS ACQ SYS is to acquire, and to made available to the ESS ICS, the signals either electrical or optical generated when a thin metal wire is scanned across the ESS accelerator vacuum pipe. As the amplitude of these signals is proportional to the charge density at that specific transverse coordinate of the wire, the beam transverse profile may be obtained by plotting the signal amplitudes vs. the wire transverse position.

A schematic representation of the WS operating principle is shown in Fig.1 below.

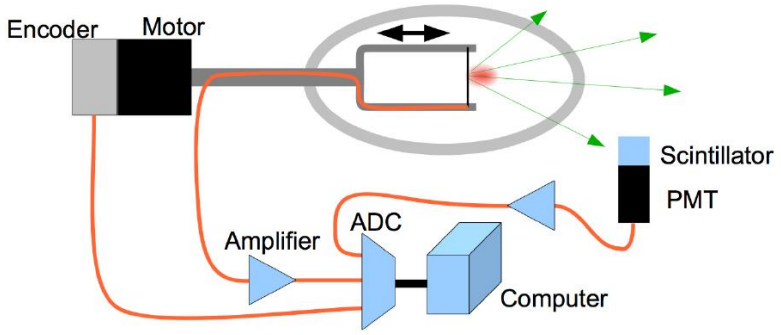

Figure 1: schematic representation (taken from ref. [1]) of the wire scanner operating principle, including the WS acquisition system.

A detailed analysis of the expected signal levels at different ESS sections, i.e. at different beam energies, has been carried out in [1]. Two signal sources have been identified in [1]: SEM and SCINT. In the SEM system, the secondary emission current, generated in the wire when hit by the beam, is acquired and measured. In the SCINT system, the light generated in a scintillating bulk material when exposed to the shower of secondary radiations coming from the wire-beam interaction, is detected by a high sensitivity photo diode connected to an optical fiber used to bring the light outside the machine tunnel.

In the same document [1] is also clearly explained how, by considering the physics of the two phenomena involved in the SEM and SCINT schemes, at the lower beam energies the electrical signal is a more efficient source of information whereas at higher energies the light from the SCINT is the optimal solution to our problem.

Therefore, the WS ACQ SYS, at the low level, is made of custom designed HW modules; at the high level, commercial-of-the-shelf (COTS) digital boards have been deployed to digitize the analogue signals.

Two **front-end / back-end** pairs have been developed to interface the low level signals to the digital part; these are the **Analogue Front End** and the associated **Back End,** for the SEM current readout, and the **Optical Front End** and the associated **Modified Back End,** for the SCINT light readout.

A specific control and processing code, running under EPICS, has been developed as well to make to physical signals available at the ESS ICS as beam transverse profiles; a set of general “user” and “engineering” panels have been developed for this purpose.

In fig. 2 below, the general block diagram of the ESS WS ACQ SYS for a single wire scanner is presented; it is worth mentioning here that the **AFE** is the only electronic module which sits in the machine tunnel requiring special design and implementation rules.

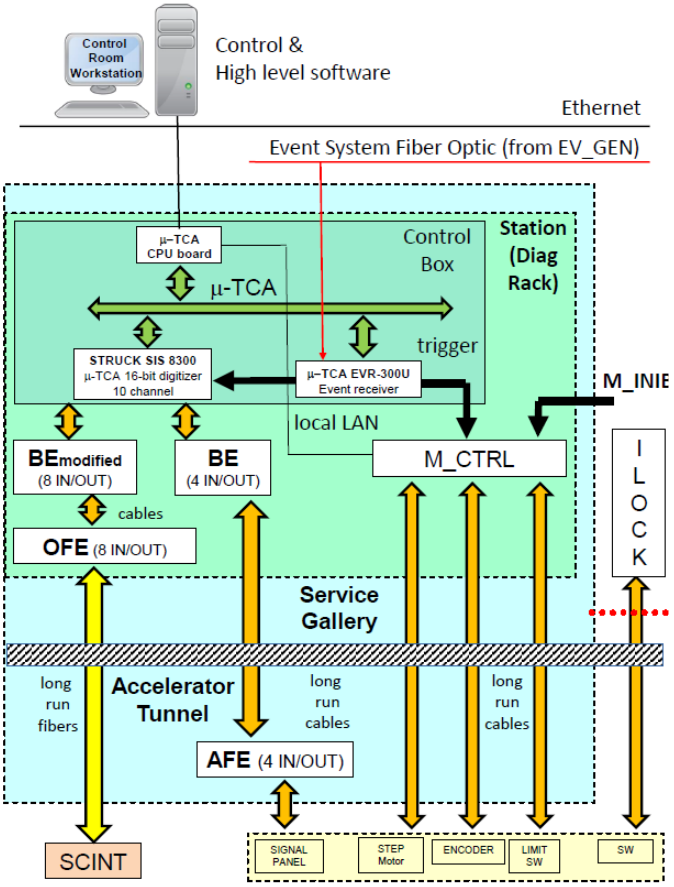

Figure 2: block diagram of the wire scanner acquisition system;
the single WS case is presented here.

1.2. WS ACQ SYS global picture

Two different types of WS devices are planned to be installed at different sections of the ESS accelerator complex. Depending on the beam energy at a given location, either the SEM signal only or both the SEM and SCINT signals will be acquired. This global picture is shown in figure 3a and 3b, below.

On the low energy part (**MEBT**) of the accelerator, three single-axis/double-wire WS will be installed. These units, developed by **ESS-Bilbao**, provide both horizontal and vertical profiles using a single actuator: the actuator moves along a 45º rotated axis w.r.t the reference vertical axis. Also, on this low energy section, only the signals for the SEM current developing on the wire itself will be acquired, as the scintillator yield has been evaluated [1] to be too low.

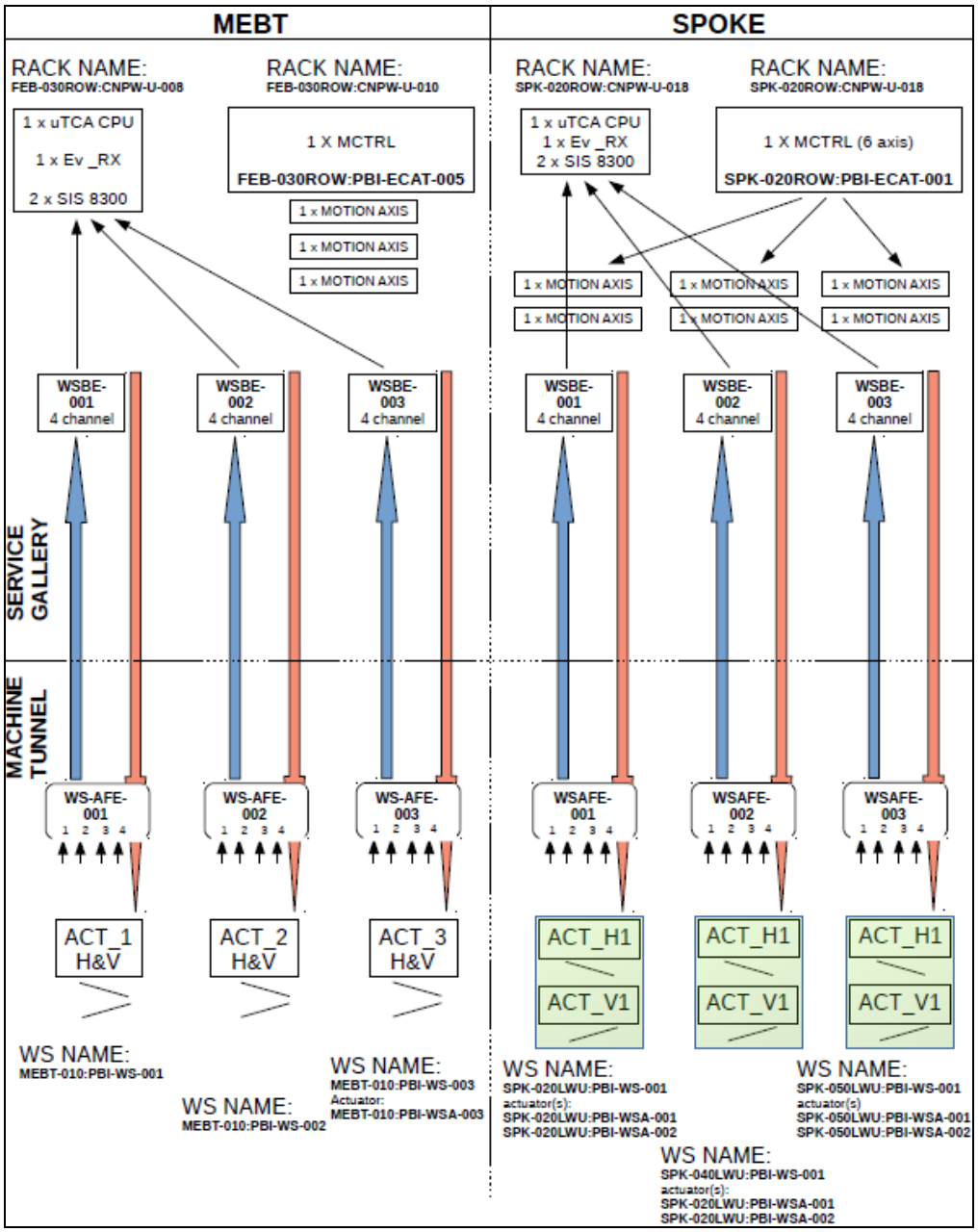

Figure 3a: the global picture of the WS ACQ SYS (MEBT and SPOKE sections), showing all main system components, including the custom developed modules by ST as well as the COTS device provided by ICS.

From the SPOKE section onward, the second type of WS will be installed; it is a single-axis/single-wire device developed for ESS by Danphysik. Three WS of this second type will be installed on the SPOKE section, acquiring only the SEM signal from the wire.

At higher beam energies, four more single-axis/single-wire WSs will be installed in the ELLIPTICAL section and one at the A2T section (see figure 3b), each one equipped also with four scintillator assemblies.

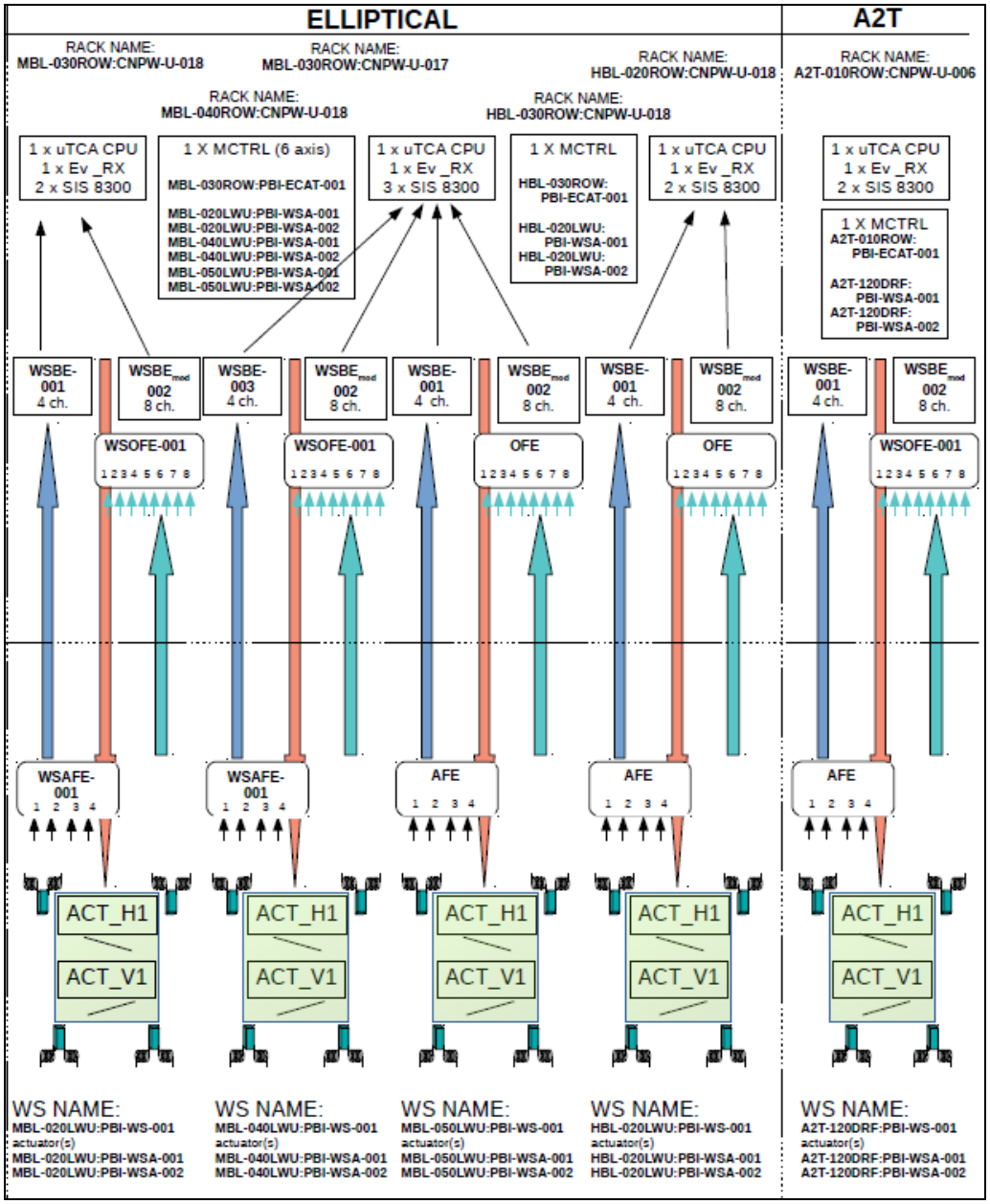

Figure 3b: the global picture of the WS ACQ SYS (MBL, HBL and A2T sections), showing all main system components, including the custom developed modules by ST as well as the COTS device provided by ICS.

Summarizing, the total quantities of the WS ACQ SYS are listed in table 2.

item	MEBT	SPOKE	ELLIPTICAL	A2T	Total	notes
AFE	3	3	4	1	11	+ 2 spares = **13** in total
BE	3	3	4	1	11	+ 2 spares = **13** in total
OFE	0	0	4	1	5	+1 spare + 3 FAST WS = **9**
$BE_{modified}$	0	0	4	1	5	+1 spare + 3 FAST WS = **9**
SCINT	0	0	4x4	1x4	20	not part of ST IKC
uTCA CPU	1	1	3	1	6	not part of ST IKC
ADC SIS-8300	2	2	7	2	13	not part of ST IKC
EV_RX	1	1	3	1	6	not part of ST IKC
Motion Controller (3 axis)	1 (3)	1 (6)	2 (6+2)	1 (2)	5	not part of ST IKC

Table 2 – WS ACQ SYS total quantities

It is worth noting here how the COTS boards and crates part of the WS ACQ SYS will be provided by ICS.

1.3. AFE / BE for the SEM current read out

The main purpose of the AFE / BE pair is to detect and deliver to the Service Gallery the weak current pulse that originates in the WS wire while it is hit by the beam.

The specifications of the SEM current read out module have been presented in [1,2]. The proposed solutions have been presented at the CDR-1 [3].

Due to the ultra-low current level developed in the thin wire, the AFE front end needs to sit as close as possible to the WS, i.e. in the accelerator tunnel. As this is a radiation hard environment only analogue RAD-tested electronics has been used in the AFE while this module is powered from the BE back end, as power supply are typical rad sensitive devices.

The detected current is then transmitted to the BE, which sits in the Service Gallery, over a shielded twisted pair line. Finally, the resulting voltage pulse is sampled by the ADC module housed in the μ-TCA crate.

As said, all supply voltages are generated inside the BE and sent to the AFE over voltage compensated lines; also some control lines are used to set the AFE operating mode properly.

1.4. OFE / $BE_{modified}$ for the SCINT read out

The main purpose of the OFE / BE pair is to detect and deliver to the Service Gallery the light pulses that originates in the scintillator devices, located downstream each WS, while it is hit by the beam.

The specifications of the SEM current read out module have been presented in [1,2]. The proposed solutions have been presented at the CDR-1 [3].

A set of four scintillators are foreseen at each WS location. Taking advantage of the outstanding EMC performance of the optical fibers, in the system the OFE has been directly located in the Service Gallery rack. As each scintillator will be provided with two fiber outputs, the OFE has been accordingly designed with eight fiber inputs such that one OFE will serve one WS station. Due to this topology also the back end needs to have 8 inputs; therefore, a modified BE (named BE_{mod}) has been developed to keep the design consistent, to optimize the system cabling and to save also some room in the Service Gallery racks.

1.5. The WS software overview

In order to operate and control the WS ACQ SYS and to efficiently present the acquired data to the machine operator, a set of EPICS routines and control panels have been developed. The software architecture can be split in two layers: the low level, strictly related to EPICS IOC and hardware centric, and the high level, composed of the CSS (Control System Studio) based operator and engineer interfaces focused on human interaction.
The low level is meant to run as close as possible to the acquisition and timing hardware and its corresponding IOC (ADC + Timing) acts as data and timing software generator. When the wire scanner IOC runs on the same CPU board of the “ADC + Timing” IOC, the data exchange between them is performed in the best communication conditions. The operator interface, on the other and, can run in any hosting system able to support CSS and network connection. It is then in charge of Channel access protocol to connect the low level (EPICS IOC layer) with the high level one (human interface). A network connection is also used to communicate with the motion controller in charge of mechanical axis displacement.

1.6. WS ACQ SYS Cabling

The design of the WS ACQ SYS cabling is part of the ST IKC to ESS. Given the distributed nature of the WS ACQ SYS, the low level of the involved analogue signals and the pretty noisy environment, typical for a proton accelerator, special care has been devoted to the study of the signal path and cabling related issues, from the in-vacuum wire up to the service Gallery racks.

A blend of tri-axial, co-axial and shielded twisted pair connectors and cables have been adopted, to optimally suit the signal integrity requirements at each specific location.

Frequent contacts have been established with the WS mechanical design Team, mainly with the ESS-Bilbao one, as well as with the ESS cabling and installation Teams.

The cabling system design covers from the WS up to the diagnostic rack in the service gallery; the layout of the WS racks is presented in the next chapter of this document, whereas the detailed description of the WS cabling and its interfaces is given in the specific interface document.

2. WS ACQUISITION SYSTEM DESCRIPTION

2.1. The Analogue Front End (AFE) module

The main purpose of the AFE is to convert the ultra-low current generated in the wire into a voltage. This voltage is then transmitted to the acquisition system at long distance, outside the machine tunnel. As the wire is very thin and may break up during operation, a wire integrity check is also required. A Trans impedance Amplifier (TIA) is implemented in the AFE to perform I to V conversion. Due to the very high required input current dynamic range, two TIAs sharing the same signal have been adopted, each one with a different gain and each one connected at one wire end. By doing so, both a large input dynamic range and the wire integrity check have been obtained. To check the wire integrity, a small current pulse is injected, on request, at one wire end and then it is measured on the other end. The AFE contains two identical stages, one to manage the vertical wire and one to manage the horizontal one.

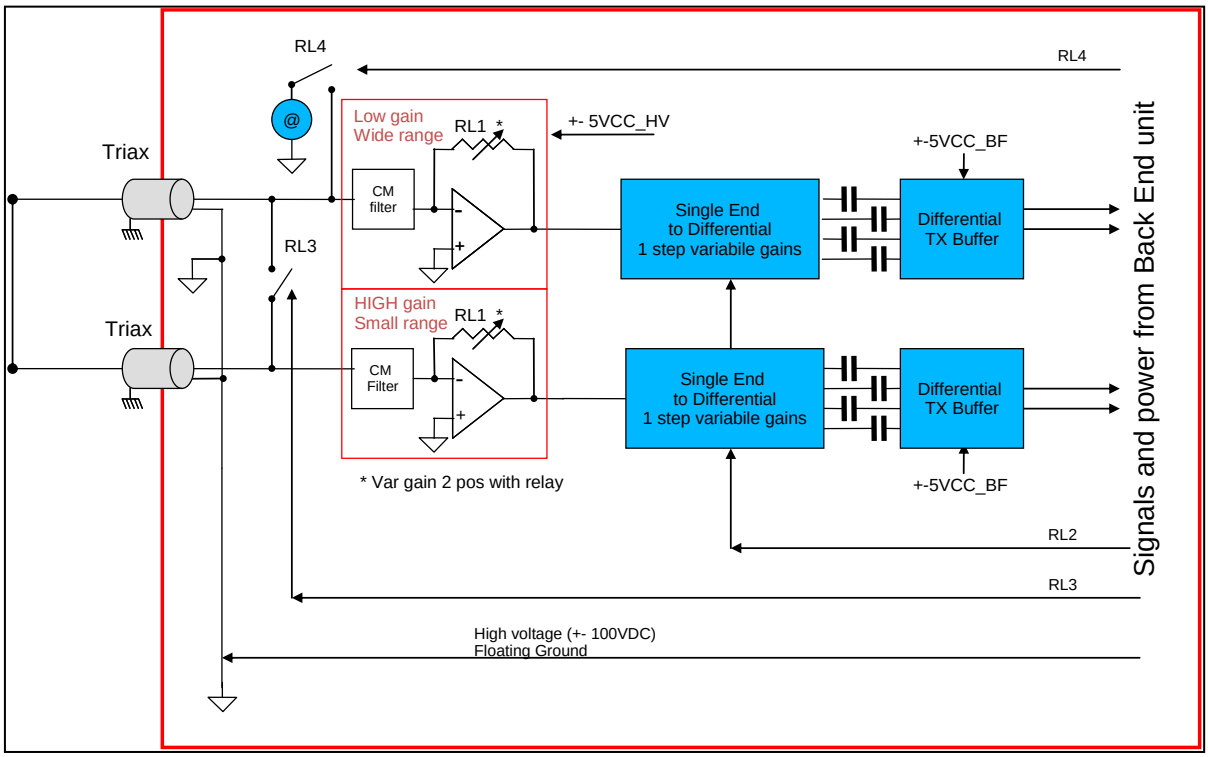

Figure 4: simplified block diagram of the AFE

To improve the measurement signal to noise, an adjustable wire polarization, at +/- 100V DC with respect to the ground of the vacuum chamber, is needed. All power supply voltages of the AFE board are generated in the Back End module. This solution also allows us to minimize the number of power components used inside the tunnel, subject to radiation.

The power supply required by the AFE is +/- 5V DC. In order to be able to adjust the wire voltage, a floating mass has been provided in the Back End, referenced by two supply voltages for the first amplification stage, the TIA and the first differential buffer. Thus, the signal from the first differential buffer is AC coupled to the second differential buffer by means of high-capacity / high-voltage capacitors.

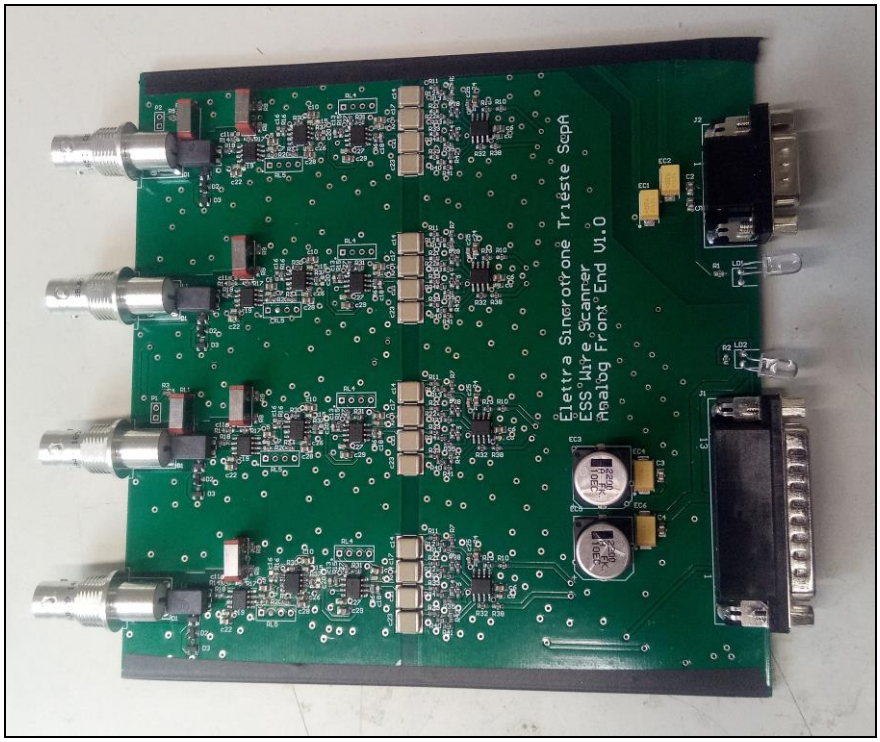

Figure 5: AFE printed circuit board (PCB)

This means that the AFE circuit manages signals in AC and not in DC, thus eliminating the need to subtract the background in the acquisition software.

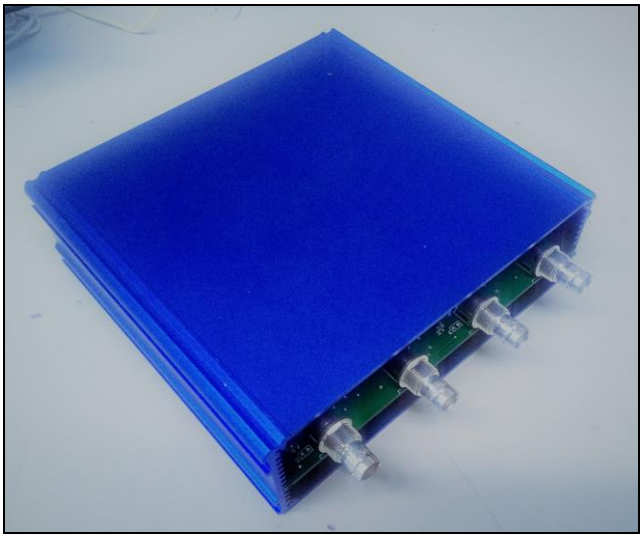

Figure 6: the AFE module

Two input signal ranges are provided, depending on which WS is the AFE connected to. The first range is 50nA to 500µA and the second, more sensitive, goes from 10nA until 20µA. Since the two ranges are remotely and independently selectable for each amplifier, a combination of the ranges is possible to cover the full scale, from 10nA to 500µA. Some performance loss may occur at the intersection region, where the two amplifiers are both linear.

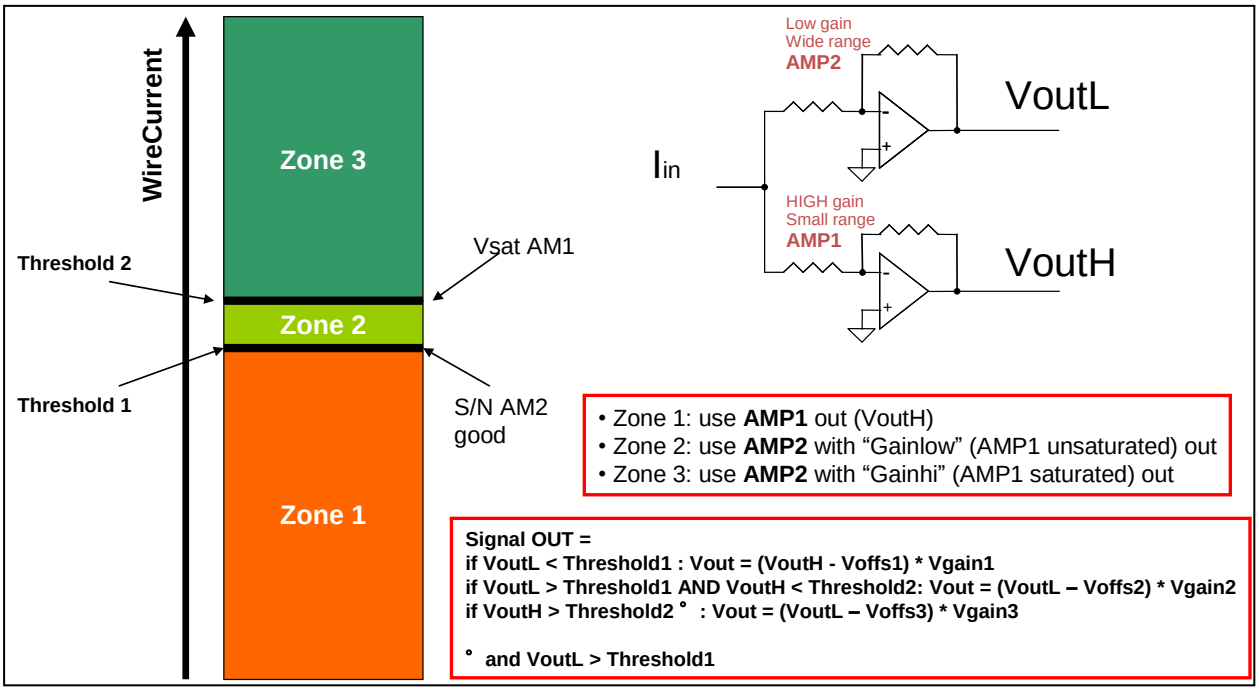

Figure 6: representation of the intercept concept adopted on the AFE

The gain of each amplifier is determined by two resistors, thus an appropriate range can be easily selected/changed in any moment simply changing one or two resistor per input channel. Actually we selected two ranges:

	from	to
AMP1 Range in high gain mode:	10nA	1µA
AMP2 Range in high gain mode:	700nA	50µA
AMP1 Range in low gain mode:	50nA	50µA
AMP2 Range in low gain mode:	40µA	500µA

Table 3 – AFE amplifier ranges

The specifications of the Analogue Front End (AFE) are listed in table 4.

Parameter	Value	Symbol	Notes
Input channel	4	I_Wi; i=1...4	Tri-axial
Max Input Voltage	3VAC	I_W_{MAX}	Input diode protected
Max Input Current	N/A	I_W_{MIN}	
Input Impedance	50 ohm	Z_{IN}	Not well matched
Bandwidth	2MHz	BW_{AFE}	
Output channel	4	$OUT_{AFE}i$	Balanced twisted pair
Minimum Gain	1V/400µA	G_{MIN}	V / A
Maximum Gain	1V/1µA	G_{MAX}	V / A
Power supply	+/- 5 V @ **50mA MAX**	I_{supply}	via BE cable
Dimension	170 x 160 x 54		mm
Weight	400 g		

Table 4 – AFE specification Table

2.2. The Optical Front End (OFE) module

The Optical Front End (OFE) is presented in this section. The OFE is an 8-channel module used to convert into electrical signal the light pulses coming from the scintillator located close the WS, in the machine tunnel. The OFE is conveniently located in the service gallery as the light from the scintillators propagates up to the service gallery in optical fibers. In figures 7a and 7b the OFE front panel and back panel, respectively, are presented.

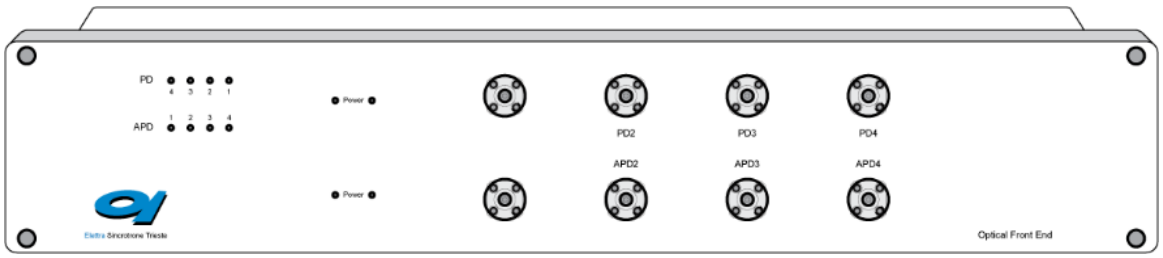

Figure 7a: front panel of the OFE

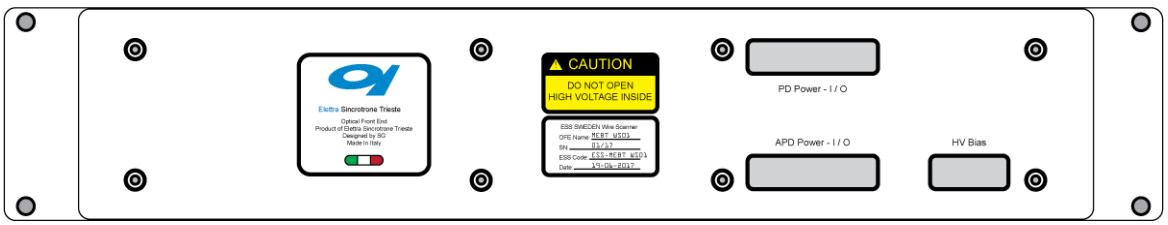

Figure 7b: back panel of the OFE

2.2.1. OFE electrical Specifications

In this paragraph, the electrical specifications of the OFE are listed below.

- Low-voltage noise JFET-input stage
- Power supply -5V to +5V
- High Gain Bandwidth Product 1.6 GHz
- High Bandwidth 275 MHz
- Slew Rate 700 V/µs
- Operating Temperature Range –40°C to 85°C
- Low-Input Offset Voltage ±250 µV
- Low-Input Bias Current 2 pA
- Low-Input Voltage Noise 4.8 nV/√Hz
- Input noise current 1.8 pA/√Hz
- High-Output Current 70 mA

2.2.1.1. Si photodiode Hamamatsu S1226-44BQ

A Hamamatsu Si photodiode is used to detect the light from the scintillator; it is the type 226-44BQ:

- Photo sensitivity area 3.6 x 3.6 mm
- Operating temperature -20 to +60 deg. C
- Spectral response range 190 to 1000 nm
- Peak sensitivity wavelength 720 nm
- Photosensitivity 0.36 A/W
- Dark current 10 pA
- Terminal capacitance 500 pF

2.2.1.2. Avalanche Si photo diode (APD) Hamamatsu S5544

A second Hamamatsu avalanche photodiode is used to detect the light from the scintillator; it is the type S5544:

- Photo sensitivity area diameter 3.0 mm
- Operating temperature -20 to +60 deg. C
- Spectral response range 200 to 1000 nm
- Peak sensitivity wavelength 620 nm
- Photosensitivity 0.42 A/W
- Dark current typ. 1 nA; max. 30 nA
- Terminal capacitance 120 pF
- Break down voltage typ. 150V; max. 200V

2.2.1.3. OFE Power Supply

The following supply voltages are used on the OFE provided by the BE.

- Main power supply (BE_{mod}) -5V / +5V
- Main current max -100 mA / +200 mA
- Bias High Voltage (BE) 0 V to +120V DC

These voltages are all generated by the BE_{mod}.

2.2.2. Trans Impedance Amplifier (TIA) design

To design a good current-to-voltage converter may not be a trivial task. A photodiode produces either a current or voltage output from exposure to light. The OFE trans-impedance amplifier (TIA) is utilized to convert this low-level current to a usable voltage signal and the TIA often needs to be compensated for proper operation. The OFE voltage feedback amplifier with photodiode and capacitances is illustrated in fig. 8.

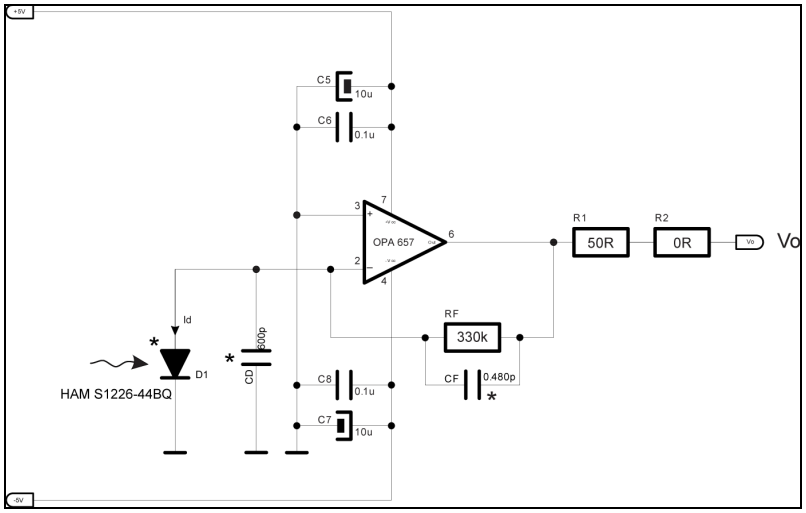

Figure 8: OFE voltage feedback amplifier

The OPA657 allows operation of a low-light intensity due to its low-input bias current by using larger values of gain (RF). The total capacitance (CT) on the inverting terminal of the op amp includes the photodiode capacitance (CPD) and the input capacitance (CIN). The CT plays an important role in the stability of the circuit. The noise gain (NG) of this circuit determines the stability, and is defined by:

$$NG = \frac{1 + sR_f(C_T + C_f)}{1 + sC_f R_f} \quad (1)$$

Where: $f_z = \frac{1}{2\pi R_f C_T}$ (2)

$$C_T = C_{PD} + C_{IN} \quad (3)$$

Figure 9 shows the BODE plot of the noise gain intersecting the op amp open-loop gain (AOL). With larger values of gain (RF), CT and RF create a zero in the transfer function. At higher frequencies, trans impedance amplifiers could

become inherently unstable as there will be excess phase shift around the loop.

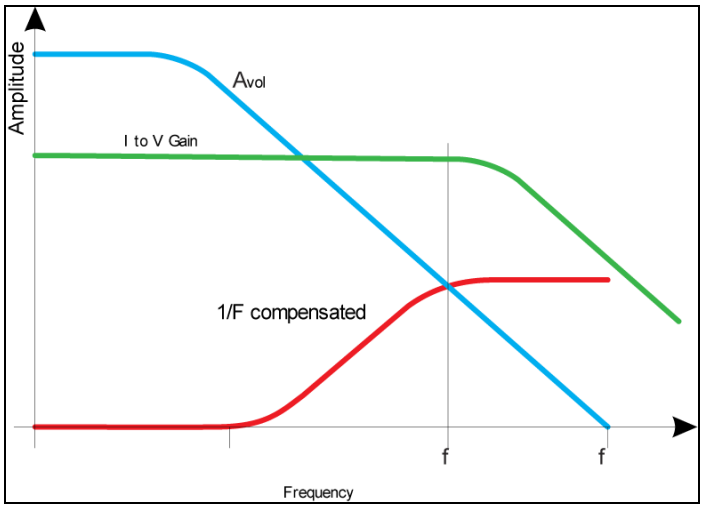

Figure 9: BODE plot of OFE TIA

To maintain the stability, a feedback capacitor (CF) across RF is placed to create a pole at f_p in the noise gain function. The noise gain slope will be flattened by an appropriate value of CF for the optimum performance, such that noise gain is equal to the open loop gain of the op amp at fp. This "flattening" will result in a phase margin (PM) of 45°. Because at the point of intercept, the noise gain pole at fp will have a 45° phase lead contribution that gives PM of 45°.

Equations 1 and 2 calculate the optimum value of CF and the expected -3 dB bandwidth:

$$C_F = \sqrt{\frac{C_T}{2\pi R_F (GBW)}} \qquad (1)$$

$$f_{-3dB} = \sqrt{\frac{GBW}{2\pi C_T R_F}} \qquad (2)$$

Equation 2 indicates that the -3 dB bandwidth of the TIA is inversely proportional to the feedback resistor therefore the best approach would be to have a moderate TIA gain stage followed by a broadband voltage gain stage. Following this recommendation, we obtain for the selected Si Photo diode:

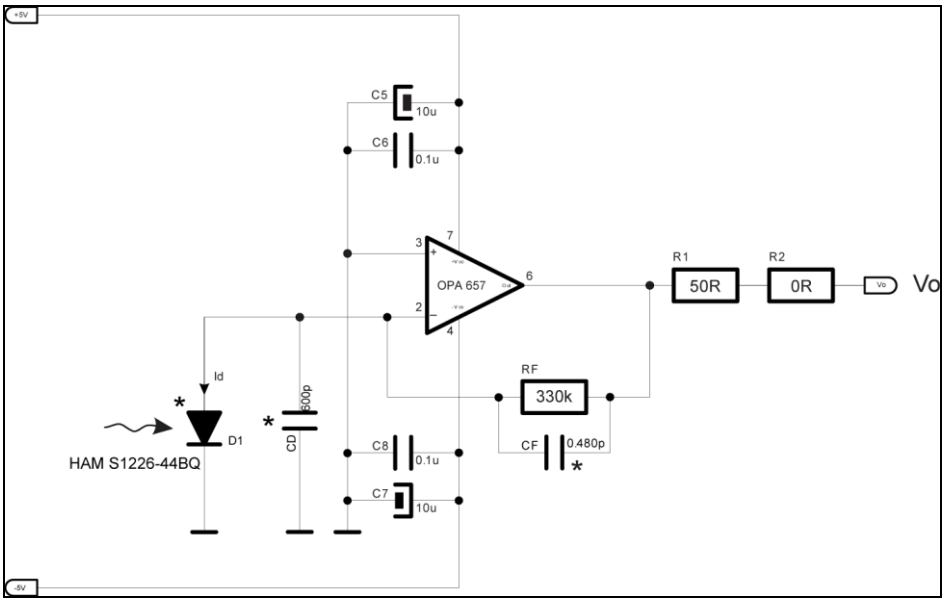

Figure 10: OFE TIA for Si photodiode

with:

- Cd = 500pF
- RF = 330k
- CF = 0.5pF
- f-3dB = 1.4 MHz

For Si APD diode:

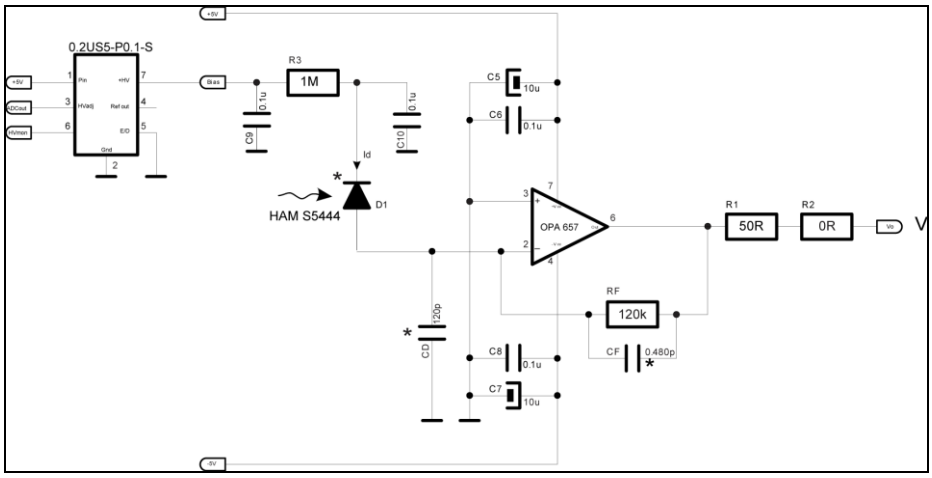

Figure 11: OFE TIA for APD photodiode

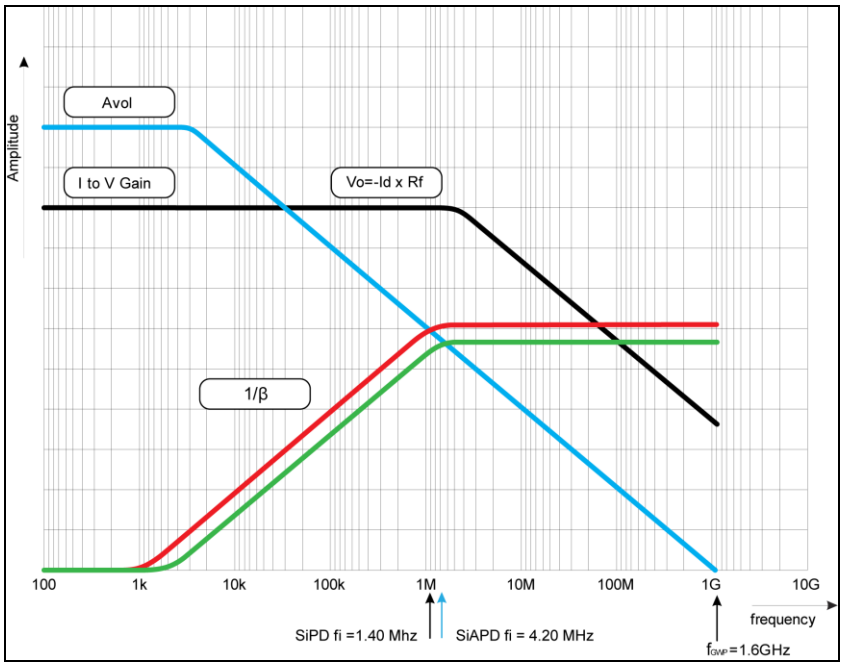

Figure 12: OFE TIA BODE plots with OFE actual values

It is essential to take into account various noise sources. Op amp noise voltage, feedback resistor thermal noise, input noise current, and photodiode noise current do not all operate over the same frequency range while analyzing the noise at the output of the TIA. The op amp noise voltage will be gained up in the region between the noise gain's zero and its pole. The higher the values of R_F and C_T, the sooner the noise gain peaking starts, and therefore its contribution to the total output noise will be larger.
To summarize, the total capacitance (C_T) plays an important role in the stability of the TIA and, therefore, it is advantageous to minimize C_T by proper op amp choice.

2.2.3. OFE Printed Circuit Boards (PCB)

The Printed Circuit Board developed for the OFE is shown in fig. 13, a and b.

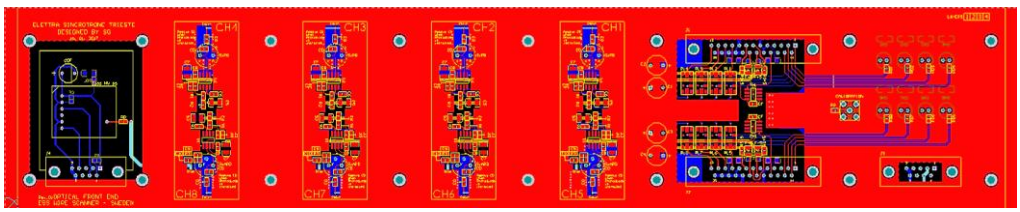

Figure 13a: OFE PCB, solder side.

Figure 13b: OFE PCB, component side.

2.2.4. OFE mechanical Specifications

- Aluminum milled body case
- Mechanical dimension 19 inch 1U rack mount,
- case W-483mm H-88mm D-50mm
- Weight 1.9 kg

In the following figures, 14 to 17, some views of the OFE parts and OFE assembled are presented.

Figure 14: OFE prototype mechanical parts, front view.

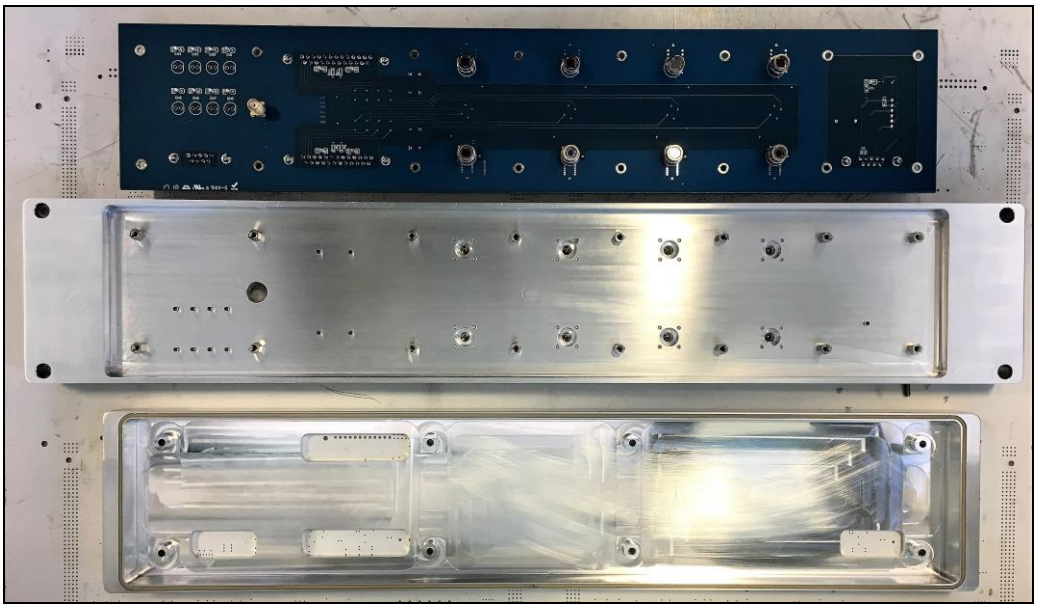

Figure 15: OFE prototype mechanical parts, back view.

Figure 16: OFE assembled prototype, back panel

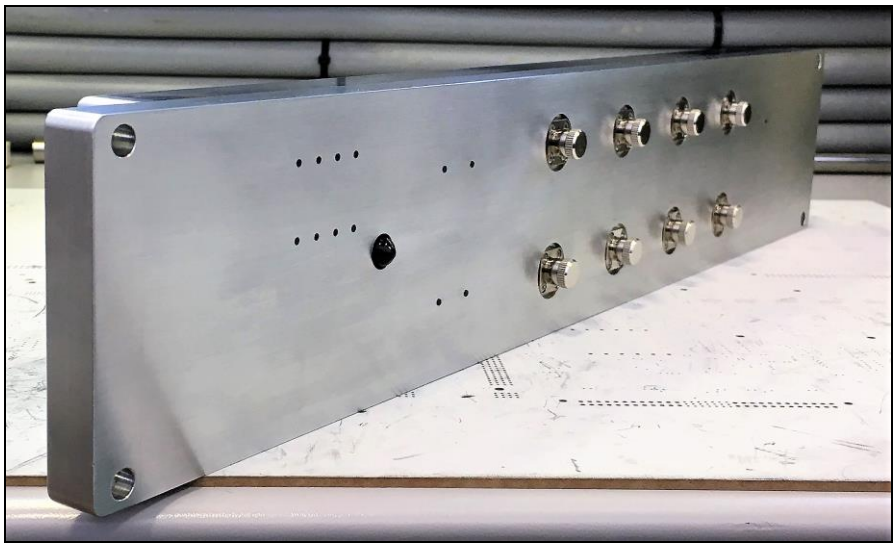

Figure 17: OFE assembled prototype, front panel

2.3. The Back End and Modified Back End modules

In order to interface the front end modules to the digital acquisition part of the system, dedicated back end modules have been developed. Actually, due to the different number of analogue channels managed by the AFE (4) and the OFE (8), two different type of BE have been developed: the BE (used with the AFE) and the BE_{mod} (used with the OFE).
Both BEs are also providing both the supply and the programmable biasing voltages to the respective FE. Some control lines have been also fitted to set the gain level at its most suitable level.
Both BE types are located in the service gallery in the racks used for the WS system.

The Back End is a 2U 19” rack mount module used to manage the AFE and OFE modules. It performs the following functions:

- +/- 5VDC power supply for AFE, non-floating ground
- +/- 5VDC power supply for AFE, floating ground
- High Voltage +/- 100VDC or 0-120VDC, at low current, generator for wire polarization for AFE and/or optical receivers bias for OFE
- Four $_{differential}$ input +/-5V to +/- 1V single end/buffer translator
- Current buffers to drive AFE/OFE relays
- PIC μ-controller (with Ethernet interface) to integrate into ICS, with the following tasks:
  a) Relays control
  b) High voltage set/read

Two versions of BE module have been developed to cope and optimize the general WS ACQ SYS layout and module count. The original BE module is a 4 channel unit and it is used with the AFE. The Modified Back End module has been developed for the OFE, which is an 8 input channel module. Therefore, a second four differential input +/-5V to +/- 1V single end/buffer translator has been added to it. The block diagram of the BE and of the BE_{mod} is shown in figure 18.

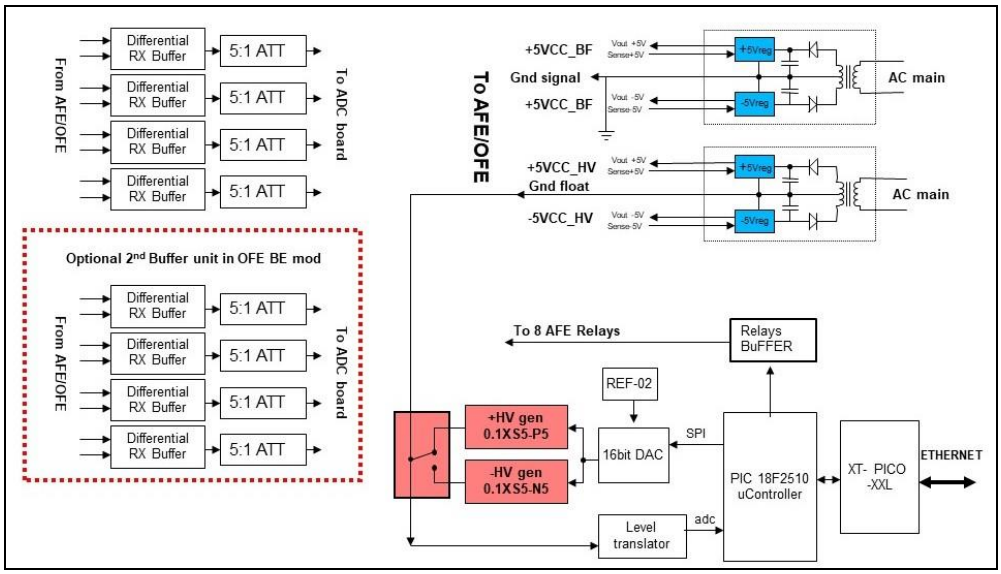

Figure 18 Back end and Modified Back End block diagram

2.4. The WS ACQ SYS cable system

The WS ACQ SYS uses a rather complex cabling and interconnection system, due to several reasons like:

- electrical and optical modules
- long distances between modules
- to assure the highest EM immunity
- to transmit the information signal outside the machine tunnel

In the following paragraphs, all different types of cable are presented divided per machine sections.

2.4.1. MEBT WS cables

From ---> TO	Number	Cable	Connector
WS ---> AFE	12	Triaxial	Triaxial
AFE ---> BE	3	DSTP	DSUB9_F-M
AFE ---> BE	3	DSTP.	DSUB25_F-M
BE ---> ADC	12	coaxial	SMA_M-M
MCTRL ---> WSA	3	DSTP	Souriau_F-M
MCTRL ---> WSE	3	DSTP	DSUB9_F-M
MCTRL ---> WSL	3	DSTP	DSUB9_F-M
LAN ---> BE	3	Eth. CAT6	RJ45
LAN ---> uTCA	2	Eth. CAT6	RJ45
LAN ---> MCTRL	1	Eth. CAT6	RJ45
Power ---> Units	8	Power cord	*VDE_F

Table 5: MEBT cable list

Notes

- DSTP - Double shielded twisted air,
- Eth. Cat6 – Ethernet cable CAT6,
- F-M = Female – Male type of connector
- * ***European*** VDE; ***European standard*** 3-pin power plug; Certificate: VDE; Rated current & voltage: 16A/250V; Applicable cable & cord: H05VV-F 3G0.75-1.5; Number of cores: 3

All other cable information in WS cable and connection table.xlsx by J. Norin.

2.4.2. SPOKE WS cables

From ---> TO	Number	Cable	Connector
WS ---> AFE	12	Triaxial	Triaxial
AFE ---> BE	3	DSTP	DSUB9_F-M
AFE ---> BE	3	DSTP.	DSUB25_F-M
BE ---> ADC	12	coaxial	SMA_M-M
MCTRL ---> WSA	6	DSTP	Souriau_F-M
MCTRL ---> WSE	6	DSTP	DSUB9_F-M
MCTRL ---> WSL	6	DSTP	DSUB9_F-M
LAN ---> BE	3	Eth. CAT6	RJ45
LAN ---> uTCA	2	Eth. CAT6	RJ45
LAN ---> MCTRL	1	Eth. CAT6	RJ45
Power ---> Units	8	Power cord	*VDE_F

Table 6: SPOKE cable list

Notes: as previous paragraph

2.4.3. ELLIPTICAL WS cables

From ---> TO	Number	Cable	Connector
WS ---> AFE	16	Triaxial	Triaxial
AFE ---> BE	4	DSTP	DSUB9_F-M
AFE ---> BE	4	DSTP	DSUB25_F-M
BE ---> ADC	16	Coaxial	SMA_M-M
SCINT ---> OFE	32	Silica core Opt Fiber	APC
OFE ---> BE_{mod}	4	DSTP	DSUB9_F-M
OFE ---> BE_{mod}	8	DSTP	DSUB25_F-M
MCTRL ---> WSA	8	DSTP	Souriau_F-M
MCTRL ---> WSE	8	DSTP	DSUB9_F-M
MCTRL ---> WSL	8	DSTP	DSUB9_F-M
LAN ---> BE+ BE_{mod}	8	Eth. CAT6	RJ45
LAN ---> uTCA	5	Eth. CAT6	RJ45
LAN ---> MCTRL	2	Eth. CAT6	RJ45
Power ---> Units	20	Power cord	*VDE_F

Table 7: ELLIPTICAL cable list

Notes: as previous paragraph

2.4.4. A2T WS cables

From ---> TO	Number	Cable	Connector
WS ---> AFE	4	Triaxial	Triaxial
AFE ---> BE	1	DSTP	DSUB9_F-M
AFE ---> BE	1	DSTP	DSUB25_F-M
BE ---> ADC	4	coaxial	SMA_M-M
SCINT ---> OFE	8	Silica core Opt Fiber	APC
OFE ---> BE_{mod}	1	DSTP	DSUB9_F-M
OFE ---> BE_{mod}	2	DSTP	DSUB25_F-M
MCTRL ---> WSA	2	DSTP	Souriau_F-M
MCTRL ---> WSE	2	DSTP	DSUB9_F-M
MCTRL ---> WSL	2	DSTP	DSUB9_F-M
LAN ---> BE+ BE_{mod}	2	Eth. CAT6	RJ45
LAN ---> uTCA	1	Eth. CAT6	RJ45
LAN ---> MCTRL	1	Eth. CAT6	RJ45
Power ---> Units	5	Power cord	*VDE_F

Table 8: A2T cable list

Notes: as previous paragraph

2.5. The WS ACQ SYS control software

The simplified block diagram of the Wire Scanner In-Out Controller (WS-IOC) to be used whit the AFE is reported in figure 19 below, contoured by the green line.

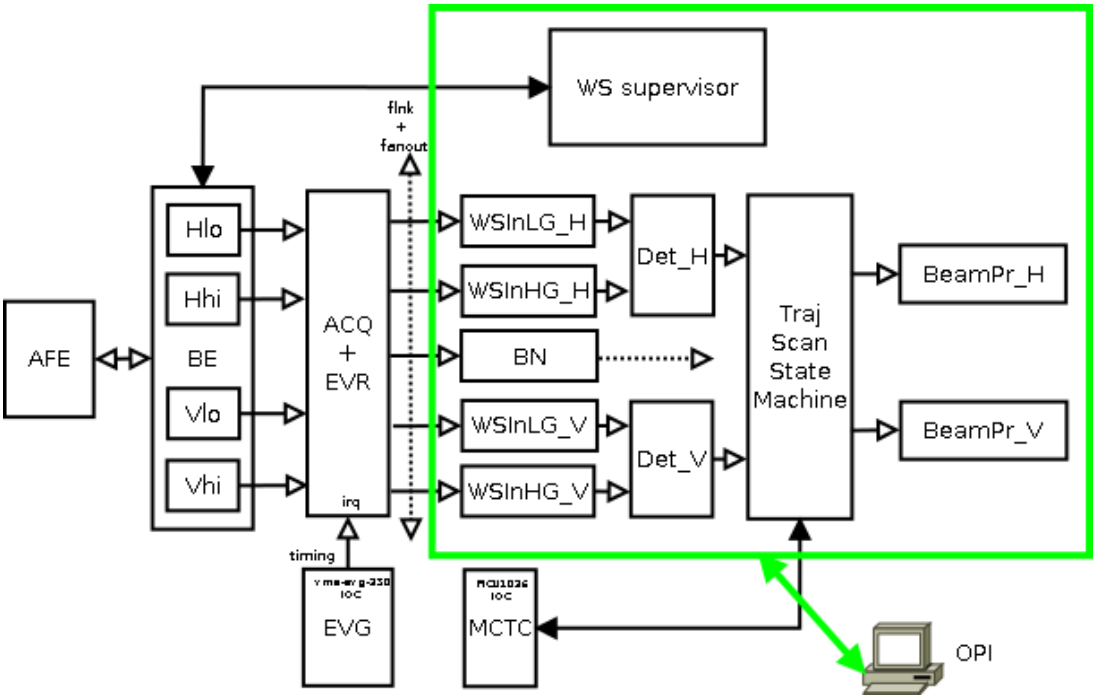

Figure 19 Block diagram of the WS IOC

Triggered by the cascade action of the EVG (event generator) and a dedicated EPICS forward link (FLNK), the data generated by the “ACQ + EVR” IOC are fed to the inputs of the WS-IOC that, accordingly to a data flow approach, elaborates it stage by stage up to the calculation of the H and V beam profiles.

The benefit of the data flow model is that the required cascade of actions (data fetch, data calculation, data forwarding), performed at each stage of the elaboration pipeline, are triggered only when the previous stage has been executed. By doin so, the synchronization required between the different records that form the WS-IOC is automatically obtained by cascading the records and the forward links involved in the pipeline.

Considering that the motion controller is not synchronized with the EVR (and even worse it isn't directly connected to the ADC sub system), a state machine has been added whose main task is to manage the mechanical trajectories.

In order to supervise the operation of the WS-IOC an extra block has been introduced outside the pipeline: the WS supervisor. Its main task is to periodically check both the internal operating status of the WS-IOC and the error

states/anomalies of the external communication channels (motion controller, triggers, BE, …).

The most critical task that is performed by the WS-IOC that works with AFE is to switch between the High Gain and Low Gain signals when the high gain channel saturates; this switching feature is not required in the OFE version of the WS-IOC.

The figure 20 below shows the simplified block diagram of the WS-IOC to be used whit the OFE (2 scintillators are indicated):

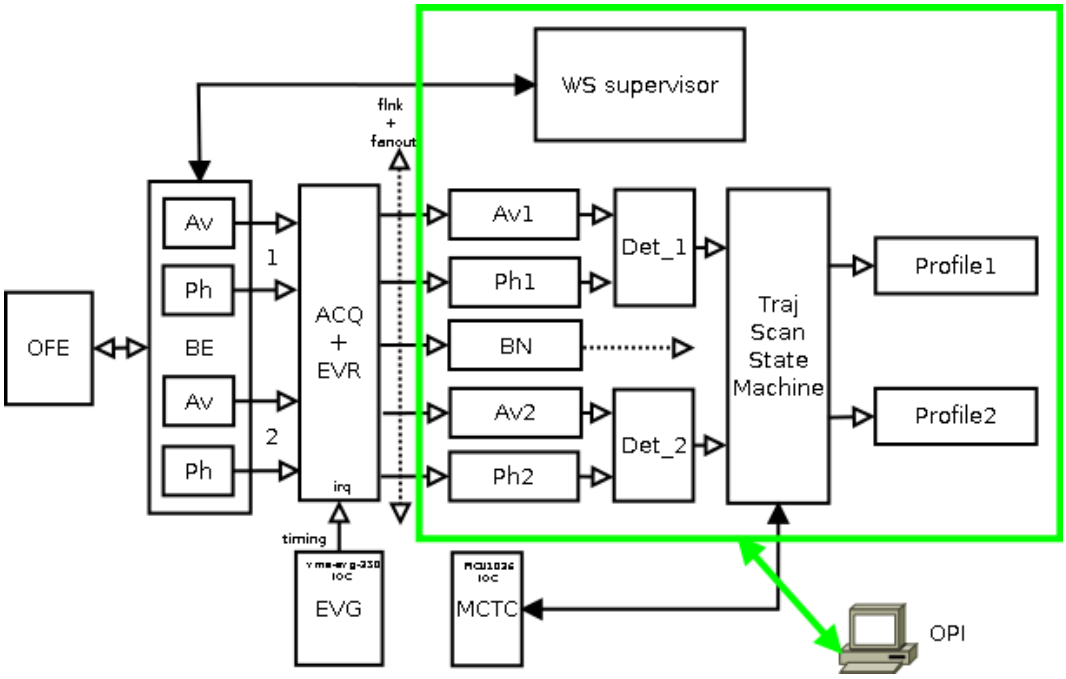

Figure 20: Block diagram of the WS IOC developed for the OFE

2.6. The WS ACQ SYS data processing algorithm

The data processing pipeline can be divided in the following cascaded steps:

1. once an IRQ has been triggered by the EVR a complete set of ADC buffers (10 channels for the SIS8300 board) is processed by the “ACQ + Timing” IOC. At the end of the processing a forward link (Channel Access type) trigger signal is sent to the WS-IOC (“xxx:PropagateHWtriggerHV.PROC” - BE CAREFUL: the name could change over the time);
2. the Process Variable “PropagateHWtriggerHV” inside the WS-IOC triggers a fanout record that processes the following PVs:
    a. "$(user):TrigSeqNum" - counter value of the triggering event;
    b. "$(user):WSInHG_V" - High Gain Vertical input buffer
    c. "$(user):WSInHG_H" - High Gain Horizontal input buffer
    d. "$(user):WSInLG_V" - Low Gain Vertical input buffer
    e. "$(user):WSInLG_H" - Low Gain Horizontal input buffer

even in this case the PVs name and scan mechanism could change over the time

3. once all the buffers and the event counter have been acquired, the vertical and horizontal selecting records are triggered by dedicated forward links located in the input buffers records. The main goal of this stage is to detect which input array is saturated (this stage could be named “detect and select array”). Saturated means that a configurable number of elements of the array are greater than a configurable threshold inside a configurable region of interest.
4. If neither the HG array nor the LG array is saturated, the HG array will be propagated. If the HG array is saturated, instead, the LG one will be processed in order to be correctly scaled and then propagated. If the LG array saturates a warning indicator is turned on but the processing pipeline isn't stopped. If LG saturation occurs, the gain of the input stages (AFE/OFE) could be too high. At the end of this processing stage a forward link (one per plane) triggers the next stage.
5. this is the stage that calculates the significative parameters of the previously selected array that are, basically, areas identified by specific algorithms (e.g. RMS, mean, ABS) and parameters that can be set by the operator interface. Once the outputs are calculated, a forward link triggers the process responsible of the creation of the profile.
6. the beam profile is built in two different manners depending on the type of scan required: Step By Step (SbS) or On The Fly (OtF). The SbS case is fully driven by a state machine in order to scan a precisely defined set of axis positions; in each of them, furthermore, a number of beam samples can be acquired in order to calculate the mean value of the main parameters. This kind of operation can be summarized as “position driven”. At the end of each scanning step a value is fed in the final buffer, the one that contains the beam profile. This kind of scan could be extremely slow.
7. The OtF mode is only partially driven by the state machine, because its goal is to get a quick indication of the beam shape without stopping in any position of the mechanical trajectory. This scanning mechanism is implemented by a dedicated record that is enabled only when the trajectory starts and that is disabled when the trajectory stops. At each trigger this record outputs a point of the beam profile.
8. This kind of operation can be summarized as “event trigger driven”; the mechanical speed is supposed to be constant over the scansion.
9. The operation of the OFE version of the WS-IOC is in principle the same of the AFE version. The main difference is that OFE doesn't require the discrimination between HG and LG signals and the corresponding saturation detection and switching mechanism.

2.7. The WS ACQ SYS control panels

The WS control panel is split in a set of tabs, each having a specific context, as illustrated in the figures below, 21 to 26. The Tab in figure 21 represents the status of the “ACQ + EVR” IOC. It is put in the panel in case of a rapid check of the underlying hardware/IOC is necessary.

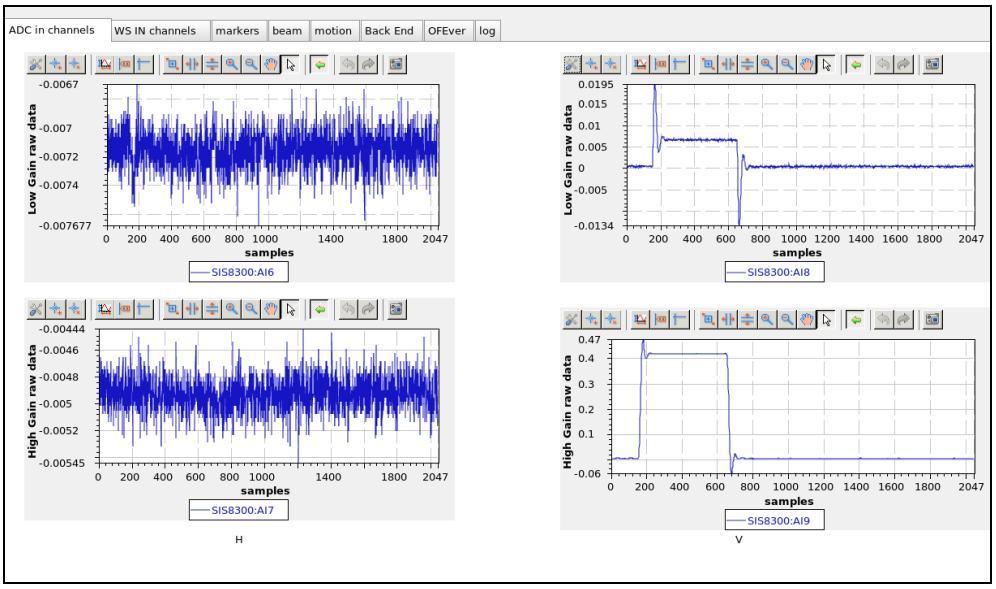

Figure 21: WS control panel tab ADC Channel

The next figure 22 presents the status of the Wire Scanner input channels

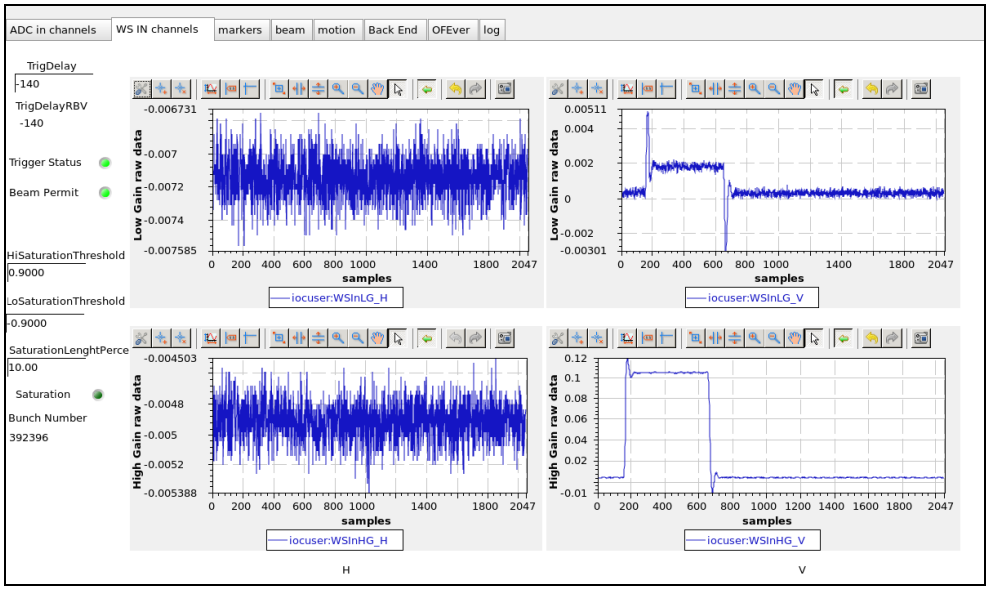

Figure 22: WS control panel input channel tab

The next figure 23 reports the markers used to calculate the beam main parameters on the automatically selected array.

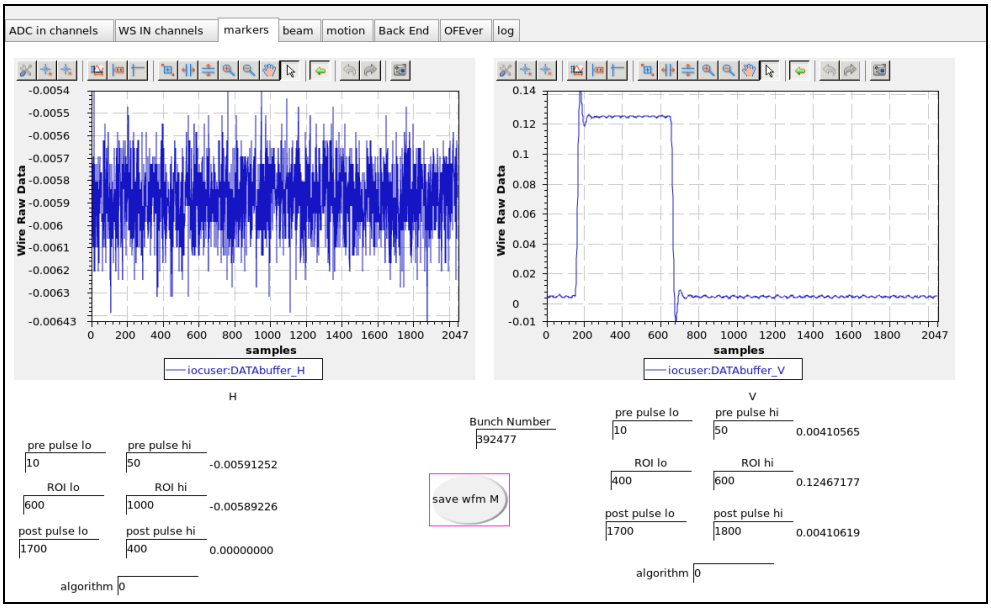

Figure 23: WS control panel main parameter setting tab

A detailed view of the configurable parameters is presented in figure 24.

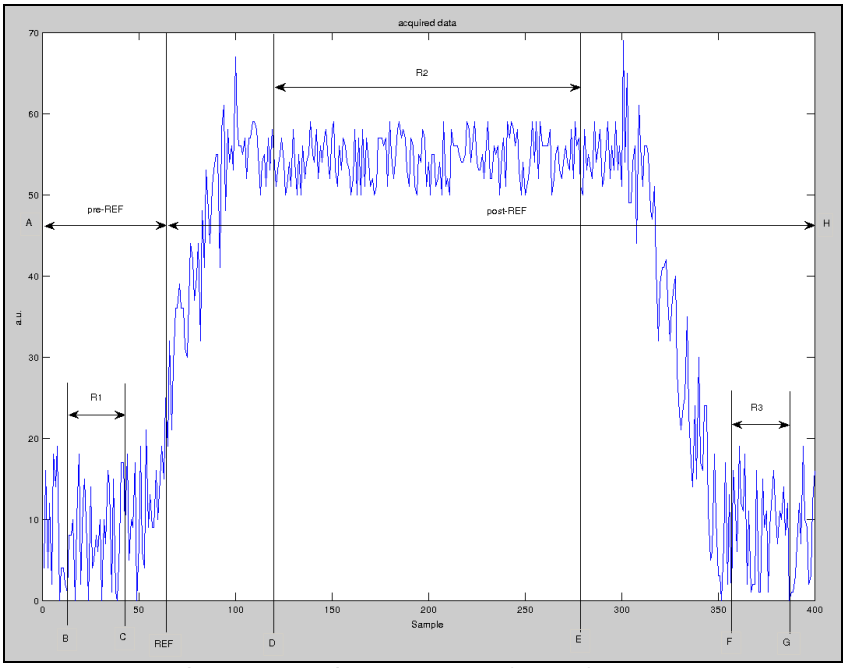

Figure 24: main parameter of waveform

The beam tab shows the final beam reconstructed profile.

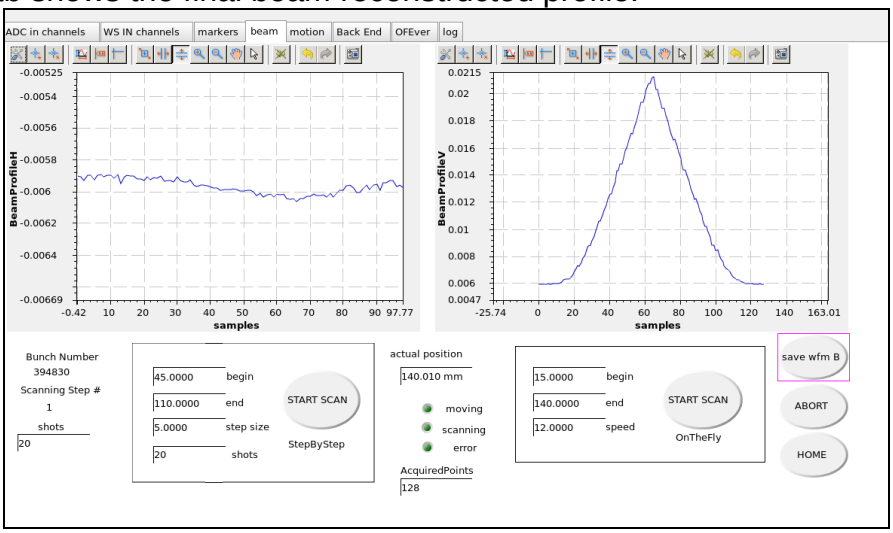

Figure 25: reconstructed profile tab

The BE tab shows the operating status of the Back End (both for AFE and OFE):

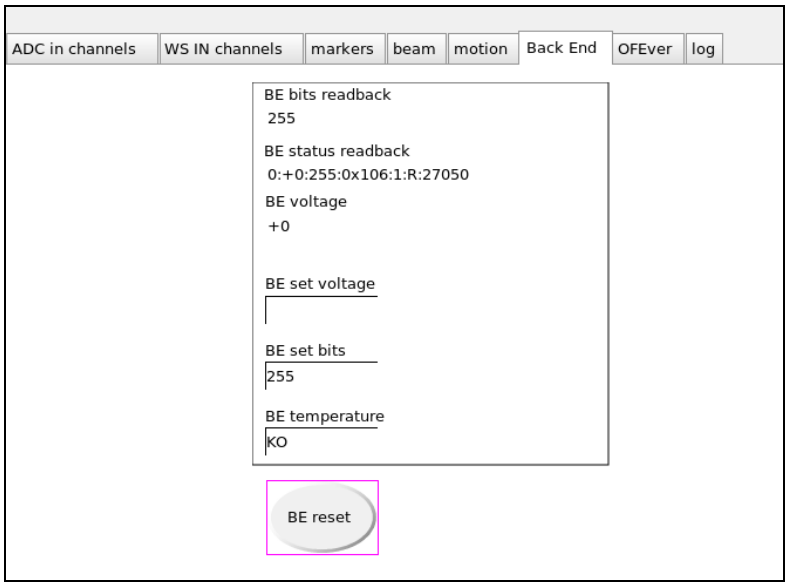

Figure 26 BE status information tab

3. THE WS ACQ SYS PERFORMANCES

In the present chapter we present the laboratory measurements performed to assess the HW module performances.

3.1. AFE laboratory tests

The SEM section of the Wire Scanner Acquisition System is composed of four blocks:

- The wire
- AFE
- BE
- DIGITIZER and SW

The AFE and the BE modules shall be considered as a “single block”. As written above, the BE provides all voltages to the AFE and the control signals. The AFE sends back to the BE the analog signals via a shielded twisted pair cable with electrical levels and impedances that do not compromise the signal even after 120m of cable. Therefore, the electrical characterizations of the AFE has been carried out jointly with the associated BE. The AFE has 4 input signals (4 x tri-axial connectors) while it is provided with a DB9 and a DB25 connectors for power, signals outputs and control signals. The BE provides all supply voltages and the control signals with the following functions:

- to set gain
- to start a wire integrity test
- to set High Voltage offsets

The output signals are transmitted to the BE over a shielded twisted pair cable as they are full differential. The AFE is internally AC coupled, with a high voltage rated capacitors to insulate the wire floating ground, so only AC signals can be acquired. As a result, no DC offsets have to be compensated for.

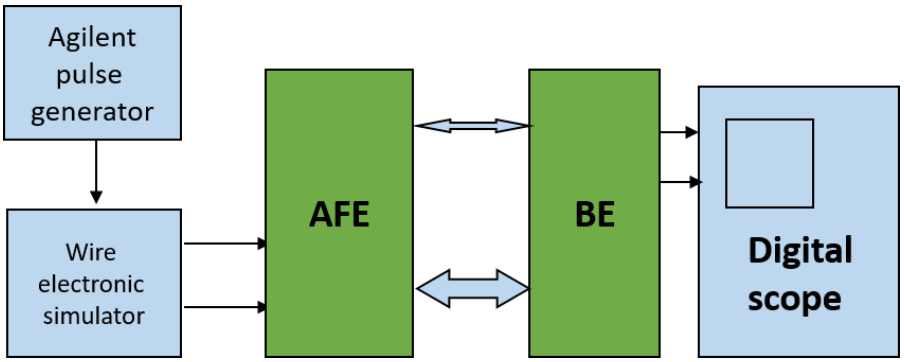

Figure 27 block diagram of the test set-up: DUT=AFE + BE

3.1.1. AFE wire electronic simulator

A specific circuit has been developed (figure 28) to simulate the pulsed current to characterize the AFE with no real wire current. By using an analogue opto-coupler, HCNR201 from HP, small current pulses may be generated using a remotely programmable pulse generator.

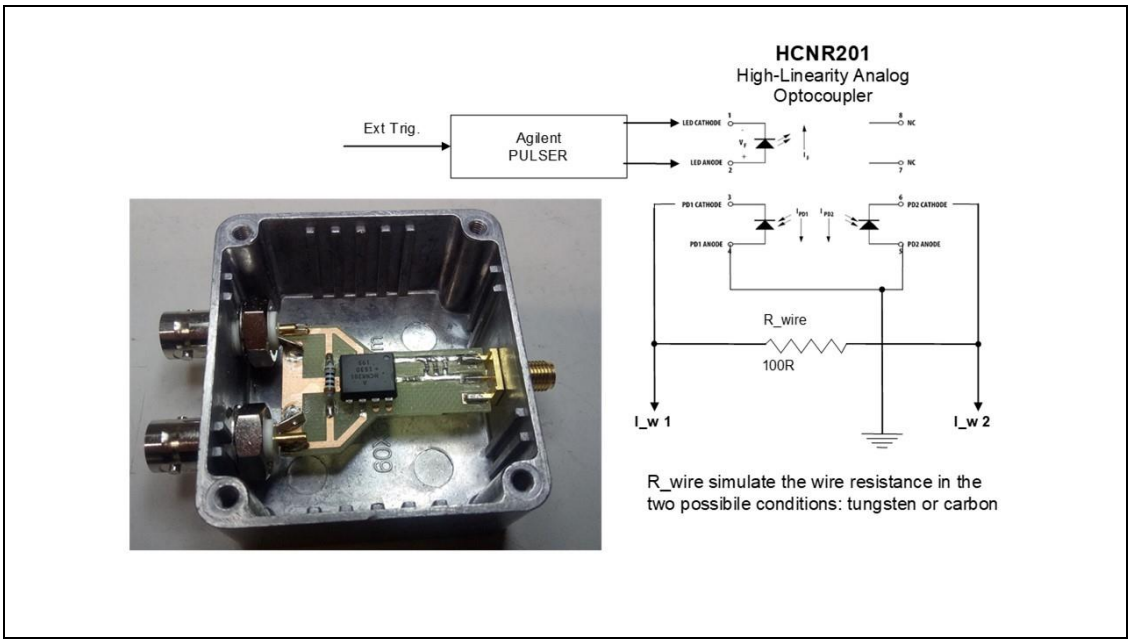

Figure 28: wire electronic simulator: a circuit used to apply symmetric inputs to the AFE inputs, while using a mono polar pulse generator.

3.1.2. AFE input dynamic range measurement

Vpulser HI (V)	Vpulser LO (V)	CURRENT (calibrated at +- 20%)	Relay =1 (LOW) OUT LoGain mV	Relay =1 (LOW) OUT HiGain mV	Relay =0 (HIGH) OUT LoGain mV	Relay =0 (HIGH) OUT HiGain mV
1,165	1,100	10 nA		1		11
1,193	1,100	30 nA		3,8		35
1,206	1,100	50 nA		5,8		61
1,215	1,100	70 nA		8,3	1	93,5
1,225	1,100	100 nA		12,3	3	139
1,256	1,100	300 nA	0,5	37,1	6	434
1,271	1,100	500 nA	1	63,9	10	716
1,281	1,100	700 nA	1,8	88,27	15,3	986
1,294	1,100	1 uA	2	129,5	21,7	1427
1,339	1,100	3 uA	5,2	351	60	2600
1,366	1,100	5 uA	8,3	545	92	4200
1,392	1,100	7 uA	11,5	758	130	4200
1,422	1,100	10 uA	15,2	1010	172	4200
1,589	1,100	30 uA	41,5	2760	380	4200
1,742	1,100	50 uA	70	4200	600	4200
1,879	1,100	70 uA	229	4200	2500	4200
2,089	1,100	100 uA	522	4200	4200	4200
3,547	1,100	300 uA	2600	4200	4200	4200
5,157	1,100	500 uA	4070	4200	4200	4200
7,235	1,100	700 uA	4070	4200	4200	4200

3mV * 2uA	2,5mV * 20nA	3mV * 200nA	30mV * 20 nA
300mV * 20uA		40mv * 20ua	

Table 9 conversion table for the test input circuit with resulting gains (table below).

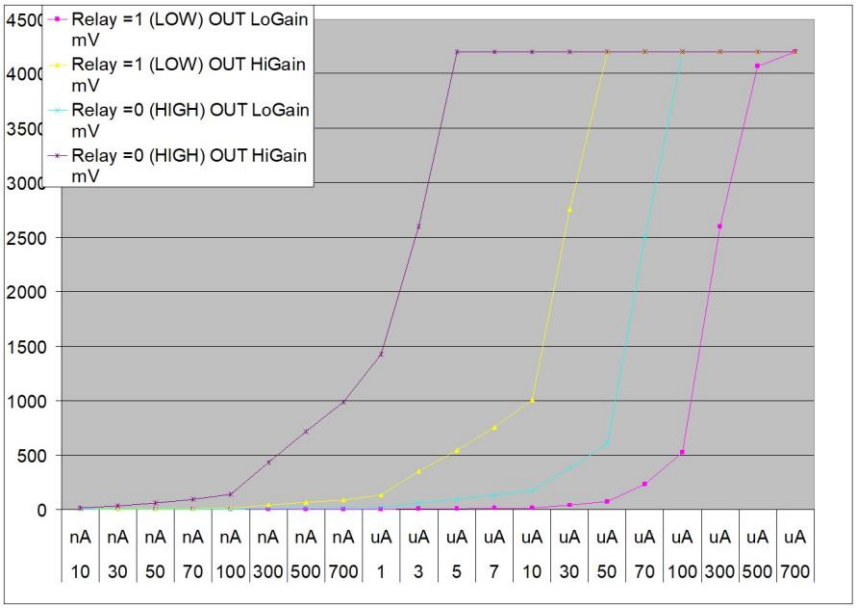

Figure 29: plots V(out) vs. I(in) for all 4 different gain settings

3.1.3. AFE amplifier chain linearity and crosstalk measurement

An un calibrated (means: without direct correspondence with a wire current) voltage signal is applied to an input to characterize the response of the complete amplifier chain and transmission buffers and receivers. The signal amplitude is adjusted such that the output is at its maximum (+/- 4VDC), without attenuators on the BE output to the ADC inputs.

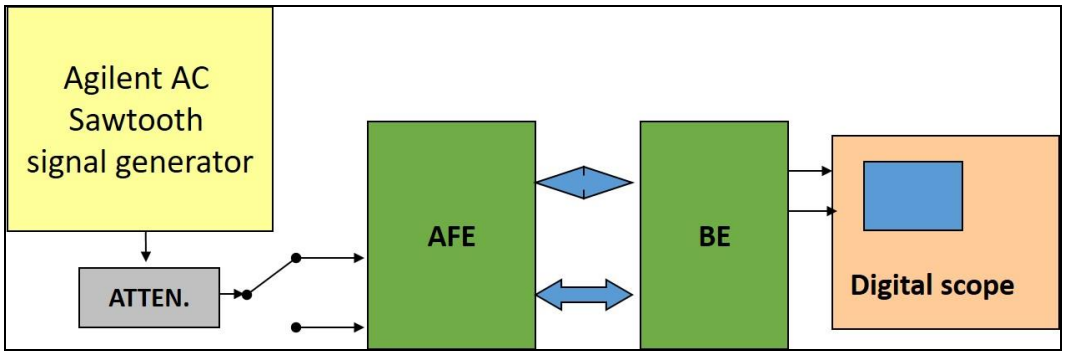

Figure 30: block diagram for the linearity and cross talk measurements

The signal output in CH2 trace is the result of a saw-tooth signal from Agilent directly connected to one of the TIA inputs .

As results an undistorted signal can be read at the end of all of the amplifier chains. In addition, we can notice that there are no or negligible crosstalk between the other channel (note the different scales: **2V** per division and **2mV** per division.

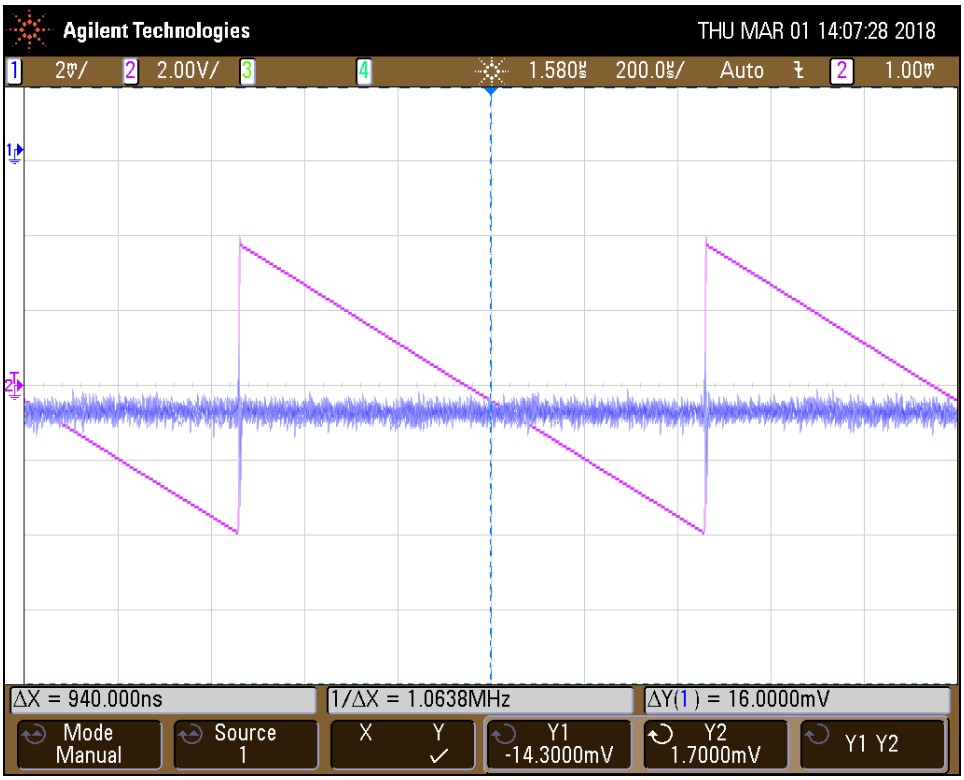

Figure 31 linearity and cross talk characterization of the complete amplifier and transmission line sequence, AFE + BE

All four gain combinations (shown in table below) have been tested; by using this method, it is possible to check all AFE amplifiers of any WS station.

Setting	AFE channel	Gain set to
1	Low gain	LOW
2	Low gain	HIGH
3	High gain	LOW
4	High gain	HIGH

Table 10 possible AFE gain combination

3.1.4. AFE + BE transmission measurement

The AFE signals are transmitted to the BE, by analogue balanced buffers, over a shielded twisted pair cable. Main purpose of this set-up is to preserve the signal integrity while transmitting it over few 100s meters and in a EMC unfriendly environment. Therefore, the transmission capabilities of this channel have been tested in the Laboratory before in-field tests at CERN. In the figures below, the received pulse at the BE output in plot with a short (40cm) and with a long (140m) line.

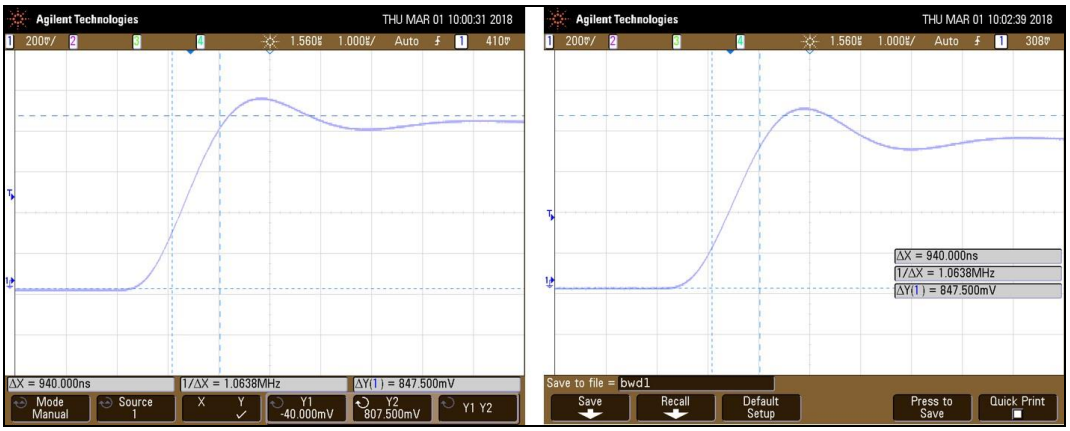

Figure 32 received pulse at the BE output after transmission over
a short (40cm) twisted pair cable (left plot) and
a long cable (140m) twisted pair cable (right plot)

3.2. OFE laboratory tests

With photodetectors used in optical front end we have to detect light which is coming from scintillators in two ways: one for Si photo diode and one for Si Avalanche photo diode. The spectrum of the captured light by scintillator and shifted to wavelength suitable for transport in optical fibers of pure silica core of 1mm diameter to the photo detectors is presented in figure 33.

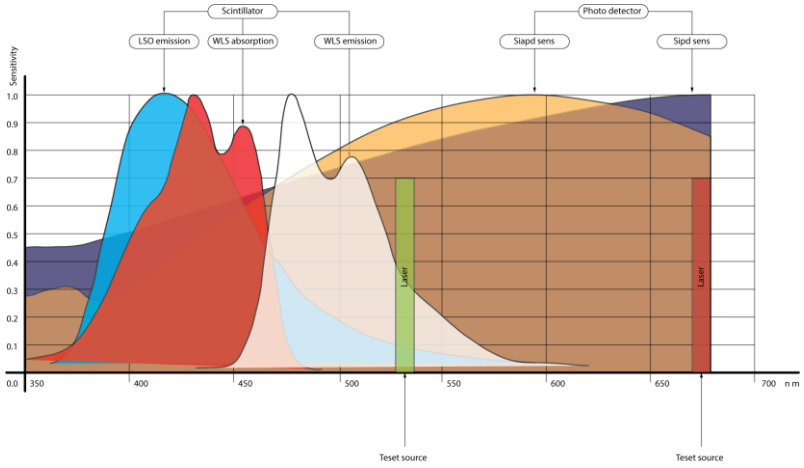

Figure 33: spectra of scintillator generated light and wavelength shifted
to couple the fiber optic for transport

For this test, a laser source with 760nm and 5mW power was used: Thorlabs optics and fibers with power meter and Keithley multi meter. The layout is presented in fig. 16. With laser source and additional optics 1nW light power was delivered to optical front end. At the output of OFE firmly and stable voltage was measured. For delivered 1nW of light power -1.4 mV was measured (figure 34).

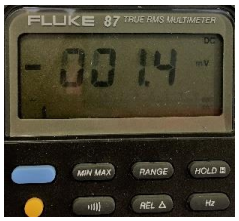

Figure 34: Keithley multi meter read out for 1nW of optical power: -1.4mV

With no source or no light at the input of photo diode stable 0.22nV was registered with Keithley multi meter.

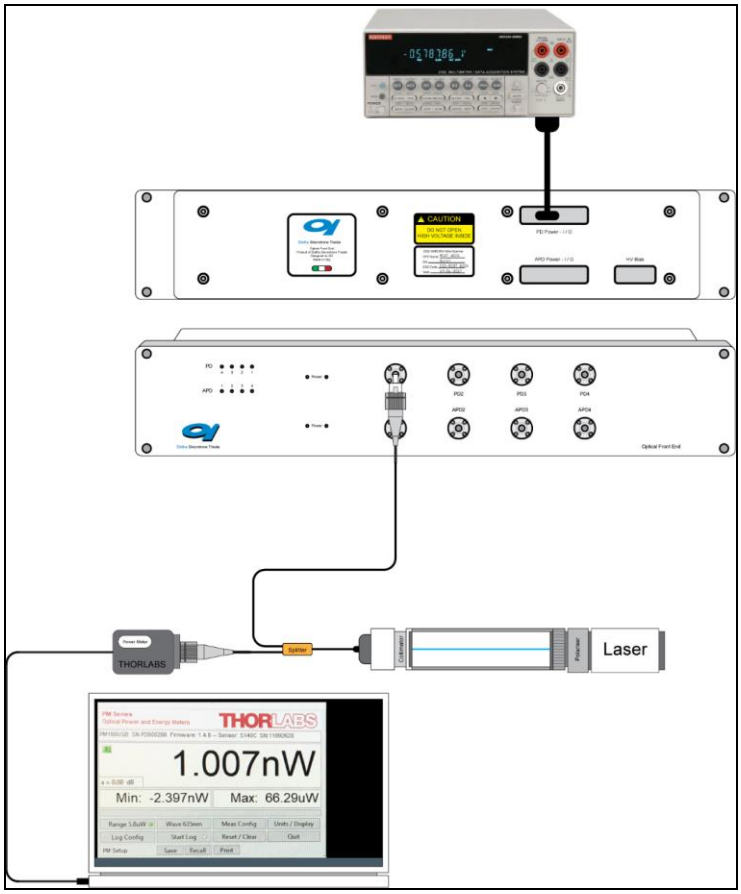

Figure 35: OFE test bench block diagram

In the following Table 11 the characterization results are presented.

Light Power [W]	OFE output [V]
1.00E-09	2.54E-03
1.00E-08	8.16E-03
1.00E-07	8.22E-03
2.00E-07	1.39E-02
5.00E-07	2.29E-02
1.00E-06	2.98E-02
4.50E-05	
5.00E-05	

Table 11 OFE TIA characterization results.

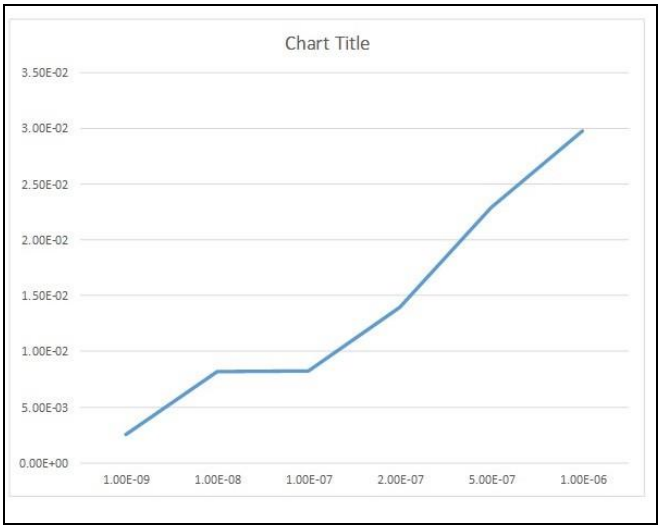

Figure 36: OFE characterization plot

3.3. The vertical integration test (VIT) at ESS

The vertical integration test is intended as a pre-installation verification. It requires all the WS system items to be available and commissioned at a single location and, for the control software, it will make use to the ESS ICS infrastructure. It is a multi-laboratory effort that, most reasonably, has to take place at the ESS where all the WS system items are converging and where the final ESS ICS infrastructure is available. It has to be set-up in an ESS laboratory space to be time efficient, thanks to easier in-situ debugging.

It will be coordinated by ESS staff and it is scheduled to happen by 18 May, 2018.

The hardware items that need to be available are:

- WS mechanics with 1 or 2 (?) axis
- on-board WS patch panels and cables
- WS ACQ SYS with:

  - AFE prototype
  - BE prototype
  - μ-TCA crate with boards (CPU, ADC, EV_Rx)
  - Motion controller
  - OFE prototype
  - BE_{mod} prototype
  - Short WS ACQ SYS cables
  - Control panel
  - Engineering panel
  - Acquired data processing
- Long Run cables (simulated)
- Local Ev_gen with FO output
- Local control PC / WS
- Local PLC to mimic machine safety I/Os
- Pulse generator to mimic beam current
- Diode laser to mimic scintillator light signal
- *anything else we may have forgotten*

A fundamental pre-requisite for a fast and successful vertical integration test is that all the items have been individually pre-tested as standalone units. This statement holds true both for electronics (hardware and software items) and mechanical items.

3.3.1. Vertical Integration Test final output

The final output of the VIT is the synchronous acquisition of both the AFE and OFE inputs while the WS is moving, either in “on the fly mode” or “step by step mode”, while both electrical pulse generator and diode laser are generating pulses of variable amplitude (to mimic the signals generated during a WS scan). Once the scan is over, the FW processes the acquired data and plots the calculated profile.

3.3.2. Possible SW sequence for the vertical integration test

A procedure (see fig.) that, assuming the nominal operation of the underlying components (ADC + Timing IOC, Motion Control IOC, data connections), assures that if all the sub-steps involved in it are passed, then the WS software can be considered validated.

At first, check:

- timing system (EVR is receiving events from the EVG)
- ADC triggered

If so, the IOC called "ADC + Timing" (e.g. SIS8300:xxx and EVR-MTCA:yyy records in the demo IOCs by ESS) will be running and triggering the WS IOC, as indicated by the green led indicated as "Trigger Staus".

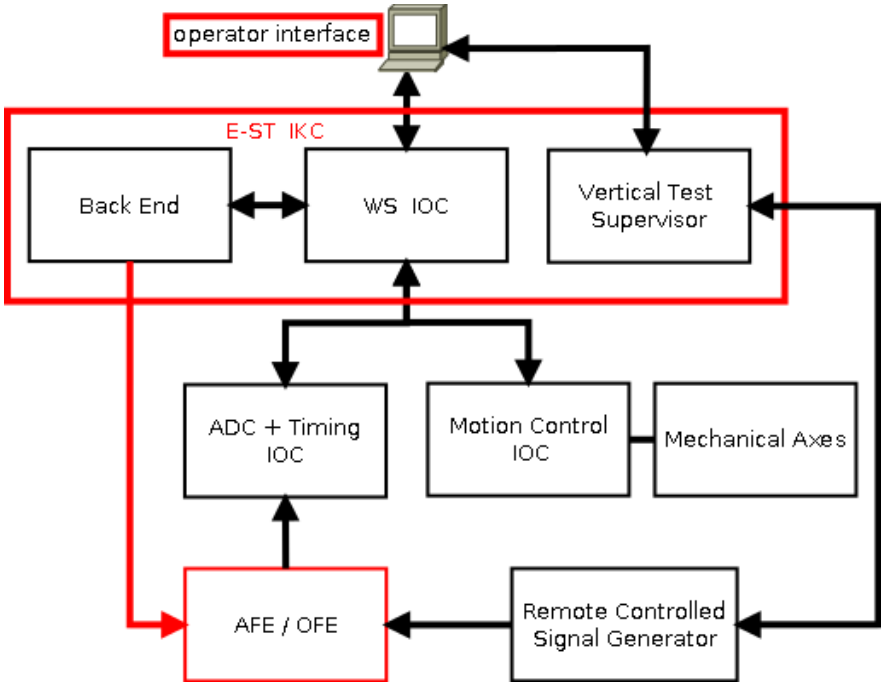

Figure 37 block diagram of the Vertical Integration Test software modules

Then, verify that the motion controller IOC up, initialized (limit sw OK) and running. If so, set accordingly the scan start and stop values in the WS IOC. At this point, the test of the WS IOC can start under the supervision of the "vertical test supervisor" application, responsible for:

- to generate a set of commands to be sent to the WS IOC and to the signal generator in order to simulate a real beam generated currents
- to read back the Process Variables of the WS IOC in order to evaluate if its behavior is compliant to a defined test procedure

The test procedure can be divided in the following steps:

- without acting on the motion subsystem (wire in parking position or equivalent one), check the Back End status
- If BE OK, execute "On The Fly" trajectory and plot processed data
- Then, execute a "Step By Step" trajectory and plot processed data

3.4. Test session at CERN on LINAC4

For the development of the WS ACQ SYS modules and of the associated control software, a fundamental role has been played by the in-field tests of the prototype modules in a real accelerator environment.

The extremely low level of the signals to be detected, the highly EM noisy environment typically found in a proton accelerator together with the fact that some modules need to be installed in the accelerator tunnel, generated some concerns about the EM noise immunity of our systems.

Therefore, we deemed extremely important to carry out these on-field tests to get a final validation of our design and implementation.

Thanks to the availability of the Colleagues at CERN, with particular reference to F. Roncarolo and his co-workers, in the Fall of last year such tests have been successfully carried out on LINAC4.

The test conditions were pretty much similar to the final ones at ESS, in terms of proton energy, accelerator and service gallery layout and size, and of a pretty noisy proton gun.

3.4.1. Measurement set-up and installation

At first, the test has been set-up during a shut-down period of LINAC4 (Oct 2017); a complete WS ACQ SYS prototype has been installed in LINAC4 and connected to the existing long run cables connecting the tunnel to the service gallery.

The hardware installed at CERN included:

- 1 AFE (in tunnel) with associated BE (in the service gallery);
- 1 μ-TCA crate with CPU, ADC board and EV_RX board;
- 1 VME crate with EV_GEN and fiber output to clock the system;
- 1 PC to act as WS ACQ SYS terminal

In the following figure n a block diagram of this installation is shown.

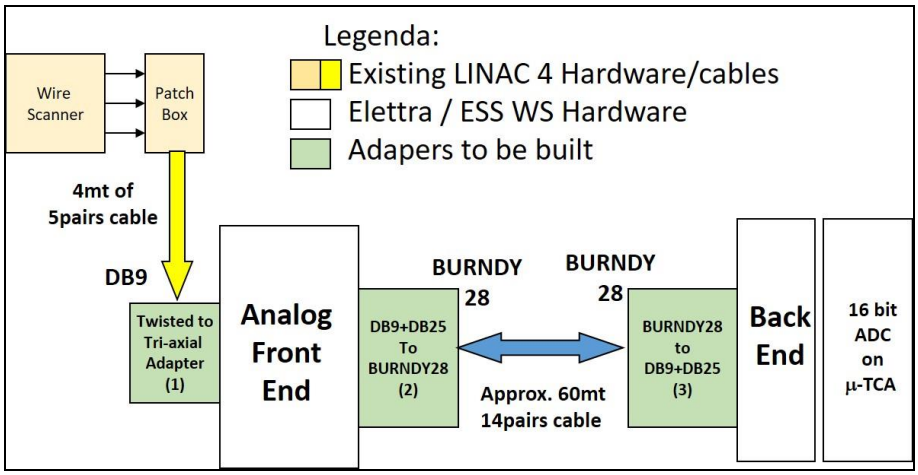

Figure 38: block diagram of the LINAC 4 test stand at CERN;
ad-hoc cables and connectors shown in light green

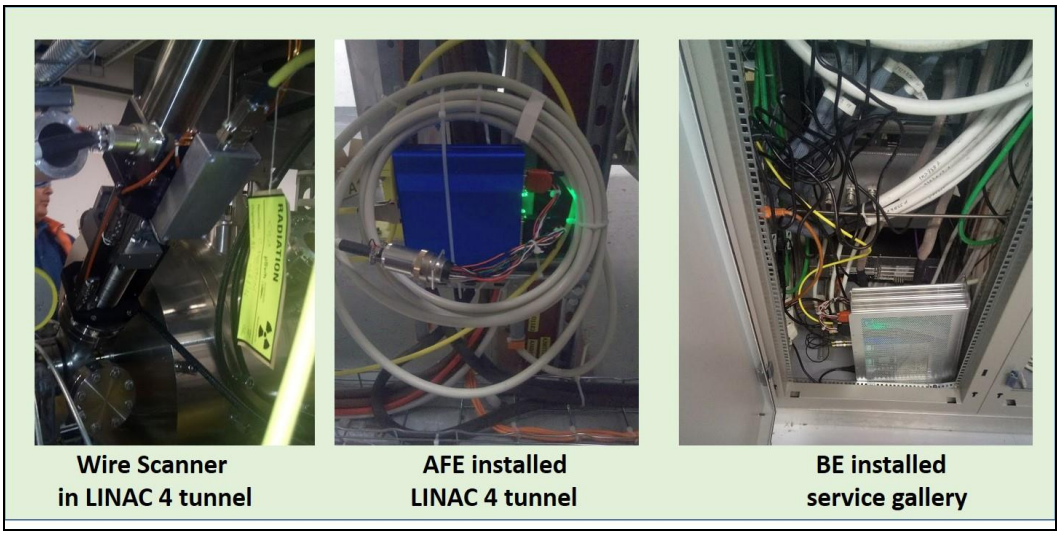

Figure 39: the Elettra hardware modules (AFE+BE)
installed in the LINAC 4 tunnel and in the service gallery

3.4.2. LINAC4 measurement result

In the following figures the main results of the LINAC4 measurements are reported. In figure 40, a typical pulse from the wire is shown.

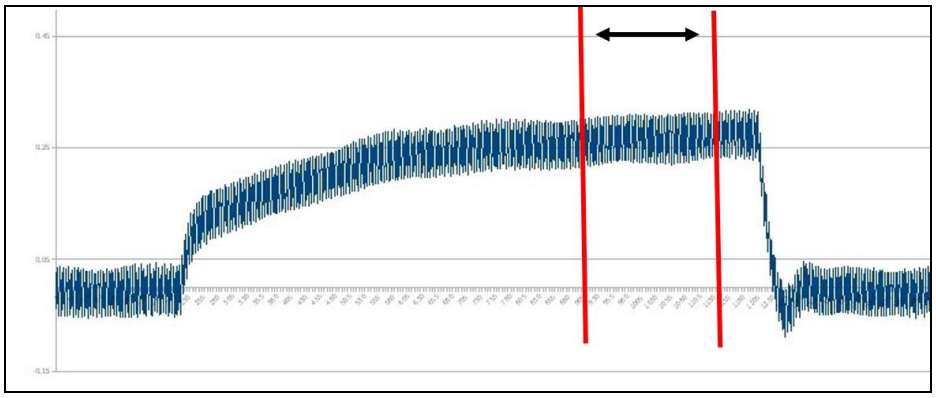

Figure 40 typical single pulse acquired as wire current from wire scanner installed on LINAC4; the vertical bars indicate the good region used for profile computation. The large visible ripple is due to the proton GUN noise and it cancels out being a zero average signal.

To calculate the A.U. value for the beam profile plot we use a simple integral value (sum) of samples from n=900 to n=1100, shown by the two red vertical bars in figure 40. In this zone the samples are less noisy and dispersed than in previous (head) or sub-sequent (tail) parts.

A good idea is to make these parameters configurable in the user interface of the beam profile measurement system.

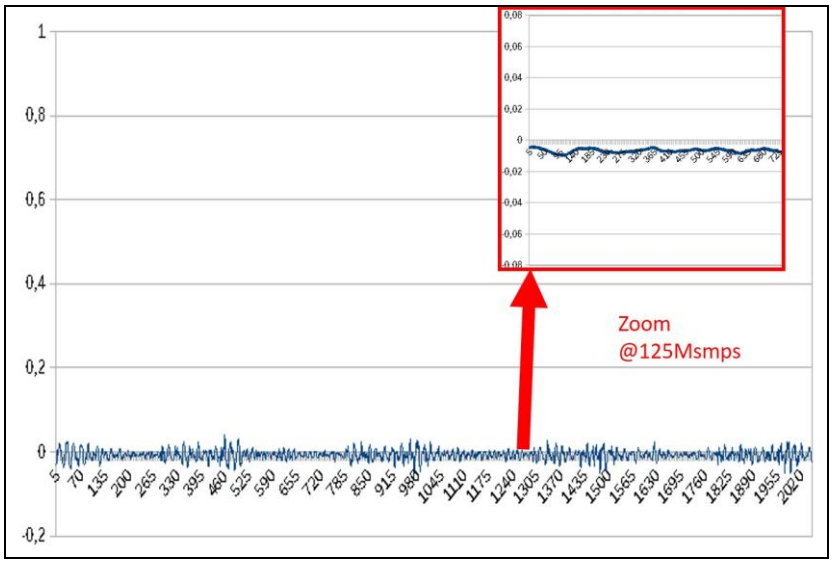

Figure 41: typical acquired signal with proton GUN OFF.

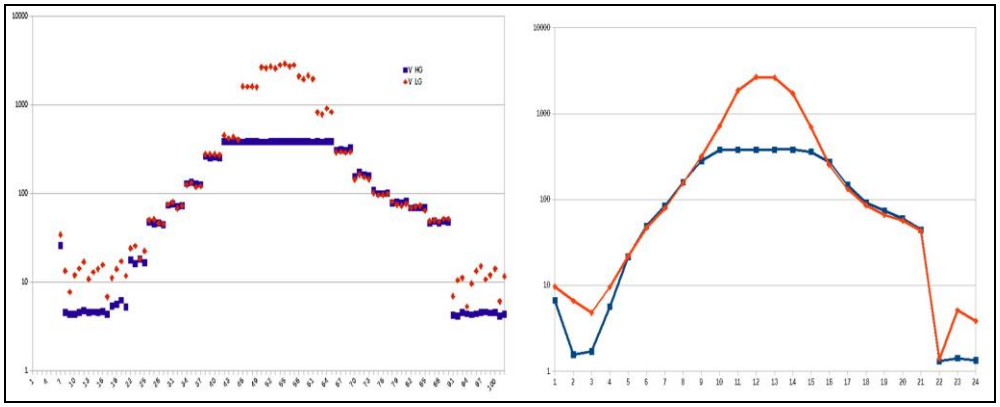

Figure 42: reconstructed profile over multi shots from proton GUN.
Left is single shot, right is averaged.

d

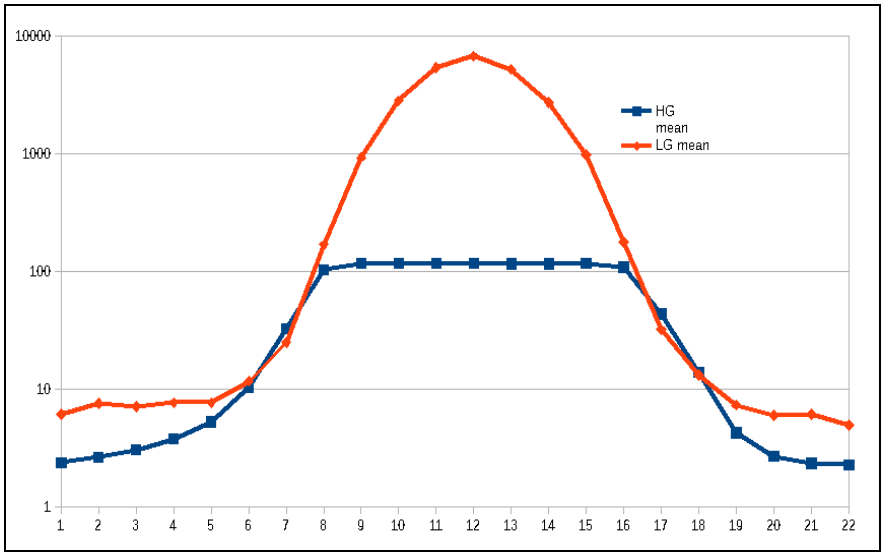

Figure 43: overlapping of the two acquisition channel outputs (LOW gain and HIGH gain).

3.4.3. Observations to the LINAC4 measurement results

A minor fault has been observed in the Back End high voltage part that in certain conditions required a reset (an electrical disturb was affecting a feedback control). It has been now fixed.

In this configuration the input cables with nA signals were multipolar and with unique shielding: a lot of noise was coming from there.

An issue with the EPICS acquisition system has been observed while the debug output was sent thru the network instead of local terminal.

The 2MHz signal seems to be collected by the wires at the input, but in ESS installation the source will be completely different.

- The klystrons noise wasn't affecting too much the measure (less than 1% → 0.01 on +- 1V → 0,1uA). Averaging it out with 100 or more ADC samples can reduce the effect by a factor of 10.
- The working principle of the extended range analog front end has been tested with a real beam and it works as expected.
- The signal cables and all the current detection part should be shielded as much as possible.
- The 2MHz signal coming from L4 source is affecting our measure, but also with this big issue the measurements are possible over a 4 decades range.
- Without this disturb, a factor of 5 will get back.
- A laboratory calibration is possible using the in house developed “wire scanner electronic simulator”.
- An automated calibration procedure, using a programmable pulse generator and our “wire scanner electronic simulator” will be performed to create an complete calibration table that will be used by the software to use as best as possible the combination of the two amplifiers (LO and HI gain).

4. Rack layout for the installation of the WS ACQ SYS

All racks used for the WS ACQ SYS installation are standard 19” racks from SCHROFF company. In the following figures the size of the racks is presented with hardware assembly layout.

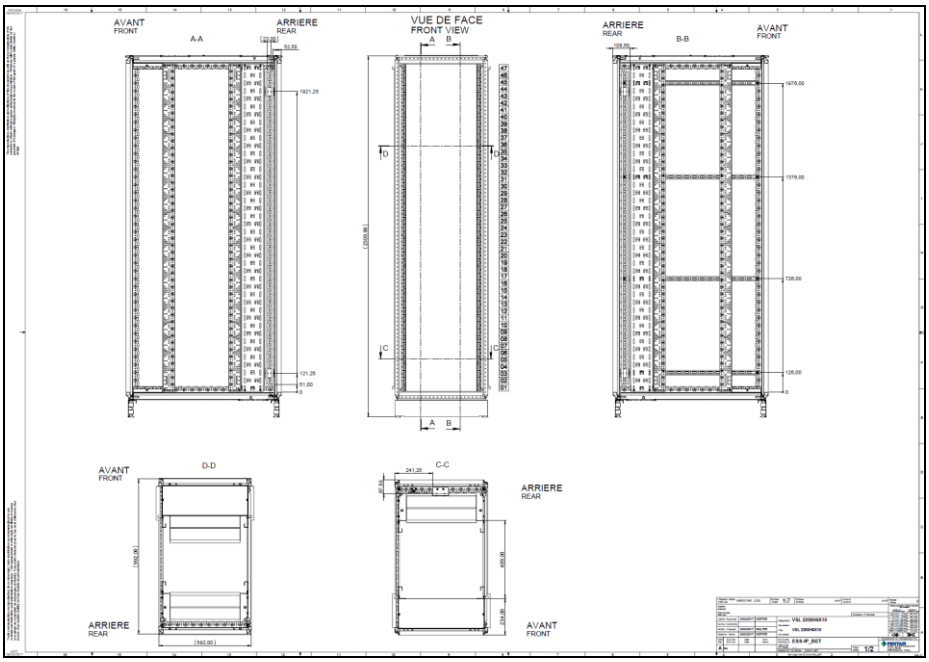

Figure 44 19° rack mechanical drawing

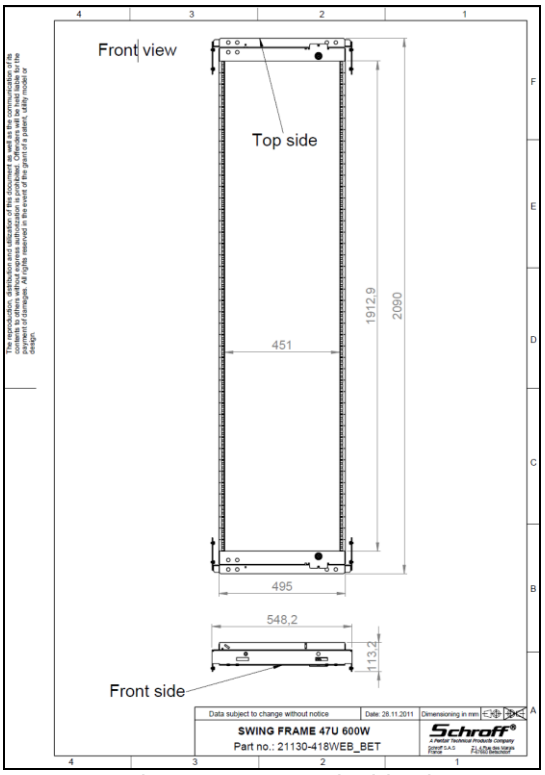

Figure 45: 19° rack side view

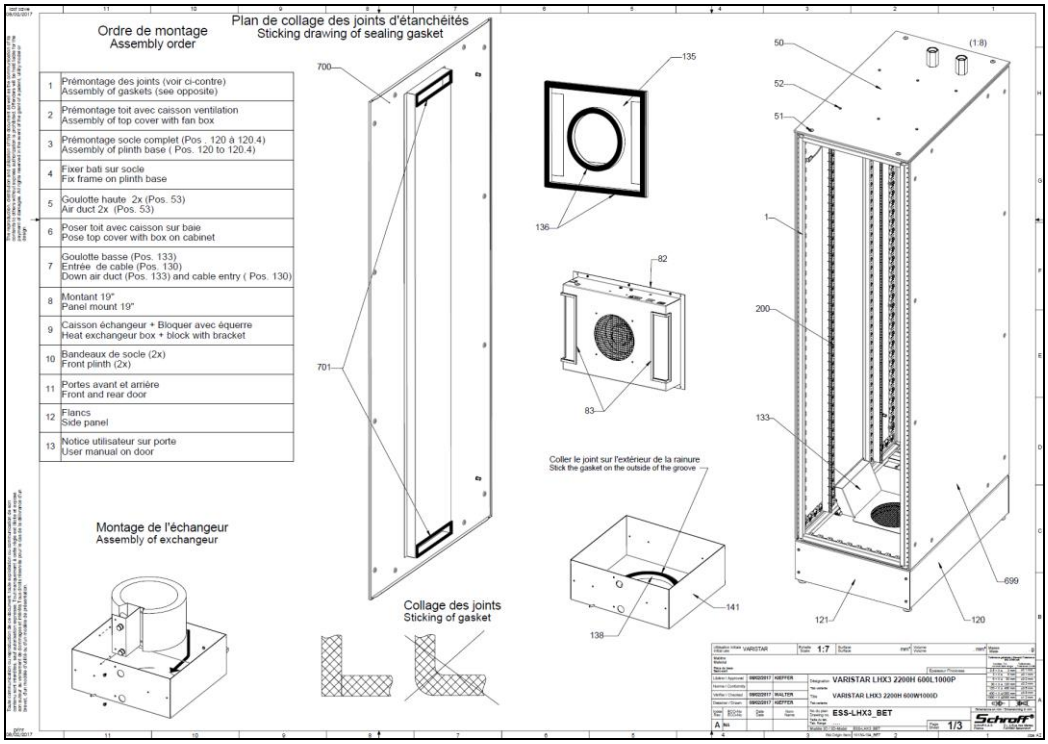

Figure 46: 19” rack fan assembly

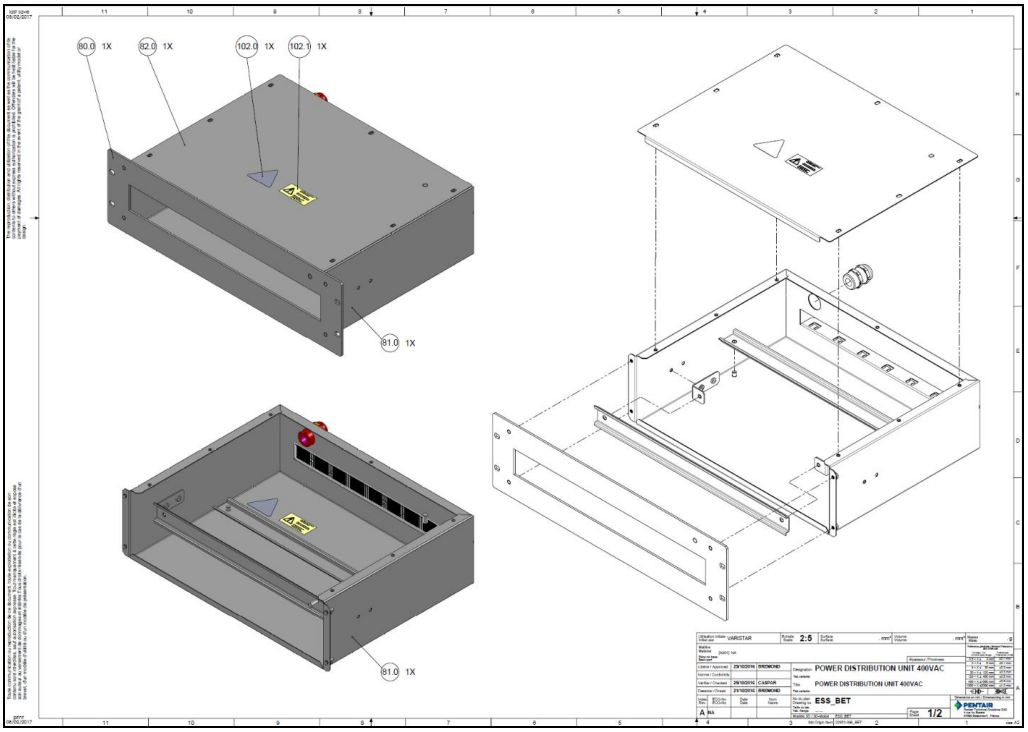

Figure 47: ESS 19” rack power distribution unit

4.1. Layout of WS ACQ SYS racks

In this section the layout of each rack used for the WS ACQ SYS is presented, including front ends and motion controllers

4.1.1. MEBT racks

Layout of the MEBT WS racks:

rack name: **FEB-030ROW:CNPW-U-008**

- BE1 2U
- BE2 2U
- BE3 2U
- uTCA 6U
- LAN switch 1U

Total 13U

rack name: **FEB-030ROW:CNPW-U-008**

- MCTRL 3U
- uTCA 6U
- LAN switch 1U

Total 10U

4.1.2. SPOKE racks

Layout of the SPOKE WS racks:

rack name**: SPK-020ROW:CNPW-U-018**

- BE1 2U
- BE2 2U
- BE3 2U
- uTCA– 6U
- LAN switch 1U

Total 13U

rack name: **SPK-020ROW:CNPW-U-018**

- MCTRL 3U
- uTCA 6U
- LAN switch 1U

Total 10U

4.1.3. ELLIPTICAL WS racks

Layout of the Elliptical WS racks:

Rack name: **MBL-030ROW:CNPW-U-018**

- BE 2U
- BE_{mod} 2U
- OFE 2U
- uTCA 6U
- LAN switch 1U

Total 13U

Rack name: **MBL-030ROW:CNPW-U-017**

- BE1 2U
- BE2 2U
- $BE_{mod}1$ 2U
- $BE_{mod}2$ 2U
- OFE1 2U
- OFE2 2U
- uTCA 6U
- LAN switch 1U

Total 19U

rack name: **HBL-020ROW:CNPW-U-018**

- BE 2U
- $BE_{mod}1$ 2U
- OFE 2U
- uTCA 6U
- LAN switch 1U

Total 13U

rack name: **MBL-040ROW:CNPW-U-018**

- MCTRL 3U
- uTCA 6U
- LAN switch 1U

Total 10U

rack name: **HBL-030ROW:CNPW-U-018**

- MCTRL 3U
- uTCA 6U
- LAN switch 1U

Total 10U

4.1.4. A2T WS racks

Rack name: **A2T-010ROW:CNPW-U-006**

- BE 2U
- $BE_{mod}1$ 2U
- OFE 2U
- MCTRL 3U
- uTCA 6U
- LAN switch 1U

Total 16U