



Elettra Sincrotrone Trieste

**- *Critical Design Review* -**

**The WS acquisition system  
project overview**

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*Elettra Sincrotrone Trieste*

# WS Acquisition System CDR: guidelines to the Committee

Monday, 5 March 2018

09:00 - 09:30	Arrival 30'
09:30 - 09:40	Introduction and committee charge 10' Speaker: Dr. Andreas Jansson (European Spallation Source ERIC)
09:40 - 10:00	WS acquisition system: Requirements 20' Speaker: Clement Derrez (European Spallation Source ERIC) Material: <a href="#">Slides</a> 
10:00 - 10:20	The WS Acquisition System project overview 20' Speaker: Dr. Mario Ferianis (Sincrotrone Trieste) Material: <a href="#">Slides</a>  <a href="#">document</a> 
10:20 - 10:40	Coffee break
10:40 - 11:00	Controls infrastructure 20' Speaker: Joao Paulo Martins (European Spallation Source ERIC)
11:00 - 11:30	Analog Front End & Back End Design 30' Speaker: Mr. Raffaele De Monte (Elettra) Material: <a href="#">Slides</a> 
11:30 - 12:00	Optical Front End Design 30' Speaker: Dr. Sandi Grulja (Elettra) Material: <a href="#">Slides</a> 
12:00 - 13:30	Lunch
13:30 - 14:00	Tests results at Elettra & LINAC4 30' Speaker: Mr. Raffaele De Monte (Elettra) Material: <a href="#">Slides</a> 
14:00 - 14:40	Cabling and Installation 40' Speaker: Dr. Sandi Grulja (Elettra) Material: <a href="#">Slides</a>  <a href="#">document</a> 
14:40 - 15:10	Software development, EPICS integration 30' Speaker: Stefano Cleva Material: <a href="#">Slides</a> 
15:10 - 15:30	Coffee break
15:30 - 16:00	Planning, budget, reliability, response to PDR 30' Speaker: Dr. Mario Ferianis (Sincrotrone Trieste) Material: <a href="#">Slides</a>  <a href="#">document</a> 
16:00 - 16:20	Verification strategy 20' Speaker: Clement Derrez (European Spallation Source ERIC) Material: <a href="#">Slides</a>  <a href="#">document</a> 
16:20 - 17:20	committee discussion 1h0'

WS\_SysDescription\_rev1.4\_01-03-18.pdf

WS\_Interface\_rev3.0\_23-02-18.pdf

WS\_Quality\_rev1.0.pdf

WS\_Safety\_rev2.0\_26-02-18.pdf

WS\_RAMI\_rev1.0\_19-02-18.pdf

WS\_Time Schedule\_rev1.0\_19-02-18.pdf

WSACQ 2018\_02\_26.pdf

# WS Acquisition Critical Design Review

## Objective

- ✓ Have the design approved by the Committee to start the **Production Phase**

## How

- ✓ By reviewing the design of the system
- ✓ By presenting the characteristics of the system
- ✓ By presenting the performances, so far achieved
- ✓ By presenting the cabling system & racks
- ✓ By presenting the production schedule (forecast) & budget
- ✓ By presenting the support documentation (inc. Quality, RAMI, critical paths)
- ✓ By running a real-time DEMO session

## Our design is based on:

- ✓ Design, development and integration of in-house developed HW modules
- ✓ Integration of COTS HW boards into the ESS ICS
- ✓ Development of a custom control and processing SW, running under EPICS
- ✓ Design of a suitable cabling system

## Milestone achieved, so far

- |                                            |                                 |
|--------------------------------------------|---------------------------------|
| ✓ PDR-1                                    | 2016, June 28 <sup>th</sup>     |
| ✓ PDR-2                                    | 2016, December 13 <sup>th</sup> |
| ✓ Prototype development (AFE, OFE, BE)     | mid 2017                        |
| ✓ Epics code development                   | end 2017                        |
| ✓ Test at Partner Lab (AFE+BE+SW)          | 2017, Oct,10-13 & Nov 7-10      |
| ✓ IKC Tech Annex preparation and signature | 2018, Feb/Mar                   |

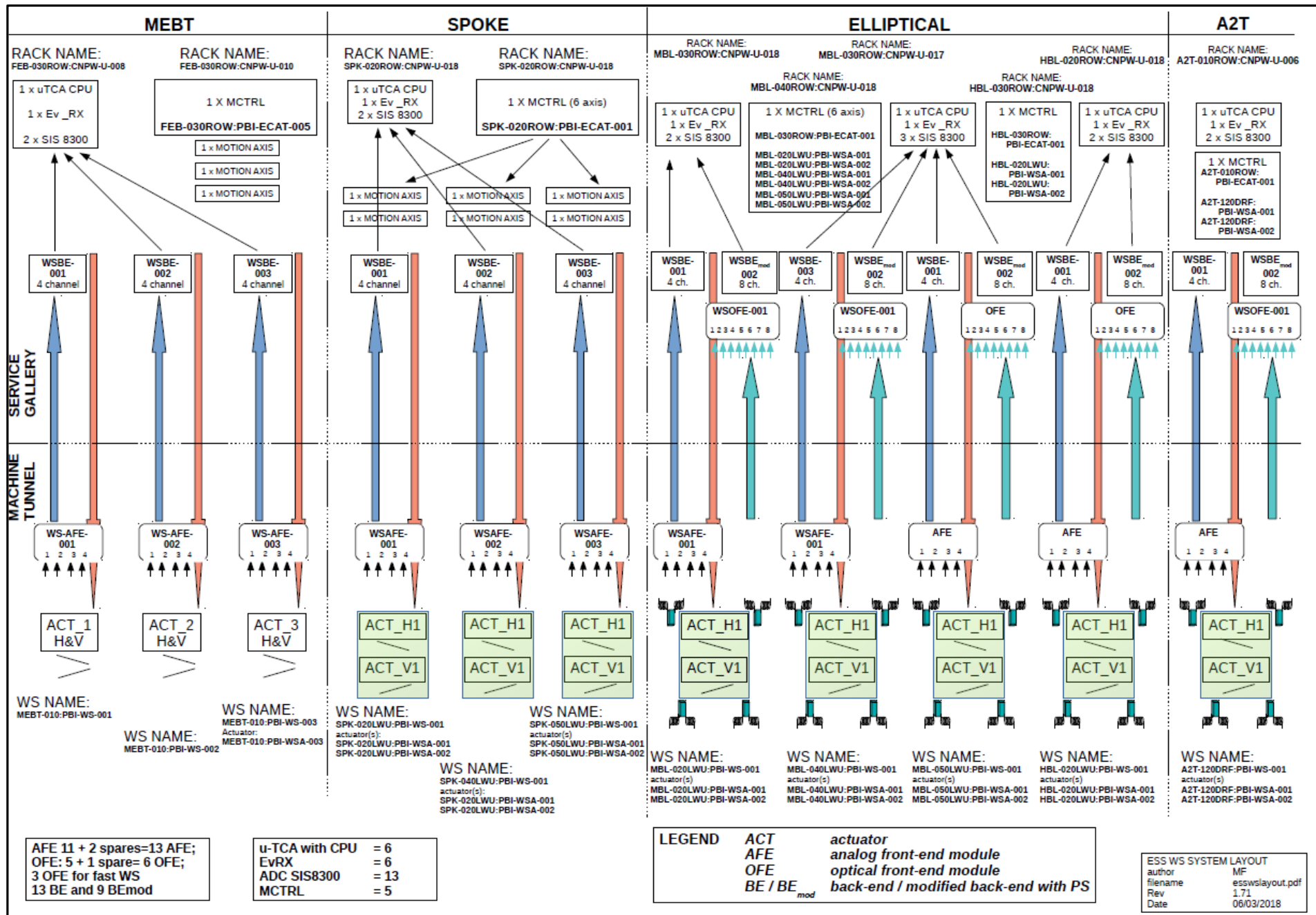
# WS ACQ SYS summary table

item	MEBT	SPOKE	ELLIPTICAL	A2T	Total	notes
<b>AFE</b>	3	3	4	1	11	+ 2 spares = <b>13</b> in total
<b>BE</b>	3	3	4	1	11	+ 2 spares = <b>13</b> in total
<b>OFE</b>	0	0	4	1	5	+1 spare + 3 FAST WS = <b>9</b>
<b>BE<sub>modified</sub></b>	0	0	4	1	5	+1 spare + 3 FAST WS = <b>9</b>
<b>SCINT</b>	0	0	4x4	1x4	20	not part of ST IKC
<b>uTCA CPU</b>	1	1	3	1	6	not part of ST IKC
<b>ADC SIS-8300</b>	2	2	7	2	13	not part of ST IKC
<b>EV_RX</b>	1	1	3	1	6	not part of ST IKC
<b>Motion Controller (3 axis)</b>	1 (3)	1 (6)	2 (6+2)	1 (2)	5	not part of ST IKC

## acronyms

- ✓ **AFE** analogue front end
- ✓ **BE** back end (4 ch. Module)
- OFE** optical front end (8 channel module)
- Be<sub>mod</sub>** Modified back end (8 ch. module)

# WS ACQ SYS block diagram



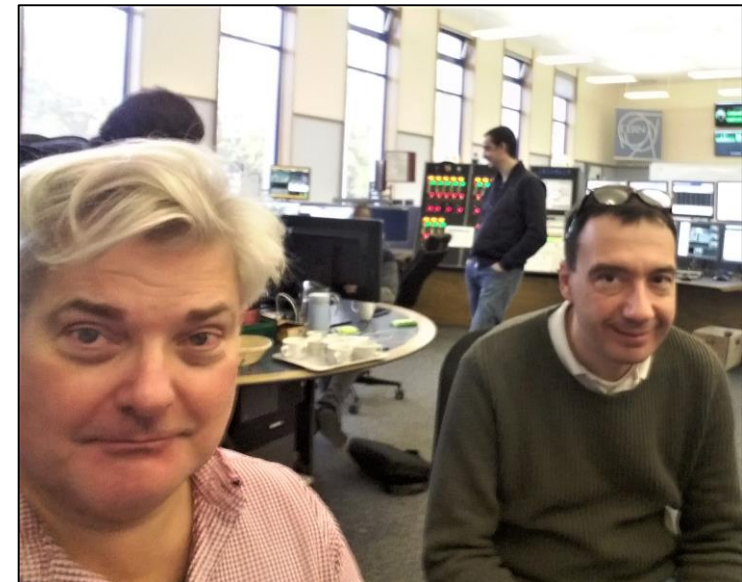
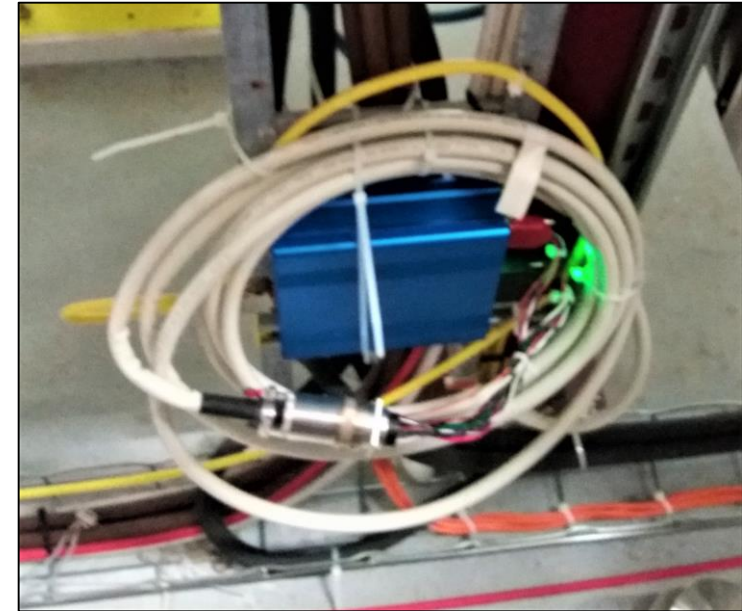
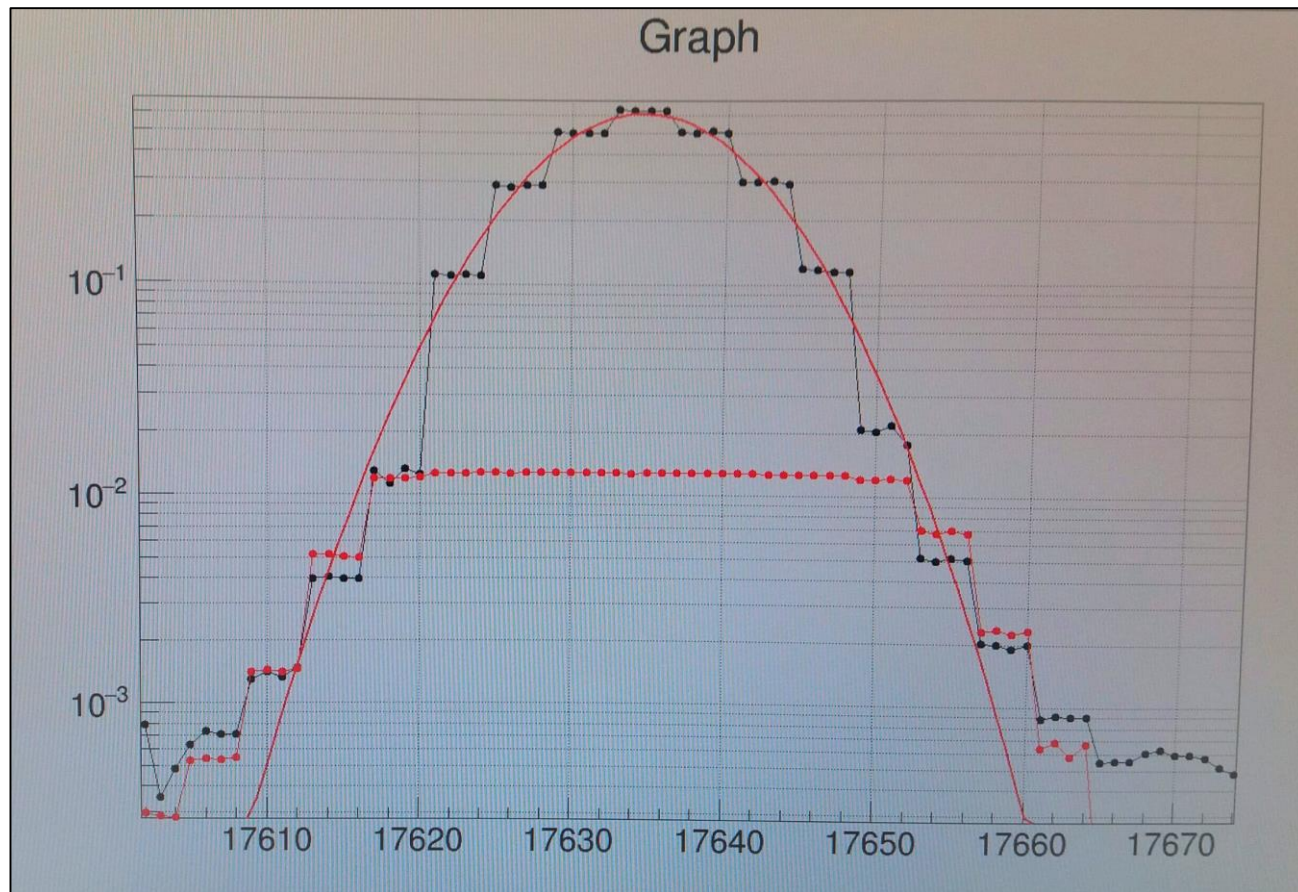
## SEM section: AFE + BE

- |                              |                                     |
|------------------------------|-------------------------------------|
| ✓ AFE / BE design            | completed                           |
| ✓ Prototype construction     | completed                           |
| ✓ In-house testing           | done                                |
| ✓ Test with beam             | done                                |
| ✓ ICS Integration            | running, <b>done 80%</b>            |
| ✓ Acceptance Test definition | running, <b>done 25%</b>            |
| ✓ Production set-up          | running, <b>done 20%</b> (PCB, BoM) |



## SEM section: AFE + BE

Snapshots from **Test at CERN** on LINAC4  
(Oct – Nov / 2017)



## SCINT section: OFE + BE<sub>mod</sub>

- ✓ OFE design completed
- ✓ BE<sub>mod</sub> design completed
- ✓ Prototype construction completed
- ✓ In-house testing done
- ✓ Test with beam **scheduled** for Spring 2018 at CERN
- ✓ Scintillator prototype **running** (external task, Slava G.)
- ✓ ICS Integration running, **done 50%**
- ✓ Acceptance Test definition running, **done 75%**
- ✓ Production set-up running, **done 20%** (PCB, BoM)



**SCINT section: OFE + BE<sub>mod</sub>**

**Optical Front End:**

is it really a prototype ??

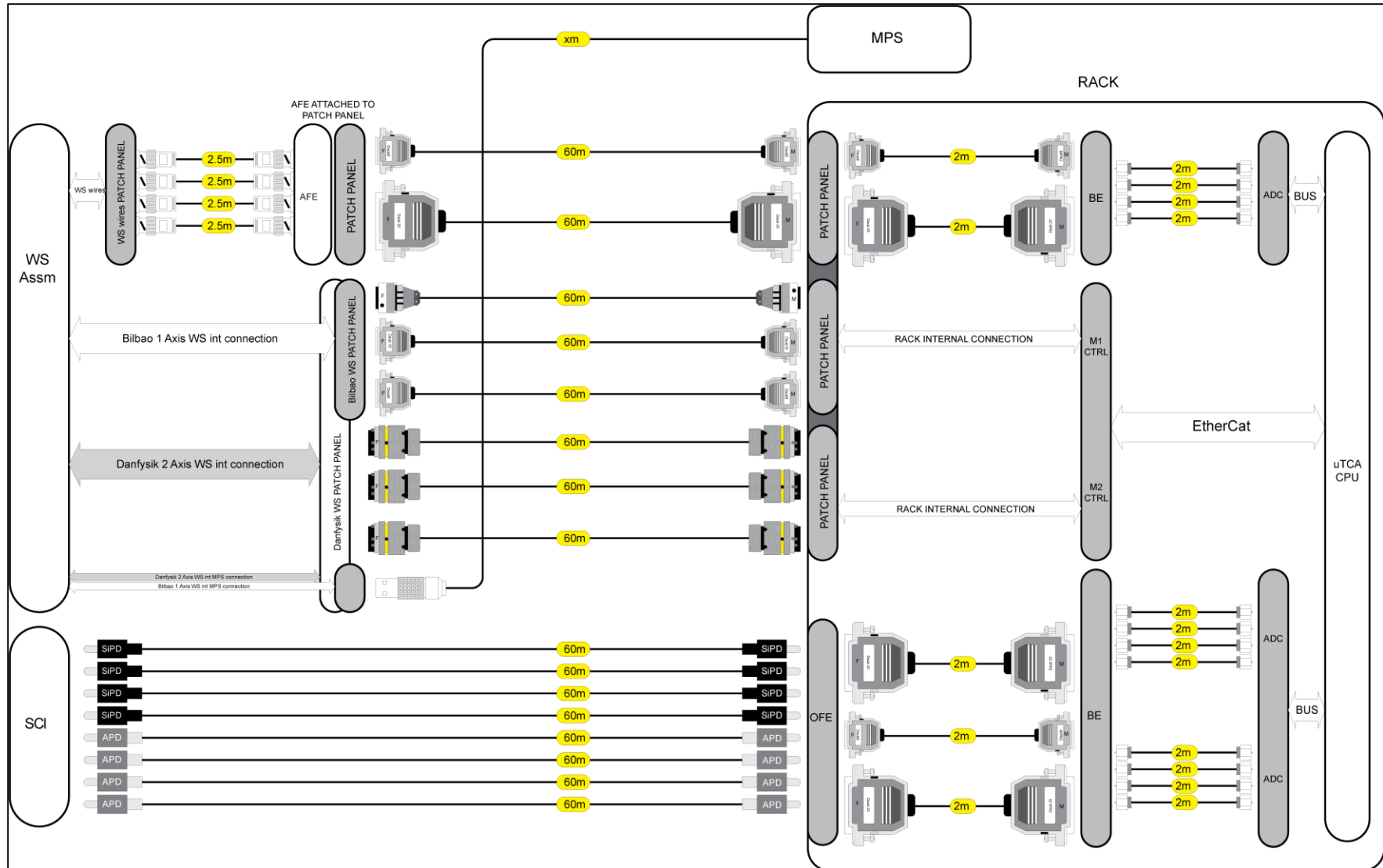


## Racks & cabling

- |                                             |                             |
|---------------------------------------------|-----------------------------|
| ✓ Cabling specifications                    | completed                   |
| ✓ Cabling documentation                     | completed                   |
| ✓ WS on-board cabling                       | completed (with ESS Bilbao) |
| ✓ Long run cable list                       | completed                   |
| ✓ Rack identification                       | completed                   |
| ✓ Rack layout                               | completed                   |
| ✓ In-rack cabling                           | running, <b>done 50%</b>    |
| ✓ AFE to BE communication                   | tested with beam            |
| ✓ OFE to BE <sub>mod</sub> via Fiber Optics | completed                   |
| ✓ Final cabling and signal double check     | running, <b>done 50%</b>    |

## Racks & cabling

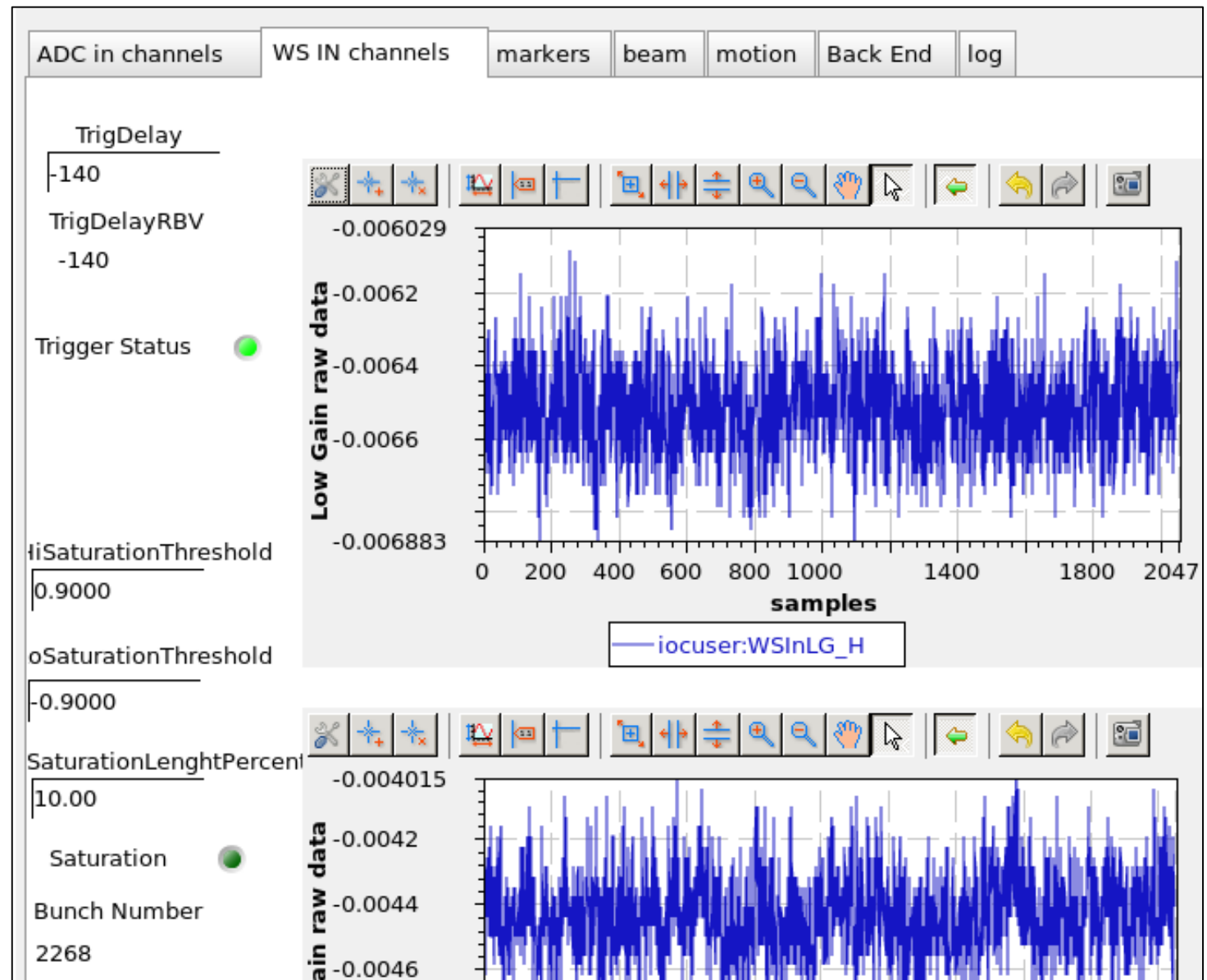
### MEBT WS cabling diagram



## WS software

- |                                          |                          |
|------------------------------------------|--------------------------|
| ✓ Control software specifications        | completed                |
| ✓ $\mu$ -TCA / EPICS dev. system set up  | done                     |
| ✓ Low level integration /link to ICS IOC | done                     |
| ✓ Motion controller integration          | done                     |
| ✓ Event / timing system integration      | done                     |
| ✓ Control panel                          | running, <b>done 75%</b> |
| ✓ Engineering panel                      | running, <b>done 75%</b> |
| ✓ Data post processing                   | running, <b>done 75%</b> |

## WS software Control Panel



Task #	Description	notes
1	System design	SEM section and SCINT section
2	PDR-1	SEM section
3	PDR-2	SCINT section
4	Prototype construction	SEM and SCINT
5	Prototype in-house test	SEM and SCINT
6	Prototype test at Partner lab	SEM
7	CDR	jointly, SEM and SCINT
8	Prototype test at Partner lab	SCINT
9	WS Vertical test (mech+ACQ SYS)	at ESS
10	Series construction	SEM
11	SEM Series in-house acceptance	at Elettra
12	SEM series delivery to ESS	
13	SAR-1	Acceptance test at ESS / SEM
14	Series construction	SCINT
15	SCINT series in-house acceptance	at Elettra
16	SCINT series delivery to ESS	
17	SAR-2	Acceptance test at ESS / SCINT



# WS Acquisition System: schedule

















































ID	i	Milestone	Task Name	Duration	Start	Finish	Prede
1			<b>WSACQ</b>	859 days	01/10/15	11/01/19	
2		1	Kick-off meeting	0 days	01/10/15	01/10/15	
3		2	ESS final specification for the scintillator	0 days	01/04/16	01/04/16	
4			WS ACQ SYS layout definition	198 days	01/10/15	30/06/16	
5			Design of SEM prototype	198 days	01/10/15	30/06/16	
6			SEM ICS integration preliminary design	132 days	01/01/16	30/06/16	
7		4	PDR-1 Full system SEM (ICS+AD)	0 days	28/06/16	28/06/16	
8			Shipment of 1st ICS development station to Elettra	0 days	15/02/17	15/02/17	
9			SEM ACQ SYS design	88 days	01/06/16	30/09/16	
10			SEM board&module; prototype & characterization	195 days	01/09/16	31/05/17	
11			Controls Detailed Design Document	0 days	16/12/16	16/12/16	
12			Control Acceptance Test Plan	0 days	30/06/17	30/06/17	
13			SEM prototype integration in ICS	97 days	01/12/16	14/04/17	
14			SEM ICS engineering and interface panels	108 days	15/02/17	14/07/17	8
15			SEM ICS computation SW	108 days	15/02/17	14/07/17	8
16			SCINT detection prototype design	87 days	01/09/16	31/12/16	
17			SCINT ICS integration design	195 days	01/11/16	31/07/17	
18		6	PDR- 2 - Full system SCINT	0 days	13/12/16	13/12/16	
19			Shipment of 2nd ICS development station to Elettra	0 days	31/10/17	31/10/17	
20			Delivery of final uTCA boards to Elettra	0 days	31/10/17	31/10/17	
21			SCINT ACQ SYS prototype	65 days	02/01/17	31/03/17	
22			SCINT ACQ SYS CDR Data package	109 days	01/03/17	31/07/17	
23			SCINT PROTOTYPE characterization	129 days	01/02/17	31/07/17	
24			SCINT prototype integration in ICS	44 days	31/10/17	29/12/17	19
25			Delivery of one Danphysique mechanical WS assembly to ESS	0 days	15/06/17	15/06/17	
26			SCINT ICS engineering and interface panels	44 days	31/10/17	29/12/17	19
27			SCINT computation SW	44 days	31/10/17	29/12/17	19
28		9	CDR- 1 - Full system design SEM (ICS+AD)	2 days	05/03/18	06/03/18	
29		11	CDR- 2 - Full system design (SCINT)	2 days	05/03/18	06/03/18	

Differently from what originally planned, also due to the overall ESS project delays, the developments of the two sub-systems of the WS ACQ SYS, the SEM section and the SCINT section, ended almost at the same time resulting in a single CDR.

There are also some other minor changes from what originally foreseen, like:

- line 19 *shipment of the 2<sup>nd</sup> dev. station to Elettra* .... never accomplished
- line 20 *delivery of final  $\mu$ -TCA acq. board* ..... never accomplished
- line 25 *delivery of WS mech. assembly* ..... never accomplished

# WS Acquisition System: schedule

28	 	9	CDR- 1 - Full system design SEM (ICS+AD)	2 days	05/03/18	06/03/18	
29	 	11	CDR- 2 - Full system design (SCINT)	2 days	05/03/18	06/03/18	
30	 		setup TRR data package	216 days	06/11/17	03/09/18	
31	 	15	TRR -Test readiness for SEM prototype	0 days	14/09/18	14/09/18	
32	 		In-house test of SEM boards (AFE+BE)	86 days	01/02/17	31/05/17	
33	 	12	Vertical test in lab: test of WSAS on WS MECH at ESS	22 days	19/04/18	18/05/18	25
34	 		SEM Prototype TESTED (no beam)	0 days	30/06/17	30/06/17	
35	 		arrange AFE module test at partner lab; including ICS part	119 days	04/04/17	15/09/17	
36	 	7	(AFE+BE+ADC) module test at partner lab	29 days	10/10/17	17/11/17	
37	 		AFE Prototype TESTED (with beam, @PARTNER LAB)	0 days	17/11/17	17/11/17	36
38	 		Construction budget release after Signature	0 days	23/02/18	23/02/18	
39	 		SEM PO for: Components; PCB; Assembly	24 days	23/02/18	28/03/18	38
40		14	Delivery of first series to ESS (SEM)	60 days	29/03/18	20/06/18	39
41	 		Manufacturing of SEM module series	56 days	21/06/18	06/09/18	40
42	 		In-house acceptance test of SEM module series	19 days	07/09/18	03/10/18	41
43	 		Shipment to ESS – SEM modules	5 days	04/10/18	10/10/18	42
44	 		Delivery of SCINT prototype by ESS	0 days	27/04/18	27/04/18	
45	 	13	SCINT detector prototype test at Partner facility (SCINT)	25 days	27/04/18	31/05/18	44
46	 		SCINT mode TESTED	0 days	31/05/18	31/05/18	45
47	 		SCINT PO for: Components; PCB; Assembly	50 days	01/06/18	09/08/18	46
48			Manufacturing of SCINT Module series	80 days	10/08/18	29/11/18	47
49	 		In-house acceptance test of SCINT module series	20 days	30/11/18	27/12/18	48
50	 	17	SAR-1 SEM only	0 days	12/10/18	12/10/18	43
51	 		Shipment to ESS – OFE modules	11 days	28/12/18	11/01/19	49
52	 		COTS hardware available & tested at ESS site	0 days	01/06/18	01/06/18	
53	 	21	SAR-2 Full system SCINT	0 days	11/01/19	11/01/19	51

- line 32 *in-house test of SEM boards* .... completed
- line 34 *SEM prototype tested* .... completed
- line 35 *arrange AFE module test at Partner Lab* .... completed
- line 36 *(AFE+BE+ADC) module test at P. Lab.* .... completed
- line 37 *AFE prototype tested (with beam at P. Lab.)* completed

- SCINT test at Partner lab line 45
- Vertical integration with one mechanical set-up line 33
- Production of the two series: SEM and SCINT lines 39 to 41  
lines 47 to 48
- Acceptance test, in-house at Elettra lines 42 & 49
- Shipment to ESS lines 43 & 51
- SAR, 1 and 2 lines 50 & 53

## Vertical Integration Test (VIT)

- ✓ Multi partner effort (Elettra, ESS diag & ICS, ESS bilbao...)
- ✓ At ESS, in a suitable laboratory: faster debugging and fixing
- ✓ The final output of the VIT is the synchronous acquisition of both the AFE and OFE outputs while the WS is moving, either in “**fly mode**” or “**step by step mode**”, while both electrical pulse generator and diode laser are generating pulses of programmable and variable amplitude (*to mimic the signals generated during a WS scan*). Once the scan is over, the FW processes the acquired data and plots the calculated profile
- ✓ Test the WS ACQ SYS integration & portability into ESS / ICS
- ✓ Test the interfacing to the WS mechanics

## Install a full prototype system in LEBT

- ✓ Test the cabling system in-situ

## Finalize the acceptance tests @ ESS

- ✓ Key task for successful SAR completion

## Start and complete the series production (SEM & SCINT)

- ✓ Agree on delivery / shipment schedule



- WS ACQ SYS with:
  - AFE prototype
  - BE prototype
  - $\mu$ -TCA crate with boards (CPU, ADC, EV\_Rx)
  - Motion controller
  - OFE prototype
  - BE<sub>mod</sub> prototype
  - Short WS ACQ SYS cables
  - Control panel
  - Engineering panel
  - Acquired data processing
- Long Run cables (short stub)
- Local Ev\_gen with FO output
- Local control PC / WS
- Local PLC to mimic machine safety I/Os
- Pulse generator to mimic beam current
- Diode laser to mimic scintillator light signal
- anything else I may have forgotten

- **Production schedule and budget**
- **Quality**
- **Safety**
- **RAMI**
- **Risk Assessment**



**Thank You!**